Data Converters

IC Handbook

October 1994

GEC PLESSEY
SEMICONDUCTORS

DATASHEET ANNOTATION

GPS annotate datasheets in the top right hand corner of the first page, to indicate product status. These annotations are as follows:-

TARGET SPECIFICATION

This is the most tentative form of information and represents a very preliminary product specification. No actual design work on the product has started.

PRELIMINARY INFORMATION

The product is in design and development. The datasheet represents the product as it is understood but details may change.

ADVANCE INFORMATION

The product design is complete and final characterisation for volume production is well in hand.

No annotation

The product parameters are fixed and the product is available to datasheet specification in volume.

If you have any queries about the status of any GPS product, please contact your nearest GPS Customer Service Centre.

DATA CONVERTERS

IC Handbook

GEC PLESSEY

SEMICONDUCTORS

Foreword

GEC Plessey Semiconductors is recognised as a supplier of the very best in data conversion products meeting the requirements of a wide customer base. Access to a broad range of process technologies allows GPS to get the most out of its designs; so whether you need high speed, low cost, good linearity or whatever, there's a good chance that GPS can offer the right product to meet your needs. Recent developments have focused on video bandwidth ADCs and DACs and many of these devices are offered in support of our video processing ICs (as detailed in the Digital Video and DSP handbook).

Increasingly the trend in many applications is for the data conversion function to become up-integrated into larger system chips. Indeed GPS offers a number of products with embedded data converters. But we also recognise that there is a need to maintain a range of standard ADCs and DACs and this handbook details those products which best serve the needs of our customers for general purpose and specialised higher performance data converter devices. GPS also maintains a comprehensive selection of voltage references - ranging from the latest ultra miniature 1% tolerance VR25 to the well established and extremely popular ZN458 and REFxx ranges.

And lastly, if you're not so familiar with data conversion techniques or want to know how to get the best out of your system designs then check out the Applications Notes section of this handbook. In there you will find a wealth of knowledge and advice based on the many years experience of our design and applications engineers.

Contents

Product index

Video/Graphics DACs

Type No.	Function	Minimum clock rate (MHz)	DAC max. rise time (ns) (10% to 90%)	Process	Page
MV95308	8-bit video DAC	30	6.0	CMOS	13
MV95408	8-bit video DAC	50	5.5	CMOS	18
SP98608	8-bit latched multiplying DAC	450	0.8	Bipolar	23
VP101	Triple 8-bit video DAC	30/50	9.0	CMOS	28

Advanced Function DACs

Type No.	Function	Linearity error (LSB)	Settling time (µs)	On-chip reference	Special features	Page
ZN425	8-bit DAC/ADC	±0.5	1.0	Yes	8-bit counter	37
ZN426	8-bit DAC	±0.5	1.0	Yes	Low cost	43
ZN428	8-bit microprocessor-compatible DAC	±0.5	0.8	Yes	Data latch	47
ZN429	8-bit DAC	±0.5	1.0	No	Low cost	55

Advanced Function ADCs

Type No.	Function	Linearity Options (LSB)	Conversion time (µs)	On-chip Clock	Special features	Page
ZN427	8-bit microprocessor-compatible ADC	±0.5	10	No	Three-state data outputs	63
ZN448	8-bit microprocessor-compatible ADC	±0.5	9	Yes	Three-state data outputs	78
ZN449	8-bit microprocessor-compatible ADC	±1.0	9	Yes	Three-state data outputs, low cost	78

NOTE
All Advanced Function ADCs have on-chip reference

Video and High Speed ADCs

Type No.	Function	Minimum clock rate (MHz)	Process	Page
SP973T8	8-bit flash ADC (TTL/CMOS outputs)	30	Bipolar	97
SP97504	4-bit expandable ADC (replaces SP9754)	110	Bipolar	103
SP97508	8-bit flash ADC	110	Bipolar	107
VP1058	8-bit video ADC	25	Bipolar	114
VP8708	8-bit analog video input interface	30	Bipolar	120
VP87A8	8-bit analog video input interface	32	Bipolar	128
VP87A9	8-bit analog video input interface	30	Bipolar	136

Micropower Fixed Voltage References

Type No.	Nominal voltage (V)	Guaranteed Knee current (μA)	Slope resistance (Ω)	Maximum temperature coefficient (ppm/°C)	Operating temperature range (°C)	Page
REF12D	1.26	90	4.0	80	-40 to +85	147
REF12Z	1.26	90	4.0	56	-40 to +85	147
REF25D	2.50	60	2.0	80	-40 to +85	153
REF25Z	2.50	60	2.0	110	-40 to +85	153
REF50D	5.00	60	3.5	80	-40 to +85	159
REF50Z	5.00	60	3.5	110	-40 to +85	159

SOT-23 Micropower Bandgap Voltage References

Type No.	Nominal voltage (V)	Guaranteed Knee current (μA)	Slope resistance (Ω)	Maximum temperature coefficient (ppm/°C)	Operating temperature range (°C)	Page
SR12D	1.23	90	2.5	125	-40 to +85	167
SR25D	2.50	80	2.0	90	0 to +70	170
VR25	2.50	80	0.2	150	-40 to +85	173

Fixed Voltage References

Type No.	Nominal voltage (V)	Guaranteed current (mA) Min.	Max.	Slope resistance (Ω)	Maximum temperature coefficient (ppm/°C)	Operating temperature range (°C)	Page
ZN404	2.45	2	120	0.4	145	0 to +70	181
ZN404D	2.45	2	120	0.4	145	-20 to +70	181
ZN423	1.26	1.5	12	1.5	101	-55 to +125	184
ZN458	2.45	2	120	0.2	99	-20 to +70	189
ZN458A	2.45	2	120	0.2	49	-20 to +70	189
ZN458B	2.45	2	120	0.2	29	-20 to +70	189

Standard ECL

Type No.	Function	Supply voltage (V)	Frequency (MHz)	Power (mW)	Page
SP1648	Voltage controlled oscillator	+5 or -5.2	225	150	195

Product List - Alpha numeric

The Quality Concept

Quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes (followed by strict control and on-going assessment) that quality products will be produced.

All designs conform to standard layout rules, all processes are thoroughly evaluated and all new piece part designs and suppliers are investigated before authorisation for production use.

The same basic procedures are used on all products up to and including device packing. It is only then that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures, all users benefit; the high reliability user gains the advantage of scale (hence improving the confidence factor in the quality achieved), while the volume user gains from the benefits of basic high reliability design concepts.

GEC Plessey Semiconductors (GPS) have the following factory approvals:
AQAP1
BS9450 (Capability Approval)
MIL-STD-883 Class B (In conformance with the requirements of MIL-STD-883, paragraph 1.2.1)
DESC (Department of Electronics Supply Center - Device approvals)

Screening

Different screening procedures are carried out by GPS; a brief description of the differences involved are set out in Tables 1 and 2.

Stage/ operation	Standard product	GPS Hi-rel A	GPS Hi-rel B	MIL-STD-883 Class B	MIL-STD-883 Class S[1]
Wafer-fab					Wafer-lot accept Method 5007
Probe test	100%	100%	100%	100%	100%
Visual inspect chips	Usually 2010 Cond.B	2010 Cond.B	2010 Cond.B	2010 Cond.B	2010 Cond.A
Assemble					Includes 100% bond pull
Screen	None	Method 5004 Class B	As Table 2	Method 5004 Class B	Method 5004 Class S
Test	100%	100%	100%	100%	100%
Conformance testing	None	Method 5005 Class B Group A Group B Group C Group D	None	Method 5005 Class B Group A Group B Group C Group D	Method 5005 Class S Group A Group B Group C Group D

Table 1

1. MIL-STD-883 Class S/ESA SCC9000: GPS has supplied numerous devices to customer specifications for Space and Satellite applications. Please contact your local GPS sales office for information.

Stage/ operation	GPS Hi-rel B (References are to MIL-STD-883)	MIL-STD-883 Class B Method 5004[2]
Internal Visual	Method 2010 Test Condition B 100%	Method 2010 Test Condition B 100%
Stabilisation Bake	Method 1008 24Hrs at Condition C 100%	Method 1008 24Hrs at Condition C 100%
Temperature Cycling	Method 1010 Test Condition C 100%	Method 1010 Test Condition C 100%
Constant Acceleration	Method 2010 Condition E Y1 only 100%	Method 2010 Condition E Y1 only 100%
Visual Inspection		100%
Initial Electrical	Those parameters requiring Delta calculations. 100%	Those parameters requiring Delta calculations. 100%
Burn-In	Method 1015 160Hrs at 125°C min. 100%	Method 1015 160Hrs at 125°C min. 100%
Post Burn-In Electrical Test	Full Electrical Test to Guarantee datasheet. 100%	Those parameters requiring Delta calculations. 100%
PDA Calculation	5% max. All lots	5% max. All lots
Final Electrical Test	Done as Post Burn-In Test. 100%	Full Group A tests as Method 5005. 100%
Seal (a) Fine Seal (b) Gross	Method 1014 100%	Method 1014 100%
Qualification/Quality Conformance Test		Method 5005 Class B Samples as necessary
External Visual	GPS Spec. sample	Method 2009 100%

Table 2

2. See Section 5 for further information.

Section 1
Video/Graphics DACs

GEC PLESSEY
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DS2431-2.1

MV95308

30MHz 8-BIT CMOS VIDEO DAC

The MV95308 is a CMOS 8-bit, 30MHz Digital to Analog converter, designed for use in both video graphics and general digital television applications.

A very low external component count has been achieved by including the loop amplifier and reference voltage source on chip.

The device contains a data input register and registered video controls ($\overline{\text{BLANK}}$, $\overline{\text{REFWHITE}}$, $\overline{\text{OVERBRT}}$ and $\overline{\text{SYNC}}$). These control inputs and associated internal circuitry allows the MV95308 to be used in video graphics systems by providing the necessary video pedestal levels. The $\overline{\text{STRDAC}}$ input allows the video pedestals to be disabled in conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard RS-343A or RS-170 video levels, using the appropriate R_{SET} external resistor.

Pull up resistors have been added to tie all unused control inputs into their inactive (High) states.

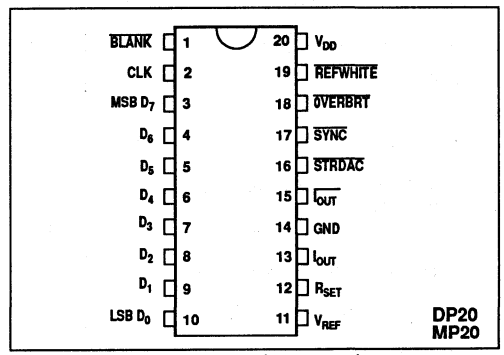


Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption (180mW Typ)
- 30MHz Pipeline Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Levels
- On Chip Reference Voltage Source
- Guaranteed Monotonic
- Drives 75Ω Loads Directly
- Single 5V Power Supply

ORDERING INFORMATION

MV95308 ADG (Military - Ceramic DIL Package)
MV95308 CDP (Commercial - Plastic DIL Package)
MV95308 CMP (Commercial - Miniature Plastic DIL Package)

APPLICATIONS

- Data Conversion (general)
- Computer Graphics
- Waveform Synthesis
- Consumer TV
- Instrumentation

ABSOLUTE MAXIMUM RATINGS (Reference to GND)

DC Supply Voltage, V_{DD}		-0.3 to +7V
Digital Input Voltage		-0.3 to V_{DD} +0.3V
Analog Output Short Circuit Duration		Indefinite
Ambient Operating Temperature	A grade	-55°C to +125°C
	C grade	0°C to + 70°C
Storage Temperature Range		-55°C to +125°C

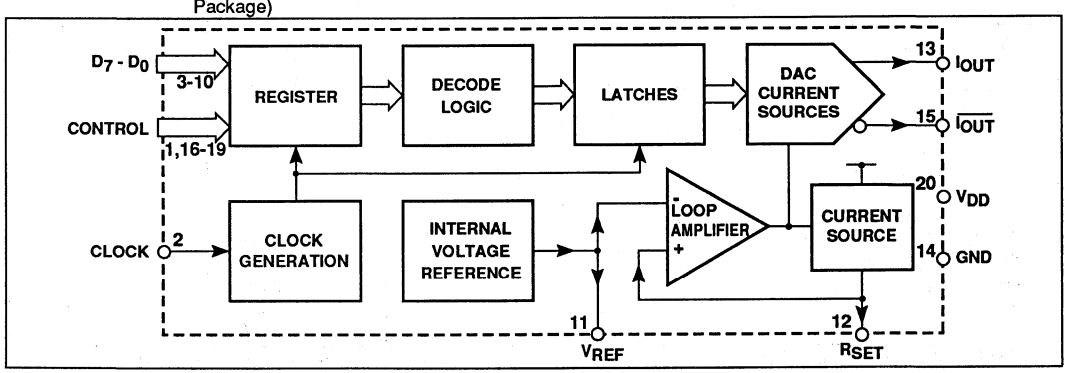


Fig.2 Block diagram of MV95308

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):
As specified in recommended operating conditions. Full temperature range: A grade = -55°C to +125°C, C grade = 0 to 70°C

DC CHARACTERISTICS

Parameter	Symbol	Temp (°C)	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution		Full	8			Bits	
Integral linearity error	INL	25		±0.5		LSB	
		Full			±1	LSB	
Differential linearity error	DNL	25		±0.5		LSB	
		Full			±1	LSB	
Gain error		25		±1%	±5%	%	Of full scale
Analog output							
Grey scale current range		25		8.8		mA	75Ω singly terminated load R_{SET} = 1.8kΩ (graphics mode)
				255		LSB	
10% Over Bright level relative to White level		25	26	27	28	LSB	
				10		IRE	
White level relative to Blank level		25	275	276	277	LSB	
				100		IRE	
Black level relative to Blank level		25	20	21	22	LSB	
				7.5		IRE	
White level relative to Black level		25		255		LSB	
				92.5		IRE	
Blank level		25	107	111	115	LSB	
				40		IRE	
Sync level		25		0		LSB	
LSB size	LSB	25		2.58		mV	
Output compliance	V_{OC}	25	-0.3		+1.5	V	
Digital inputs							
High level I/P voltage	V_{IH}	25	3		V_{DD}+0.3	V	
Low level I/P voltage	V_{IL}	25	GND-0.3		1.2	V	
High level I/P current	I_{IH}	25			+1	µA	
Low level I/P current	I_{IL}	25			-1	µA	
Internal voltage reference (V_{REF})	V_{REF}	25	0.95	1.0	1.05	V	
		Full	0.90		1.10	V	
V_{REF} temperature coefficient				40		ppm/°C	

AC CHARACTERISTICS (Refer to Fig. 3)

Parameter	Symbol	Temp (°C)	Value Min.	Value Typ.	Value Max.	Units	Conditions
Max clock rate	f_{MAX}	Full	30			MHz	maximum guaranteed freq.
Clock high time	t_{CLKH}	25	10			ns	
Clock low time	t_{CLKL}	25	10			ns	
Data and control setup time	t_{SU}	25	8			ns	
Data and control hold time	t_H	25	2			ns	
Analog output delay	t_{DLY}	25		10		ns	
Analog output rise/fall time	t_{RF}	25		3	6	ns	
Analog output settling time	t_S	25		15		ns	
Glitch energy		25		100		pV-sec	
V_{DD} supply current	IDD	25		30		mA	fc = 15MHz
				36		mA	fc = 30MHz

THERMAL CHARACTERISTICS

Thermal Resistance	DP	MP	
Chip to case θ_{jC}	20	30	°C/W
Chip to ambient θ_{jA}	75	93	°C/W

RECOMMENDED OPERATING CONDITIONS

R_{LOAD} (I_{OUT} and $I_{\overline{OUT}}$)	75Ω
V_{DD}	5.0V ± 0.5V
R_{SET} (graphics applications)	1.8kΩ
R_{SET} (straight DAC applications)	1.2kΩ

CIRCUIT DESCRIPTION

As illustrated in the function block diagram, Fig. 2, the MV95308 contains an 8-bit D-to-A converter, input registers, a loop amplifier and a voltage reference.

On the falling edge of each clock cycle, as shown in Fig. 3, eight data bits are latched into the device and passed to the 8-bit D-to-A converter. Also latched on the falling edge of the clock signal, the $\overline{SYNC}$ and $\overline{BLANK}$ inputs add the necessary weighted currents to the analog outputs to produce the required output levels for use in video applications. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$, $\overline{REFWHITE}$ and $\overline{OVERBRT}$ inputs modify the DAC output levels.

To obtain a high data throughput rate, the decoding logic of the MV95308 is fully pipelined. This introduces a one clock cycle delay between the latching of the input data and the resultant DAC output.

It also ensures synchronisation of the internal data and a minimal output glitch energy.

The DAC employed by the MV95308 eliminates the need for precision component ratios by using segmented architecture in which equal weight bit currents are either routed to I_{OUT} or $\overline{I_{OUT}}$. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed.

The MV95308 eliminates the need for an external voltage reference by providing a nominally 1.0V reference on chip. An on-chip loop amplifier also provides stability of the full scale output current against power supply and temperature variations. The full scale output current is set by an external resistor R_{SET}. By adjustment of this value it is possible to implement RS-343A or RS-170 video levels as explained in the application notes.

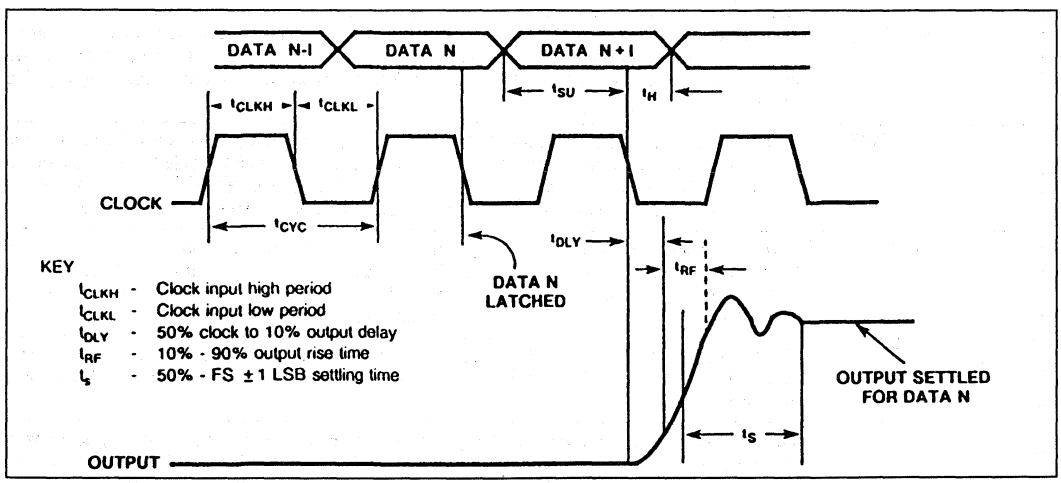


Fig.3 Timing diagram

Description	$\overline{STRDAC}$	$\overline{SYNC}$	$\overline{BLANK}$	$\overline{REFWHITE}$	$\overline{OVERBRT}$	OUTPUT DATA	I_{OUT} (LSB)
REFWHITE + 10%	1	1	1	0	0	X	414
REFWHITE	1	1	1	0	1	X	387
FULL WHITE	1	1	1	1	1	$FF	387
OVERBRIGHT	1	1	1	1	0	DATA	DATA + 132 + 27
FULL BLACK	1	1	1	1	1	$00	132
BLANK	1	1	0	X	X	X	111
DATA-SYNC	1	0	1	1	1	DATA	DATA + 21
SYNC	1	0	0	X	X	X	0
STRDAC MODE	0	X	1	1	X	DATA	DATA

Table 1: Video output truth table

Pin	Name	Description
2	CLK	**The clock input.** The falling edge of the clock latches the $\overline{DATA}$, $\overline{BLANK}$, $\overline{SYNC}$, $\overline{OVERBRT}$ and $\overline{REFWHITE}$ inputs into the logic pipeline. The decoded data will be latched into the DAC output 1 clock cycle later. The clock frequency determines the update rate of the DAC output.
3-10	D_7-D_0	**The data inputs.** D_0 is the least significant bit (LSB). The coding is in straight binary only.
13,15	I_{OUT}, $I_{\overline{OUT}}$	**The current output and its complement.** These are the high impedance current source outputs of the DAC capable of driving a 75Ω load up to a voltage of 1.5V.
14	GND	**Analog ground for the DAC.**
20	V_{DD}	**Analog power for the DAC**
11	V_{REF}	**The output of the internal voltage reference generator.** This output is nominally 1V, and should be decoupled with a 10nF capacitor.
12	R_{SET}	**The full scale adjust control.** The R_{SET} resistor is connected from this pin to ground. An internal loop amplifier adjusts a reference current flowing through the R_{SET} resistor so that the voltage across the resistor is equal to the V_{REF} voltage. This reference current has a weighting equal to 16 LSB's.
1	$\overline{BLANK}$	**The composite blank control input.** A logical zero on this input removes the Black pedestal from the I_{OUT} output, whilst forcing the internal data to the DAC to $00. This input is latched on the clock falling edge and will override the $\overline{REFWHITE}$ and $\overline{OVERBRT}$ inputs. The Black pedestal is 7.5 IRE units (actually 21 LSB's). If left open circuit this input is internally tied high.
17	$\overline{SYNC}$	**The composite sync control input.** A logical zero on this input removes the Blank pedestal from the I_{OUT} output. The Blank pedestal is nominally 40 IRE units (actually 111 LSB's). The $\overline{SYNC}$ input does not override any other control lines. This input is latched on the clock falling edge. If left open circuit this input is internally tied high.
19	$\overline{REFWHITE}$	**The reference white level control input.** A logical zero on this input overrides the input data, forcing the data to $FF. The $\overline{BLANK}$ input will override this input. If left open circuit this input is internally tied high.
18	$\overline{OVERBRT}$	**The 10% overbright control input.** A logical zero on this input switches the Overbright pedestal into the I_{OUT} output. The Overbright pedestal is 10 IRE units (actually 27 LSB's). This input does not override any other input. The $\overline{BLANK}$ input overrides this input. If left open circuit this input is internally tied high.
16	$\overline{STRDAC}$	**The straight DAC control input.** A logical zero on this input causes the Black, Blank and Overbright pedestals to be disabled, removing them from both I_{OUT} and $I_{\overline{OUT}}$. This allows the DAC contribution to the output to be extended to a full 1 Volt. To obtain this extra DAC range, it is necessary to reduce the R_{SET} resistor value, see application notes. The $\overline{BLANK}$ the $\overline{REFWHITE}$ inputs may still be used to force the input data to $00 or $FF respectively. With the $\overline{STRDAC}$ pin held low the output current can be calculated from: Output current = Data x 1 LSB Where 1 LSB= $\frac{V_{REF}}{16 \times R_{SET}}$ Full scale = 255 LSB V_{REF} = 1.0V typ. The exact value of 1 LSB must be calculated from the full scale output. If left open circuit this input is internally tied high and the device will be configured for video graphics. In this mode the output current can be calculated from: Output current = (DATA + 21 + 111) x 1 LSB V_{REF} = 1.0V typ.

APPLICATIONS INFORMATION

RS-343A and RS-170 Video Generation

For generation of RS-343A compatible video levels (see Fig.4) it is recommended that a singly terminated 75Ω load be used with an R_{SET} resistor value of approximately 1.82kΩ

Similarly for the generation of RS-170 video levels a singly terminated 75Ω load should be used but in association with an R_{SET} value of approximately 1.29kΩ to provide the increased voltage range.

Non-Video Applications

The MV95308 may be used in non-video applications as explained in the pin description for $\overline{STRDAC}$ mode.The relationship between R_{SET} and the full scale output current has been explained previously and for a singly terminated 75Ω load an R_{SET} resistor value of approximately 1.19kΩ should be used.

PCB LAYOUT CONSIDERATIONS

The PCB layout should provide low noise on the MV95308 power and ground lines by shielding the digital inputs and providing adequate decoupling. The PCB should utilise both power and ground planes for best performance, connecting both planes to their respective regular PCB planes through a ferrite bead located as close as possible to the device. For best performance, a 100nF capacitor should be used to decouple the reference and supply pins. Decoupling should take place as close to the device as possible to reduce lead inductance. The digital inputs to the device should be isolated as much as possible from the analog outputs and other analog circuitry and should not overlay the analog ground and power planes.

To reduce noise pick-up, long clock lines to the device should be avoided. For best performance the analog output should have a 75Ω load connected to analog ground.

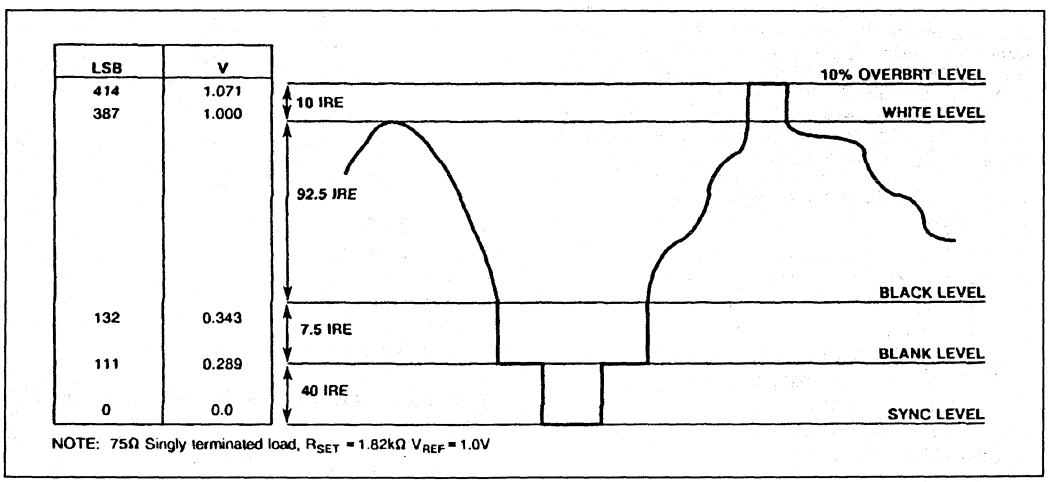


Fig.4 Composite video output waveform

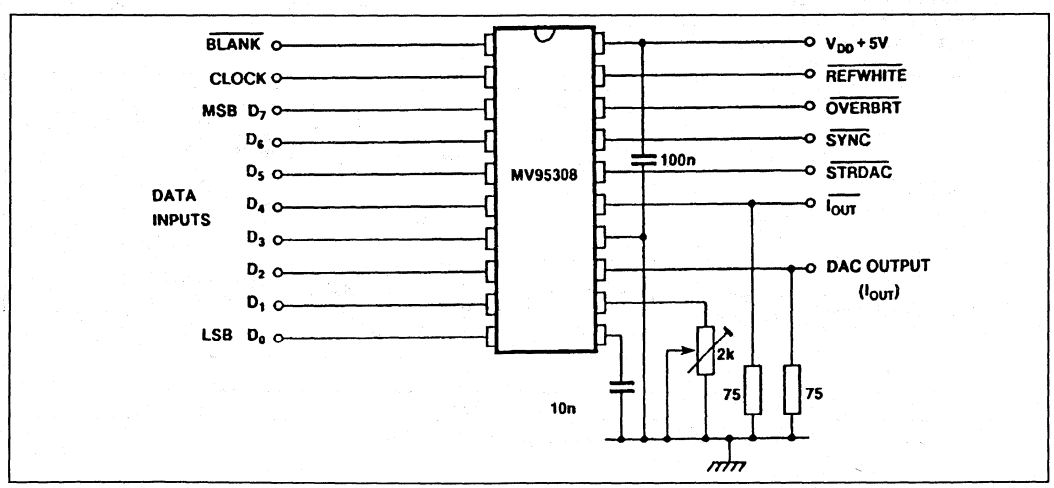


Fig.5 Applications/test board

DS2177-2.1

MV95408

50MHz 8-BIT CMOS VIDEO DAC

The MV95408 is a CMOS 8-bit, 50MHz Digital to Analog converter, designed for use in both video graphics and general digital television applications.

A very low external component count has been achieved by including the loop amplifier and reference voltage source on chip.

The device contains a data input register and registered video controls ($\overline{\text{BLANK}}$, $\overline{\text{REFWHITE}}$, $\overline{\text{OVERBRT}}$ and $\overline{\text{SYNC}}$). These control inputs and associated internal circuitry allows the MV95408 to be used in video graphics systems by providing the necessary video pedestal levels. The $\overline{\text{STRDAC}}$ input allows the video pedestals to be disabled in conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard RS-343A or RS-170 video levels, using the appropriate R_{SET} external resistor.

Pull up resistors have been added to tie all unused control inputs into their inactive (High) states.

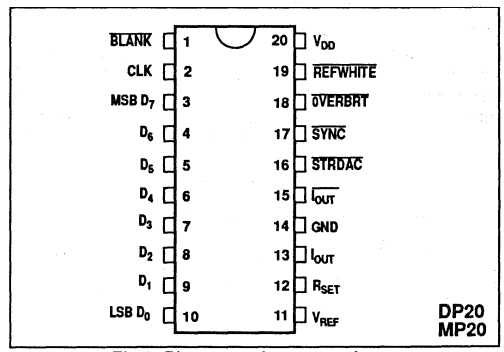


Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption (180mW Typ)
- 50MHz Pipeline Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Levels
- On Chip Reference Voltage Source
- Guaranteed Monotonic
- Drives 75Ω Loads Directly
- Single 5V Power Supply

APPLICATIONS

- Data Conversion (general)
- Computer Graphics
- Waveform Synthesis
- Commercial TV
- Instrumentation

ORDERING INFORMATION

MV95408 BDP (Industrial - Plastic DIL Package)
MV95408 BMP (Industrial - Miniature Plastic DIL Package)

ABSOLUTE MAXIMUM RATINGS (Reference to GND)

DC Supply Voltage, V_{DD}	-0.3 to +7V
Digital Input Voltage	-0.3 to V_{DD} +0.3V
Analog Output Short Circuit Duration	Indefinite
Ambient Operating Temperature	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C

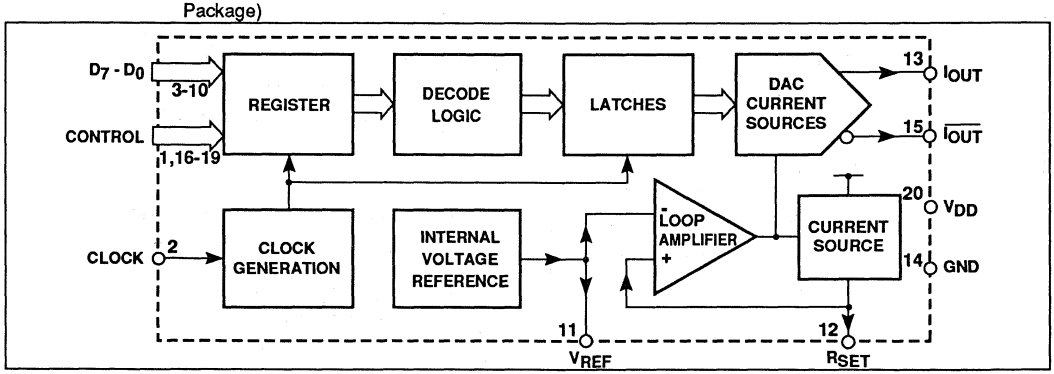


Fig.2 Block diagram of MV95408

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):
As specified in recommended operating conditions. Full temperature range = -40°C to +85°C

DC CHARACTERISTICS

Parameter	Symbol	Temp (°C)	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution		Full	8			Bits	
Integral linearity error	INL	25		±0.5		LSB	
		Full			±1	LSB	
Differential linearity error	DNL	25		±0.5		LSB	
		Full			±1	LSB	
Gain error		25		±1%	±5%	%	Of full scale
Analog output							
Grey scale current range		25		8.8		mA	75Ω singly terminated load R_{SET} = 1.8kΩ (graphics mode)
				255		LSB	
10% Over Bright level relative to White level		25	26	27	28	LSB	
				10		IRE	
White level relative to Blank level		25	275	276	277	LSB	
				100		IRE	
Black level relative to Blank level		25	20	21	22	LSB	
				7.5		IRE	
White level relative to Black level		25		255		LSB	
				92.5		IRE	
Blank level		25	107	111	115	LSB	
				40		IRE	
Sync level		25		0		LSB	
LSB size	LSB	25		2.58		mV	
Output compliance	V_{OC}	25	-0.3		+1.5	V	
Digital inputs							
High level I/P voltage	V_{IH}	25	3		V_{DD}+0.3	V	
Low level I/P voltage	V_{IL}	25	GND-0.3		1.2	V	
High level I/P current	I_{IH}	25			+1	µA	
Low level I/P current	I_{IL}	25			-1	µA	
Internal voltage reference (V_{REF})	V_{REF}	25	0.95	1.0	1.05	V	
		Full	0.90		1.10	V	
V_{REF} temperature coefficient				40		ppm/°C	

AC CHARACTERISTICS (Refer to Fig. 3)

Parameter	Symbol	Temp (°C)	Value Min.	Value Typ.	Value Max.	Units	Conditions
Max clock rate	f_{MAX}	Full	50			MHz	maximum guaranteed freq.
Clock high time	t_{CLKH}	25	7			ns	
Clock low time	t_{CLKL}	25	7			ns	
Data and control setup time	t_{SU}	25	6			ns	
Data and control hold time	t_H	25	2			ns	
Analog output delay	t_{DLY}	25		10		ns	
Analog output rise/fall time	t_{RF}	25		3	6	ns	
Analog output settling time	t_S	25		15		ns	
Glitch energy		25		100		pV-sec	
V_{DD} supply current	IDD	25		30		mA	fc = 15MHz
				42		mA	fc = 50MHz

THERMAL CHARACTERISTICS

Thermal Resistance	DP	MP	
Chip to case θ_{jC}	20	30	°C/W
Chip to ambient θ_{jA}	75	93	°C/W

RECOMMENDED OPERATING CONDITIONS

R_{LOAD} (I_{OUT} and $I_{\overline{OUT}}$)	75Ω
V_{DD}	5.0V ± 0.5V
R_{SET} (graphics applications)	1.8kΩ
R_{SET} (straight DAC applications)	1.2kΩ

CIRCUIT DESCRIPTION

As illustrated in the function block diagram, Fig. 2, the MV95408 contains an 8-bit D-to-A converter, input registers, a loop amplifier and voltage reference.

On the falling edge of each clock cycle, as shown in Fig. 3, eight data bits are latched into the device and passed to the 8-bit D-to-A converter. Also latched on the falling edge of the clock signal, the $\overline{SYNC}$ and $\overline{BLANK}$ inputs add the necessary weighted currents to the analog outputs to produce the required output levels for use in video applications. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$, $\overline{REFWHITE}$ and $\overline{OVERBRT}$ inputs modify the DAC output levels.

To obtain a high data throughput rate, the decoding logic of the MV95408 is fully pipelined. This introduces a one clock cycle delay between the latching of the input data and the resultant DAC output.

It also ensures synchronisation of the internal data and a minimal output glitch energy.

The DAC employed by the MV95408 eliminates the need for precision component ratios by using a segmented architecture in which equal weight bit currents are either routed to I_{OUT} or $\overline{I_{OUT}}$. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed.

The MV95408 eliminates the need for an external voltage reference by providing a nominally 1.0V reference on chip. An on-chip loop amplifier also provides stability of the full scale output current against power supply and temperature variations. The full scale output current is set by an external resistor R_{SET}. By adjustment of this value it is possible to implement RS-343A or RS-170 video levels as explained in the application notes.

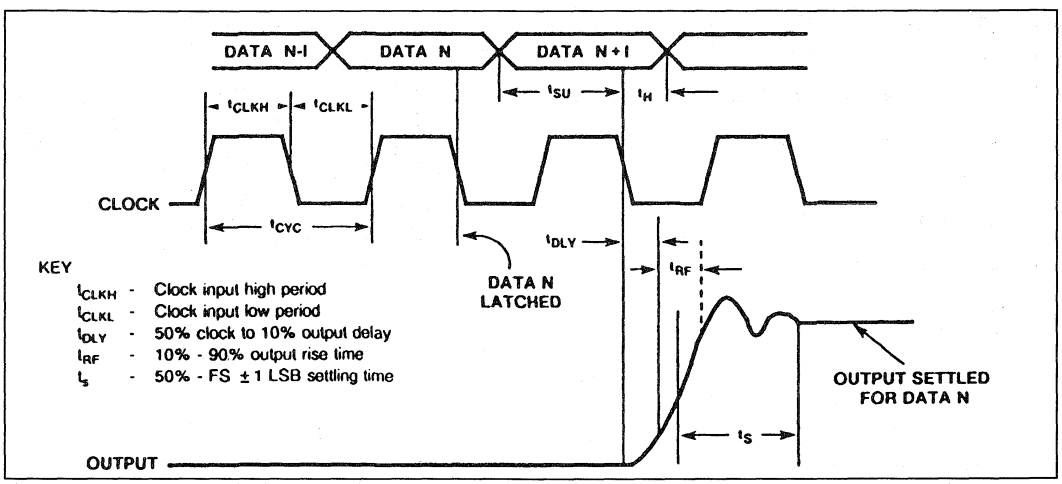


Fig.3 Timing diagram

Description	$\overline{STRDAC}$	$\overline{SYNC}$	$\overline{BLANK}$	$\overline{REFWHITE}$	$\overline{OVERBRT}$	OUTPUT DATA	I_{OUT} (LSB)
REFWHITE + 10%	1	1	1	0	0	X	414
REFWHITE	1	1	1	0	1	X	387
FULL WHITE	1	1	1	1	1	$FF	387
OVERBRIGHT	1	1	1	1	0	DATA	DATA + 132 + 27
FULL BLACK	1	1	1	1	1	$00	132
BLANK	1	1	0	X	X	X	111
DATA-SYNC	1	0	1	1	1	DATA	DATA + 21
SYNC	1	0	0	X	X	X	0
STRDAC MODE	0	X	1	1	X	DATA	DATA

Table 1: Video output truth table

Pin	Name	Description
2	CLK	**The clock input.** The falling edge of the clock latches the $\overline{\text{DATA}}$, $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$, $\overline{\text{OVERBRT}}$ and $\overline{\text{REFWHITE}}$ inputs into the logic pipeline. The decoded data will be latched into the DAC output 1 clock cycle later. The clock frequency determines the update rate of the DAC output.
3-10	D_7-D_0	**The data inputs.** D_0 is the least significant bit (LSB). The coding is in straight binary only.
13,15	I_{OUT}, $I_{\overline{OUT}}$	**The current output and its complement.** These are the high impedance current source outputs of the DAC capable of driving a 75Ω load up to a voltage of 1.5V.
14	GND	**Analog ground for the DAC.**
20	V_{DD}	**Analog power for the DAC**
11	V_{REF}	**The output of the internal voltage reference generator.** This output is nominally 1V, and should be decoupled with a 10nF capacitor.
12	R_{SET}	**The full scale adjust control.** The R_{SET} resistor is connected from this pin to ground. An internal loop amplifier adjusts a reference current flowing through the R_{SET} resistor so that the voltage across the resistor is equal to the V_{REF} voltage. This reference current has a weighting equal to 16 LSB's.
1	$\overline{\text{BLANK}}$	**The composite blank control input.** A logical zero on this input removes the Black pedestal from the I_{OUT} output, whilst forcing the internal data to the DAC to $00. This input is latched on the clock falling edge and will override the $\overline{\text{REFWHITE}}$ and $\overline{\text{OVERBRT}}$ inputs. The Black pedestal is 7.5 IRE units (actually 21 LSB's). If left open circuit this input is internally tied high.
17	$\overline{\text{SYNC}}$	**The composite sync control input.** A logical zero on this input removes the Blank pedestal from the I_{OUT} output. The Blank pedestal is nominally 40 IRE units (actually 111 LSB's). The $\overline{\text{SYNC}}$ input does not override any other control lines. This input is latched on the clock falling edge. If left open circuit this input is internally tied high.
19	$\overline{\text{REFWHITE}}$	**The reference white level control input.** A logical zero on this input overrides the input data, forcing the data to $FF. The $\overline{\text{BLANK}}$ input will override this input. If left open circuit this input is internally tied high.
18	$\overline{\text{OVERBRT}}$	**The 10% overbright control input.** A logical zero on this input switches the Overbright pedestal into the I_{OUT} output. The Overbright pedestal is 10 IRE units (actually 27 LSB's). This input does not override any other input. The $\overline{\text{BLANK}}$ input overrides this input. If left open circuit this input is internally tied high.
16	$\overline{\text{STRDAC}}$	**The straight DAC control input.** A logical zero on this input causes the Black, Blank and Overbright pedestals to be disabled, removing them from both I_{OUT} and $I_{\overline{OUT}}$. This allows the DAC contribution to the output to be extended to a full 1 Volt. To obtain this extra DAC range, it is necessary to reduce the R_{SET} resistor value, see application notes. The $\overline{\text{BLANK}}$ the $\overline{\text{REFWHITE}}$ inputs may still be used to force the input data to $00 or $FF respectively. With the $\overline{\text{STRDAC}}$ pin held low the output current can be calculated from: Output current = Data x 1 LSB Where 1 LSB= $\frac{V_{REF}}{16 \times R_{SET}}$ Full scale = 255 LSB V_{REF} = 1.0V typ. The exact value of 1 LSB must be calculated from the full scale output. If left open circuit this input is internally tied high and the device will be configured for video graphics. In this mode the output current can be calculated from: Output current = (DATA + 21 + 111) x 1 LSB V_{REF} = 1.0V typ.

APPLICATIONS INFORMATION

RS-343A and RS-170 Video Generation

For generation of RS-343A compatible video levels (see Fig.4) it is recommended that a singly terminated 75Ω load be used with an R_{SET} resistor value of approximately 1.82kΩ

Similarly for the generation of RS-170 video levels a singly terminated 75Ω load should be used but in association with an R_{SET} value of approximately 1.29kΩ to provide the increased voltage range.

Non-Video Applications

The MV95408 may be used in non-video applications as explained in the pin description for $\overline{STRDAC}$ mode.The relationship between R_{SET} and the full scale output current has been explained previously and for a singly terminated 75Ω load an R_{SET} resistor value of approximately 1.19kΩ should be used.

PCB LAYOUT CONSIDERATIONS

The PCB layout should provide low noise on the MV95408 power and ground lines by shielding the digital inputs and providing adequate decoupling. The PCB should utilise both power and ground planes for best performance, connecting both planes to their respective regular PCB planes through a ferrite bead located as close as possible to the device. For best performance, a 100nF capacitor should be used to decouple the reference and supply pins. Decoupling should take place as close to the device as possible to reduce lead inductance. The digital inputs to the device should be isolated as much as possible from the analog outputs and other analog circuitry and should not overlay the analog ground and power planes.

To reduce noise pick-up, long clock lines to the device should be avoided. For best performance the analog output should have a 75Ω load connected to analog ground.

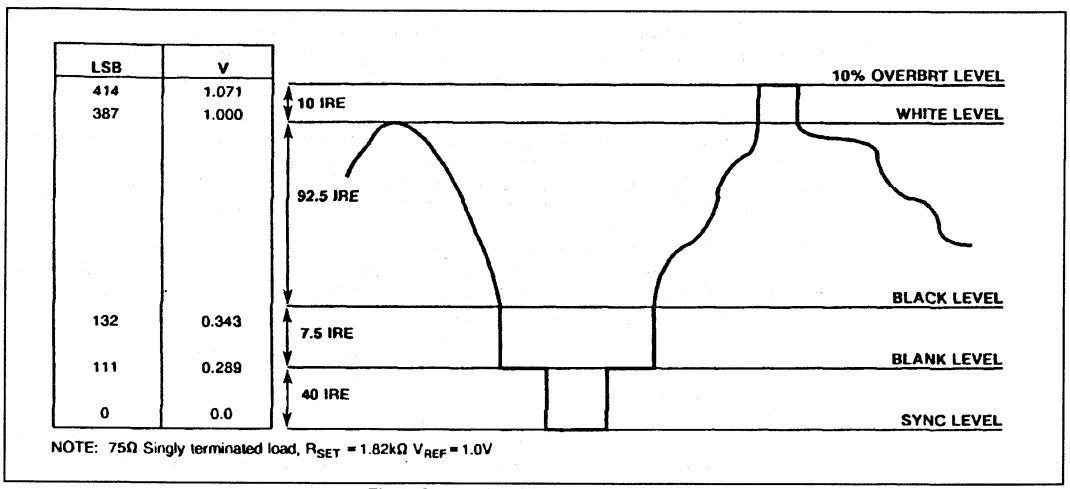


Fig.4 Composite video output waveform

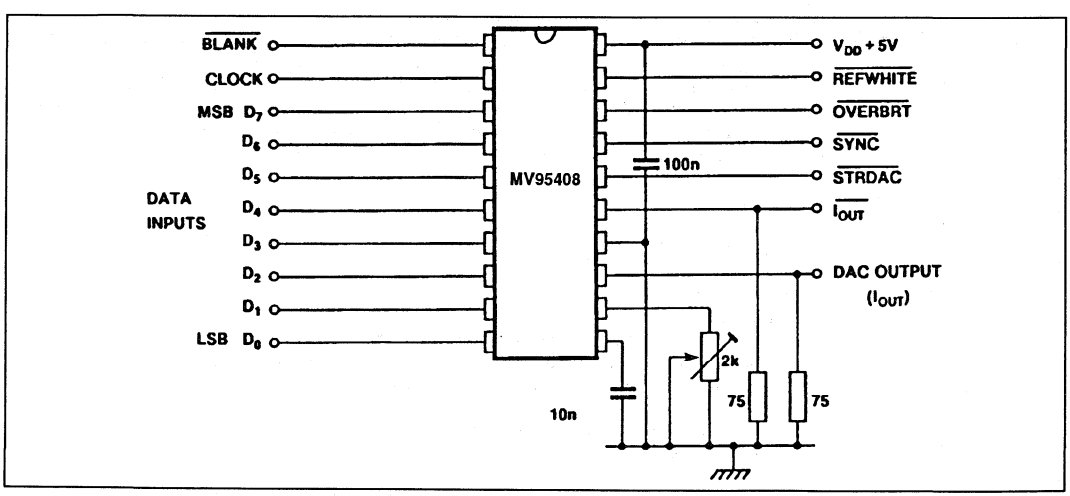


Fig.5 Applications/test board

DS2091-2.0

SP98608

8-BIT LATCHED 450MHz MULTIPLYING D-A CONVERTER

The SP98608 is an ECL 10K compatible 8-bit latched DAC. The 2.2nsec settling time allows a 450 megasample per second conversion rate. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP98608 design includes a high performance band-gap voltage reference and reference amplifier.

Both current and voltage multiplying modes are available. The input latch can be switched into transparent mode for applications that require low through delay.

FEATURES

- Latched Inputs
- 2.2ns Settling Time $^1/_2$ LSB Typically
- 8 Bits $\pm^1/_2$ LSB Integral and Differential Linearity
- Operating Temperature Range -40°C to +85°C
- ECL 10K Standard Inputs
- Complementary Current Outputs, 40mA Full Scale
- Reference Temperature Coefficient Typically <40ppm/°C
- Single -5.2V Supply

ORDERING INFORMATION

SP98608 BDG (Industrial - Ceramic DIL Package)

APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems
- ADC Evaluation

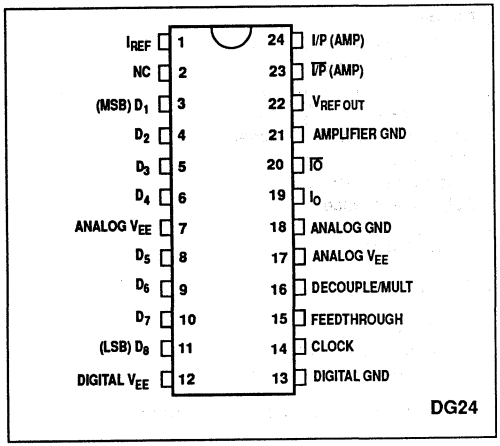


Fig.1 Pin connections - top view

ABSOLUTE MAXIMIM RATINGS

Supply Voltage,	-5.7V
Digital Input Voltage	-0 to -4.5V
Maximum R_{SET}	2.5kΩ
Output Reference Supply (V_L)	0 to +3V
Reference Input	±2V
Storage Temperature Range	-55°C to +150°C
Operating Junction Temperature	<175°C
Lead Temperature (soldering 60 sec)	300°C

THERMAL CHARACTERISTICS

θJC = 28°C/W
θJA = 90°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C; V_{EE} = -5.2V ± 5%; R_{SET} = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

Characteristic	Value Min.	Typ.	Max.	Unit	Conditions
Supply current I_{EE}		135	154	mA	all inputs at -1.8V
Digital inputs					
Input High voltage, V_{IH}	-0.96		-0.81	V	standard ECL
Input Low voltage, V_{IL}	-1.85		-1.65	V	10K compatible
Input High current, I_{IH}		115	200	µA	all inputs HI
Reference voltage V_{REF}		-1.280		V	
Reference voltage temp. coeff.		0	±80	ppm/°C	-30°C to +85°C
Output current - full scale	2		44	mA	R_{SET} 1.3kΩ to 85kΩ
Output current - full scale	38	42		mA	R_{SET} = 130Ω
Output compliance	-1.2		+1.0	V	T_{amb} = 25°C Note 3
	-1.0		+1.0	V	T_{amb} = 85°C Note 3
Bit size (LSB)	158	166	175	µA	current output R_{SET} = 130Ω
Resolution	8			Bits	
Accuracy					
Integral non-linearity			±0.5	LSB	
Differential non-linearity			±0.5	LSB	
Output dynamic parameters (see Note 1)					
Rise time t_r		600		ps	10 to 90%
Glitch energy (latched)		20		psV	mid-point
Glitch energy (transparent)		140		psV	transition
Noise output		-90	-83	dBm	see Note 2
Power supply rejection ratio (output WRT supply)	45	80		dB	±0.3V at 20kHz
Multiplying mode - voltage					
Multiplying input voltage range	-2		0	V	
Reference input resistance		10		kΩ	
Multiplying input bandwidth		30		MHz	-3dB
Transfer function non-linearity		0.2	1.0	dB	DC
Multiplying mode - current					
Multiplying input voltage range	1		15	mA	
Reference input resistance		400		Ohms	
Multiplying input bandwidth		300		MHz	-3dB
Transfer function non-linearity		1.0	3.0	%FS	DC

NOTES
1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. The output positive compliance can be increased beyond +1.0V at the expense of linearity. SEe Fig.4 for circuit configuration.
4. Analog and digital grounds should be connected together at the device pins.

Dynamic characteristic (Note 1)	Symbol	Value Min.	Typ.	Max.	Unit	Conditions
Update rate	F_{CLK}		450		MHz	
Latch setup time	t_s		0.9		ns	
Latch hold time	t_h	0			ns	
Settling time full scale	t_{st}		2		ns	1/2 LSB
Internal clock delay	t_c		500		ps	
Internal time to 10%	t_i		50		ps	

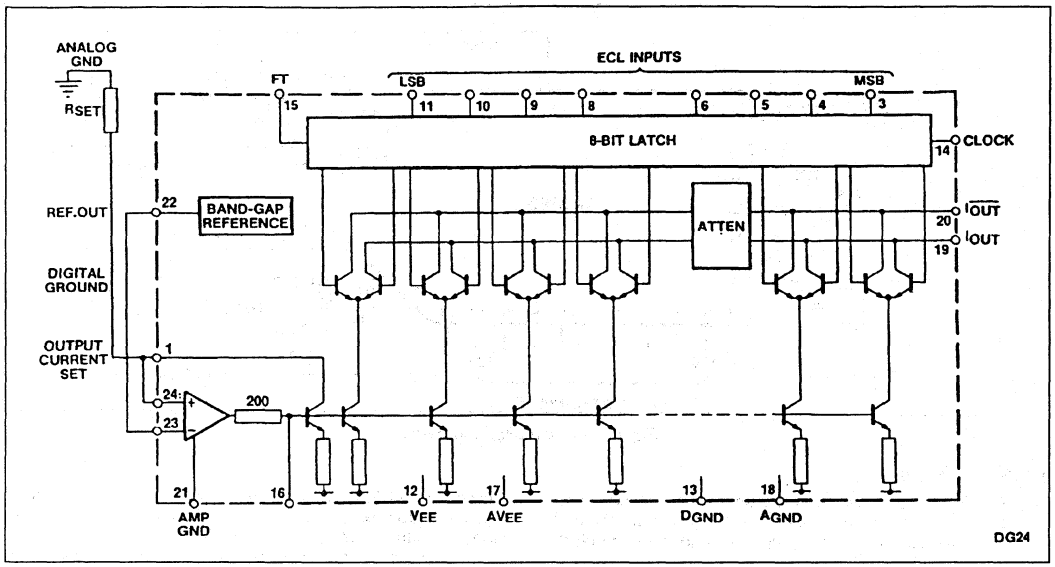


Fig.2 SP98608 block diagram

OPERATING NOTES

The pinout of the SP98608 is shown in Fig.1. External components are the current-setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 40mA, corresponding to a 1V drop across a 25Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current-setting resistor.

Output current, I_{OUT}, is given by:

$$I_{OUT} = \frac{1600}{400 + R_{LOAD}} \times \frac{V_{REF}}{R_{SET}} \text{ at full scale}$$

A complementary I_{OUT} is also provided. If single-ended output operation is employed, it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, R_{SET}, is typically 130Ω, giving a full-scale output current of 37mA and should have a temperature coefficient similar to that of the output load resistor.

Reference

The reference supply is internally compensated; however, to reduce the possibility of instability in some circuits, it has been bonded out to pin 16, it can therefore be decoupled to AV_{EE} if required.

Clock

The clock input is ECL 10K compatible. Data at the device inputs is acquired by the latch on the rising edge of the clock pulse.

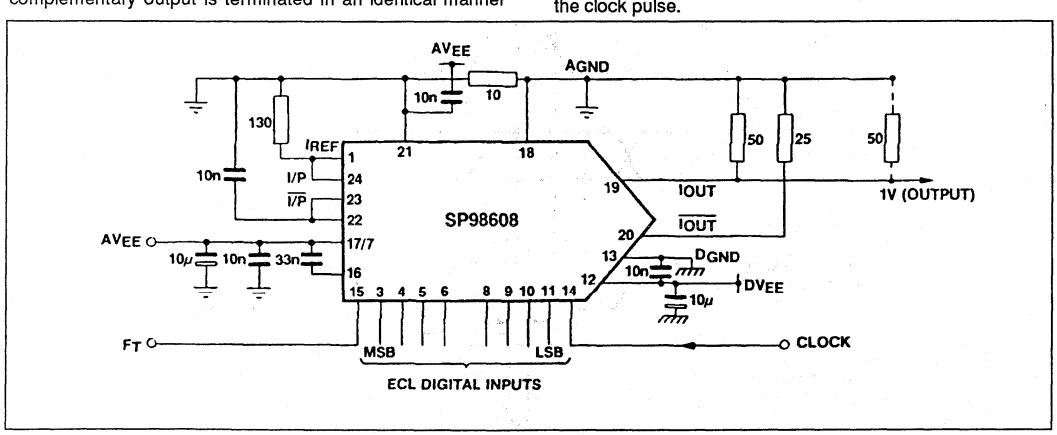


Fig.3 Test application circuit

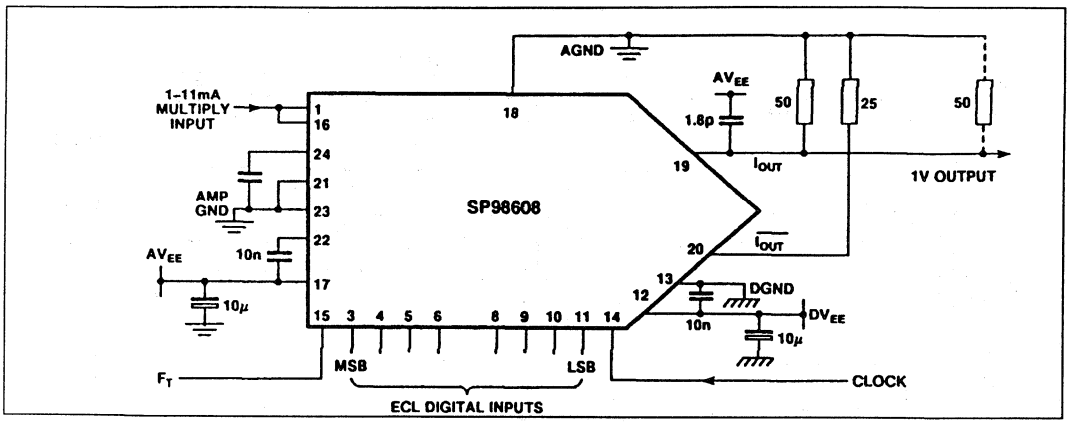


Fig.4 Current multiplying mode

F_T (Feedthrough)

The F_T input allows both transparent or latched data inputs. When open circuits this pin will self bias to -2V and the data will be retained by the input latch for one half clock cycle.

When the F_T input is connected to 0V the input latch will be transparent. In this mode, it is essential that the input data has low time skew (<100ps) to avoid output glitches.

Multiplying Mode

Multiplying operation of the DAC is available in two modes: either a voltage applied in place of the internal reference, or a current supplied via the current set pin.

Voltage Multiplying. The transfer function is approximately: I_{OUT} (Full Scale) = 4 x V_{IN}/R_{SET}. While this mode offers the best linearity of operation, the frequency response limitations mean that the maximum usable bandwidth is limited to approximately 50MHz.

Current Multiplying. A circuit for using the DAC in current multiplying mode is shown in Fig. 4. The transfer function is approximately; I_{OUT} (Full Scale) = 4 x I_{IN}. In this mode the current setting loop amplifier is not used.

The operational bandwidth of the current input to -3dB is at least 320MHz.

A 1V output is obtained into 25 ohm when a current of approximately 11mA is fed into pin 1 and the input code is selected for full output current.

Output Compliance

Using the SP98608 with a load resistor not referred to ground, allows a larger output swing than the conventional connection of Fig. 3. Connecting analog ground and the current-setting resistor R_{SET} to the load return supply ensures that the scale factor of the output is independent of the load.

Extending the compliance beyond +1V may cause slight degradation of linearity; +3V should be considered an absolute maximum.

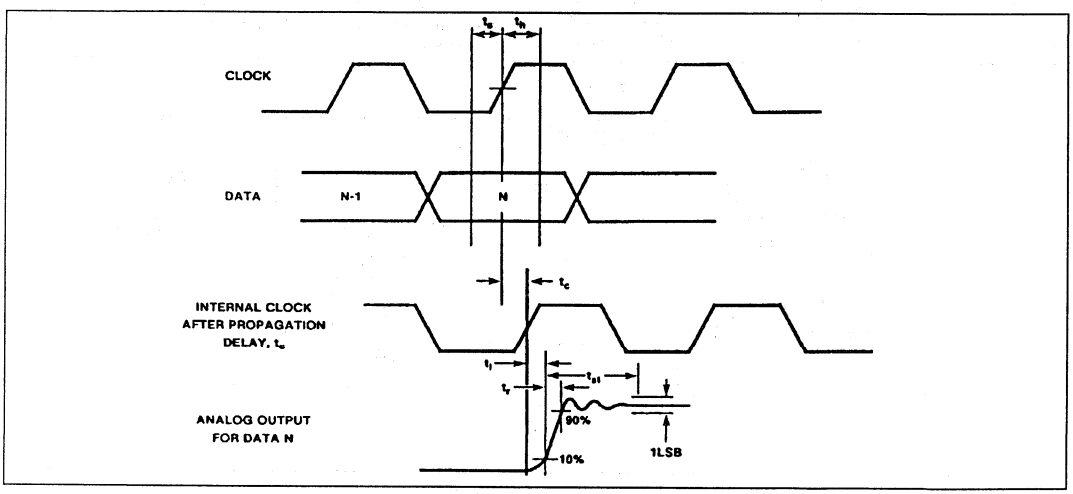


Fig.5 Timing diagram - latched mode

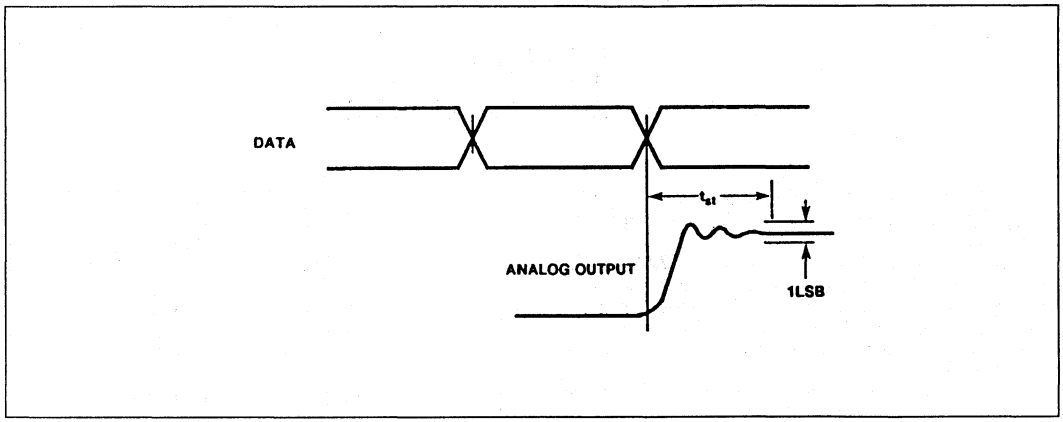


Fig.6 Timing diagram - transparent mode

DS3002-2.0

VP101

30/50MHz 8-BIT CMOS VIDEO DAC

The VP101 is a CMOS 8-bit video DAC designed for use in high performance, high resolution colour graphics applications.

The device uses video control inputs ($\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$ and REF WHITE) to provide the VP101 with the video pedestal levels required to generate RS-343A compatible video signals into a doubly-terminated 75Ω load, or alternatively to produce RS-170 video signals across a singly-terminated 75Ω load.

Data and control inputs are fully pipelined to maintain synchronisation between the DAC outputs.

The full scale output current is defined by a 1.2V reference and a single resistor. The reference voltage is included on-chip in the VP101, but may be supplied externally if required (see Fig. 2).

Differential and integral linearity errors of the D-A converters are guaranteed to be a maximum of ±1LSB over the full operating temperature range.

FEATURES

- 30/50MHz Pipeline Operation
- Triple 8-Bit D-A Converters
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Levels
- Drives Doubly Terminated 75Ω Load
- Single 5V Power Supply
- Typical Power Dissipation 500mW
- Direct Replacement for Bt101
- On-Chip Reference Available

APPLICATIONS

- High Resolution Colour Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

ORDERING INFORMATION

VP101-3 BA DP (Commercial - Plastic DIL Package)
VP101-3 BA HP (Commercial - J-lead Package)
VP101-5 BA DP (Commercial - Plastic DIL Package)
VP101-5 BA HP (Commercial - J-lead Package)
VP101-3 BA GP (Commercial - Plastic Leaded Chip Carrier, Gullwing formed leads)

ABSOLUTE MAXIMIM RATINGS (Referenced to AGND)

DC supply voltage (V_{AA})	-0.3 to +7V
Digital input voltage	-0.3 to V_{AA} +0.3V
Analog output short circuit duration	Indefinite
Ambient operating temperature	0°C to +70°C
Storage temperature range	-55°C to +125°C

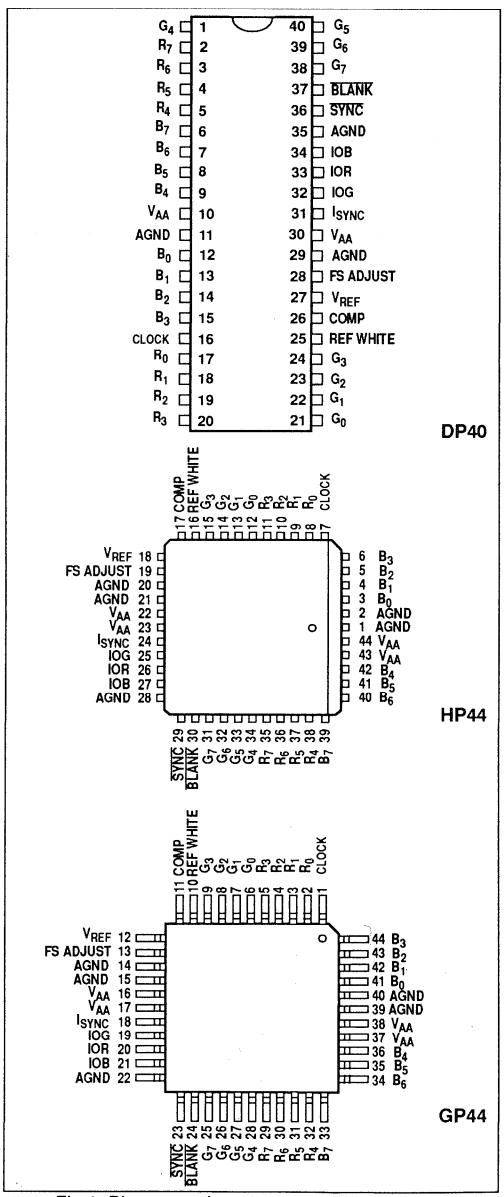


Fig.1 Pin connections (not to scale) - top view

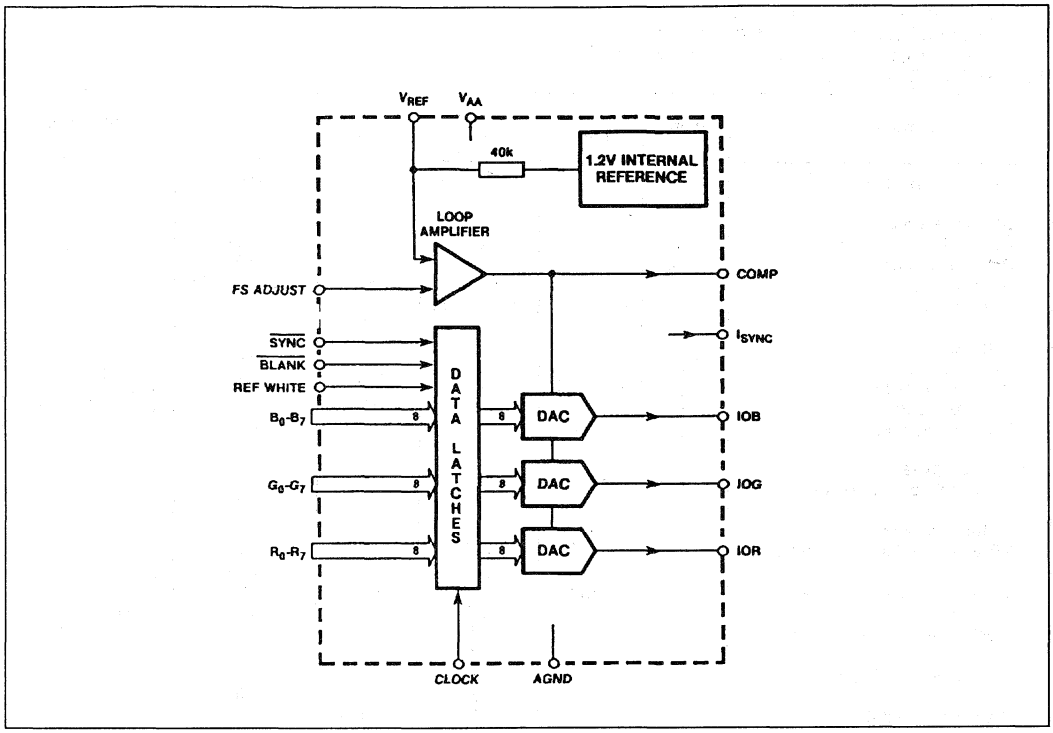


Fig.2 functional block diagram of VP101

RECOMENDED OPERATING CONDITIONS

Parameter	Symbol	Value Min.	Typ.	Max.	Units	Conditions
Supply voltage	V_{AA}	4.75	5.00	5.25	V	
Ambient operating temperature	T_{amb}	0		+70	°C	
Output load	R_L		37.5		Ω	for RS-343A compatible output levels
Reference voltage (internal or external)	V_{REF}	1.14	1.20	1.26	V	
FS ADJUST resistor	R_{SET}		542		Ω	

THERMAL CHARACTERISTICS

	DP	HP	GP	
Thermal resistance, chip-to-case θ_{jc} =	12	17	17	°C/W
Thermal resistance, chip-to-ambient θ_{jc} =	45	50	50	°C/W

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in recommended operating conditions.

DC CHARACTERISTICS

Parameter	Symbol	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution (each DAC)		8			Bits	
Accuracy (each DAC)						
Integral linearity error	INL		±0.3	±1	LSB	
Differential linearity error	DNL		±0.3	±1	LSB	
Grey scale error			±1%	±5%	% grey scale	
Monotonicity			guaranteed			
Digital inputs						
Input high voltage	V_{IH}	3.0		V_{AA}+0.3	V	binary coding
Input low voltage	V_{IL}	AGND-0.3		12	V	
Input high current	I_{IH}			+1	µA	
Input low current	I_{IL}			-1	µA	
Analog outputs						
Grey scale current range		15		20	mA	RS-343A tolerances assumed
			255		LSB	
Output currents						
White level relative to blank level		17.69	19.06	20.40	mA	
			276		LSB	
White level relative to black level		16.74	17.62	18.50	mA	
			255		LSB	
Black level relative to blank level		0.95	1.44	1.90	mA	
			21		LSB	
Blank level on IOR, IOB		0	5	50	mA	
			0		LSB	
Blank level on IOG		6.29	7.62	8.96	mA	
			111		LSB	
Sync level on IOG		0	5	50	µA	
					LSB	
LSB size	LSB		69.1		µA	
DAC to DAC matching			2		%	
Output compliance	V_{OC}	-0.5		+1.4	V	
External V_{REF} input current	I_{REF}			10	µA	
Internal voltage reference	V_{REF}	1.14	1.20	1.26	V	
Internal V_{REF} temperature coefficient			40		ppm/°C	

AC CHARACTERISTICS

Parameter	Symbol	VP101-5 Min.	VP101-5 Typ.	VP101-5 Max.	VP101-3 Min.	VP101-3 Typ.	VP101-3 Max.	Units	Conditions
Max clock rate	f_{max}	50			30			MHz	
Data and control setup time	t_{SU}	6			8			ns	
Data and control hold time	t_H	2			2			ns	
Clock cycle time	t_{CYC}	20			33.3			ns	
Clock pulse width high time	t_{CLKH}	8			10			ns	
Clock pulse width low time	t_{CLKL}	8			10			ns	
Analog output delay	t_{DLY}		10			10		ns	
Analog output rise/fall time	t_{VRF}			8			9	ns	
Analog output settling time	t_S		12			15		ns	
Glitch energy			100			100		pV-sec	
Analog output skew			0	3		0	3	ns	
Pipeline delay		1	1	1	1	1	1	Clock	
V_{AA} supply current	I_{AA}		120	175		100	140	mA	at f_{max}, V_{AA} = 5V

CIRCUIT DESCRIPTION

As shown in the Fig. 2, the VP101 contains three 8-bit D-A converters, input latches, and a loop amplifier.

On the rising edge of each clock cycle, (see Fig. 4), 24 bits of colour information (R_0-R_7, G_0-G_7, and B_0-B_7) are latched into the device and presented to the three 8-bit D-A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, and will force the inputs of each D-A converter to $FF.

$\overline{SYNC}$ and $\overline{BLANK}$ are latched on the rising edge of the clock to maintain synchronisation with the colour data. These inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as shown in Fig. 3. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$, and REFWHITE inputs modify the output levels.

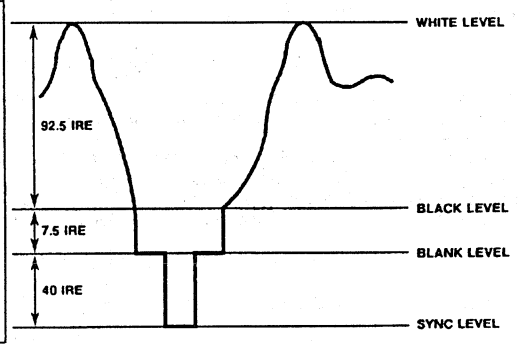
The I_{SYNC} current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If I_{SYNC} is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG and IOB outputs will have the same full scale output current.

Full Scale output current is set by an external resistor (R_{SET}) between the FS ADJUST pin and AGND. R_{SET} has a typical value of 542Ω for generation of RS-343A video into a 37.5Ω load. The VP101 may be used in applications where an external 1.2V (typical) reference is provided, in which case the external reference should be temperature compensated and provide a low impedance output.

The D-A converters on the VP101 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme.This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch energy are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilises the full scale output current against temperature and power supply variations.

The analog outputs of the VP101 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω co-axial cable or interpolation filters.

Red/Blue		Green	
mA	V	mA	V
19.06	0.714	26.68	1.000
1.44	0.054	9.06	0.340
0.00	0.000	7.62	0.286
		0.000	0.000



NOTE : 75Ω doubly terminated load, R_{SET} = 542Ω, V_{REF} = 1.2V, I_{SYNC} connected to IOG, RS-343A levels assumed

Fig.3 Composite video output waveform

Description	IOG (mA)	IOR/IOB (mA)	REF WHITE	$\overline{SYNC}$	$\overline{BLANK}$	DAC I/P Data
White Level	26.68	19.06	1	1	1	$XX
White Level	26.68	19.06	0	1	1	$FF
Data	Data + 9.06	Data + 1.44	0	1	1	Data
Data-Sync	Data + 1.44	Data + 1.44	0	0	1	Data
Blank Level	9.06	1.44	0	1	1	$00
Blank-Sync	1.44	1.44	0	0	1	$00
Blank Level	7.62	0	X	1	0	$XX
Sync Level	0	0	X	0	0	$XX

NOTE: Typical with full scale IOG = 26.68mA, R_{SET} = 542Ω, V_{REF} = 1.2V, I_{SYNC} connected to IOG

Table 1: Video output truth table

Pin name	Description
$\overline{\text{BLANK}}$	Composite blank control input. A logic '0' forces the IOR, IOG and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logic zero, the R_0-R_7, G_0-G_7, B_0-B_7, and REF WHITE inputs are ignored.
$\overline{\text{SYNC}}$	Composite sync control input. A logic '0' on this input switches off a 40 IRE current source on the I_{SYNC} output. $\overline{\text{SYNC}}$ does not override any other control or data input as shown in Table 1; therefore it should be asserted only during the blanking interval. It is latched to the rising edge of CLOCK.
REF WHITE	Reference white level control input. A logic '1' on this input forces the IOR, IOG and IOB outputs to the white level, regardless of the R_0-R_7, G_0-G_7 and B_0-B_7 inputs. It is latched on the rising edge of CLOCK. See table 1.
R_0-R_7 G_0-G_7 B_0-B_7	Red, Green, and Blue data inputs. R_0, G_0, and B_0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input. The rising edge of CLOCK latches the R_0-R_7, G_0-G_7 and B_0-B_7 $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and REFWHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated CMOS buffer.
IOR,IOG, IOB	Red, Green, and Blue current outputs. these high impedance current sources are capable of directly driving a doubly terminated 75Ω co-axial cable. All outputs, whether used or not, should have the same output load (Note: A DC path to ground must be maintained).
I_{SYNC}	Sync current output. Typically this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logic '0' on the $\overline{\text{SYNC}}$ input results in no current being output to this pin, while logic '1' results in the following current being output: $I_{SYNC}\ (mA) = 3468\ X \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 111\ LSBs$ If sync information is not required on the green channel, this output may be connected to V_{AA} and the $\overline{\text{SYNC}}$ input tied high, causing the I_{SYNC} current source to be turned off, reducing the power consumption.
FS ADJUST	Full scale adjust control. A resistor (R_{SET}) connected between this pin and AGND controls the magnitude of the full video signal (Fig. 3). The current flowing in the R_{SET} resistor is equal to 32 LSBs. note that the IRE relationships in Fig. 3 are maintained, regardless of the full scale output current. The relationship between R_{SET} and full scale current on IOG (assuming I_{SYNC} is connected to IOG) is: $IOG\ (mA) = 12082\ X \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 387\ LSBs$ The full scale output current on IOR, IOB (mA) for a given R_{SET} is defined as: $IOR,\ IOB\ (mA) = 8624\ X \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 276\ LSBs$
COMP	Compensation pin. This pin provides compensation for the internal loop amplifier. A 0.01µF ceramic capacitor must be connected between this pin and the nearest V_{AA} pin. Connecting the capacitor to V_{AA} rather than to the AGND provides the highest possible power supply noise rejection.
V_{REF}	Voltage reference output. The output from an internal reference circuit, providing 1.2V (typical) reference.A 0.1µF ceramic capacitor must be used to decouple this output to V_{AA}.
AGND	Analog ground. All AGND pins must be connected.
V_{AA}	Analog power. All V_{AA} pins must be connected.

APPLICATION NOTES

RS-343A and RS-170 Video Generation

For generation of RS-343A compatible video levels it is recommended that a doubly terminated 75Ω load be used with an R_{SET} resistor value of approximately 542Ω

Similarly for generation of RS-170-compatible video, it is recommended that a singly terminated 75Ω load be used with an R_{SET} value of about 774Ω. If the VP101 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads.t

If driving a large capacitive load (load RC >1/20Πf_c) it is recommended that an output buffer with unloaded gain >2 be used to drive a doubly terminated 75Ω load.

COMP Resistor

To optimise the settling time of the VP101, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

Non-Video Applications

The VP101 may be used in non-video applications by disabling the video specific control inputs. REF WHITE should be a logic '0' while $\overline{BLANC}$ and $\overline{SYNC}$ should be a logic '1'. I_{SYNC} should be connected to V_{AA} or AGND. All three outputs will have the same full scale output current.

The relationship between R_{SET} and full scale output current (I_{OUT}) in this configuration is as follows:

$$I_{out}\,(mA) = 7968 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 255\ LSBs$$

$$\text{Note that 1 LSB} \equiv \frac{V_{REF}\,(V)}{32 \times R_{SET}\,(\Omega)}$$

With the data inputs at $00, there is a DC offset current (I_{min}) defined as follows:

$$I_{min}\,(mA) = 656 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 21\ LSBs$$

Therefore the total full scale output current will be $I_{OUT} + I_{min}$. The REF WHITE input may optionally be used as a 'force to full scale' control.

TIMING WAVEFORMS

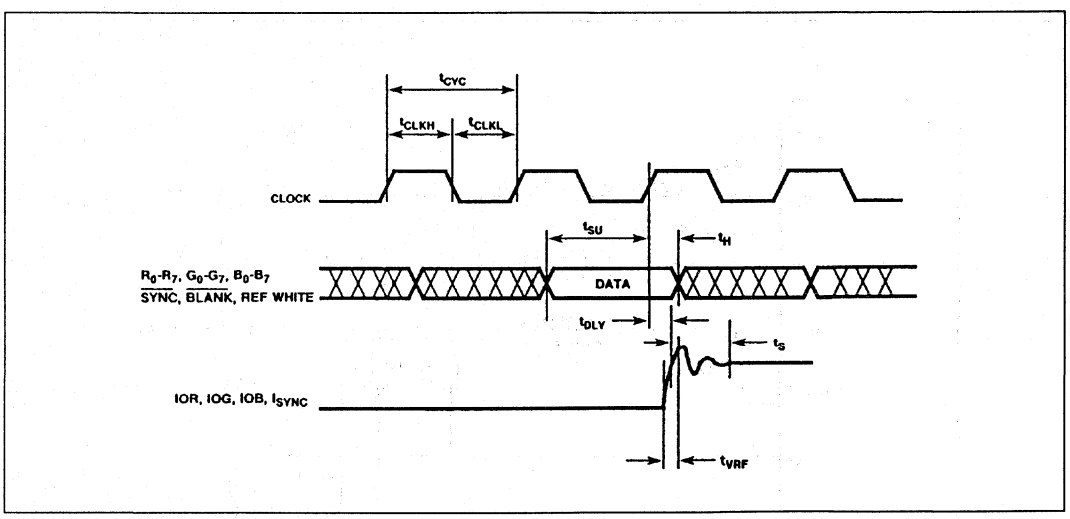


Fig.4 Input/output timing

NOTES

1. Output delay, t_{DLY}, measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
2. Settling time, t_s, measured from the 50% point of full scale transition to the output remaining within ± 1 LSB.
3. Output rise/fall time, t_{VRF}, measured between the 10% and 90% points of full scale transition.

PCB LAYOUT CONSIDERATIONS

To obtain the optimum performance from the VP101 great care must be taken in the PCB layout to ensure low noise power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling.

Power and Ground Planes

The VP101 and its associated circuitry should have its own power/ground planes connected at a single point through a ferrite bead. It is important that the regular PCB and ground planes do not overlay any portions of the analog power or ground planes to minimise plane-to-plane noise coupling.

Digital Signal Interconnect

The digital signal lines to the VP101 should be isolated as much as possible from the analog circuitry. Due to the high clock rates used, the clock lines to the VP101 should be as short as possible to minimise noise pickup.

Any pull-up resistors used on the inputs should be connected to the regular PCB power plane, not to the analog power plane.

Supply Decoupling

Noise on the analog power plane will be further reduced by the use of multiple decoupling capacitors (See Fig. 5).

Optimum performance is obtained with 0.1µF chip ceramic capacitors placed as close as possible to the V_{AA} pins, with the shortest leads possible to reduce lead inductance.

It should be noted that while the loop amplifier circuitry of the VP101 will reject power supply noise, this rejection decreases with frequency. Any high frequency noise on the regular supply (such as produced by a switch mode power supplies) must be adequately suppressed, else the designer should consider using a three terminal regulator to supply the analog power plane.

Analog Signal Interconnect

For optimum performance the analog output connectors and source termination resistors should be as close as possible to the VP101 to minimise noise pickup and reflections due to impedance mismatch. The video out signals should overlay the ground plane and not the analog power plane, to maximise the high frequency power supply rejection.

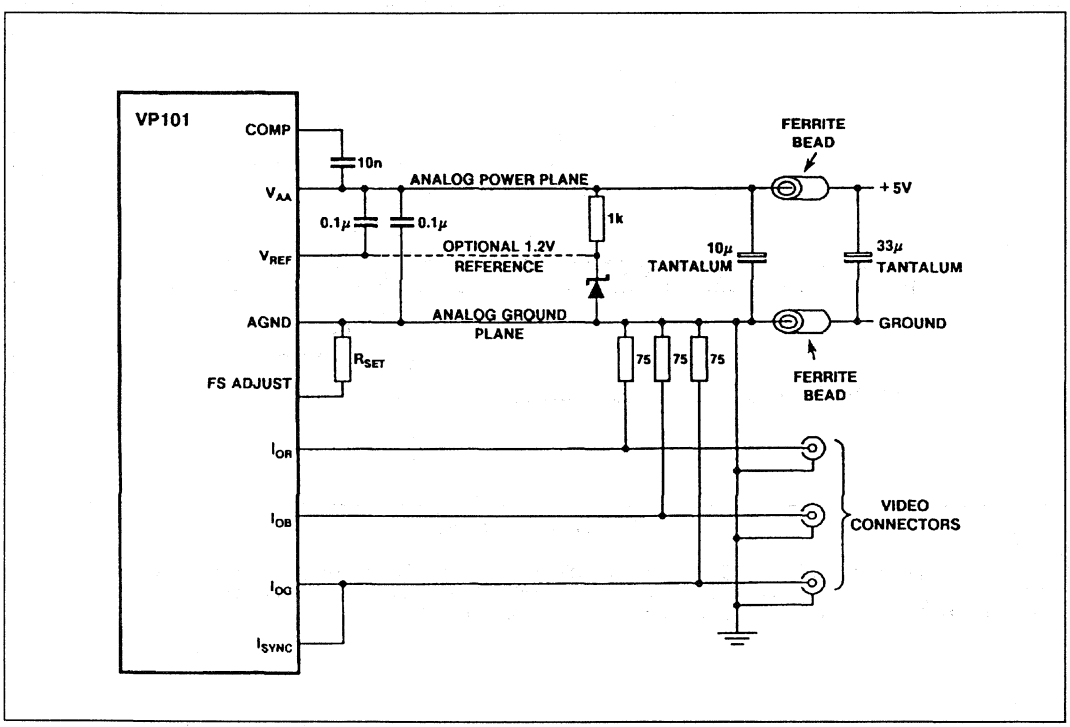


Fig.5 VP101 typical connections

Section 2
Advanced Function DACs

DS3005-2.1

ZN425E8

8-BIT D-A/A-D CONVERTER

The ZN425 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and in addition a counter and a 2.5V precision voltage reference. The counter is a powerful addition which allows a precision staircase to be generated very simply by clocking the counter.

FEATURES

- ±1/2 LSB Linearity Error
- 0°C to +70°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time (D-A) 1µs Typical
- Conversion Time (A-D) 1ms Typical, using Ramp and Compare Technique
- Extra Components Required
  D-A: Reference Capacitor (Direct Voltage Output through 10kOhms Typ.)
  A-D: Comparator, Gate, Clock and Reference Capacitor

ORDERING INFORMATION

Ambient operating temperature 0°C to +70°C
PackageDP16

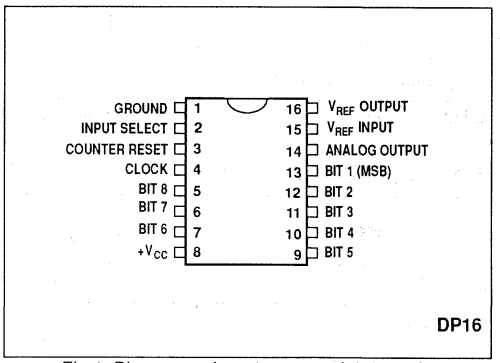


Fig.1 Pin connections (not to scale) - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs	+5.5V See note 3
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

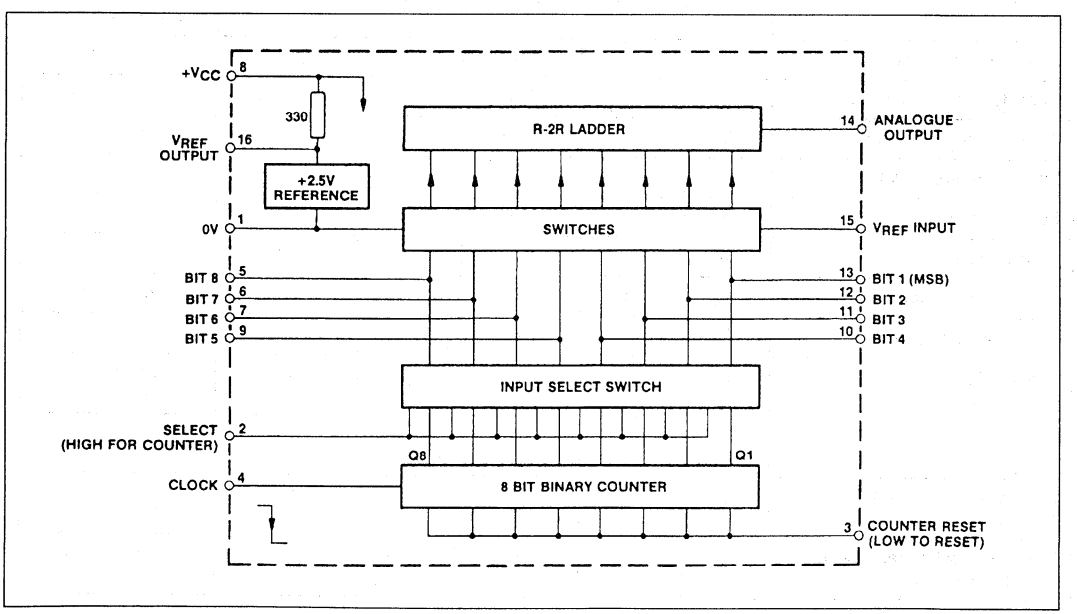


Fig.2 System diagram

ELECTRICAL CHARACTERISTICS

(at T_{amb} = 25°C and V_{CC} = +5V unless otherwise stated)

INTERNAL VOLTAGE REFERENCE

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output voltage	V_{REF}	2.4	2.55	2.7	V	I = 7.5mA (internal)
Slope resistance	R_S	-	2	4	Ω	I = 7.5mA (internal)
V_{REF} temperature coefficient		-	40	-	ppm/°C	I = 7.5mA (internal)

NOTE: The internal reference requires a 0.22μF stabilising capacitor between pins 1 and 16.

8-BIT D-A CONVERTER AND COUNTER

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolution		8	-	-	bits	
Non-linearity		-	-	±0.5	LSB	see note 3
Differential non-linearity		-	±0.5	-	LSB	see note 6
Settling time		-	1.0	-	μs	1LSB step
Settling time to 0.5LSB		-	1.5	2.5	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN425E8	V_{OS}	-	3	8	mV	All bits OFF See note 3
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. V_{REF} = 2.56V
Full-scale temp. coefficient		-	3	-	ppm/°C	Ext. V_{REF} = 2.56V
Linearity error temp.coeff.		-	7.5	-	ppm/°C	relative to F.S.R.
Analog output resistance	R_O	-	10	-	kΩ	
External reference voltage		0	-	3.0	V	
Supply voltage	V_{CC}	4.5	-	5.5	V	See note 3
Supply current	I_S	-	25	35	mA	
High level input voltage	V_{IH}	2.0	-	-	V	See notes 1 and 2
Low level input voltage	V_{IL}	-	-	0.7	V	
High level input current	I_{IH}	-	-	10	μA	V_{CC} = max. V_I = 2.4V
		-	-	100	μA	V_{CC} = max. V_I = 5.5V
Low level input current bit inputs	I_{IL}	-	-	-6.8	mA	V_{CC} = max. V_I = 0.3V
Low level input current, clock reset and input select	I_L	-	-	-0.18	mA	

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High level output current	I_{OH}	-	-	-40	µA	
Low level output current	I_{OL}	-	-	1.6	mA	
High level output voltage	V_{OH}	2.4	-	-	V	V_{CC} = min. Q = 1 I_{load} = -40µA
Low level output voltage	V_{OL}	-	-	0.4	V	V_{CC} = min. Q = 0 I_{load} = 1.6mA
Maximum counter clock frequency	f_c	3	5	-	MHz	See note 5
Reset pulse width	t_R	200	-	-	ns	See note 4

NOTES:
1. The input select pin (2) must be held low when bit pins (5, 6, 7, 9, 10,11,12, and 13) are driven externally.
2. To obtain counter outputs on bit pins the select pin (2) should be taken to $+V_{CC}$ via a 1kΩ resistor.
3. (a) Maximum operating voltage. Between 70°C and 125°C the maximum supply voltage is reduced to 5.0V.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
4. The device may be reset by gating from its own counter.
5. F_{max} in A-D mode is 300kHz, see Operating Note 2.
6. Monotonic over full operating temperature range.

INTRODUCTION

The ZN425 is an 8-bit dual mode D-A/A-D converter. It contains an 8-bit D-A converter using an advanced design of R-2R ladder network and an array of precision bipolar switches plus an 8-bit binary counter and a 2.5V precision voltage reference all on a single monolithic chip.

The special design of the ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip voltage reference is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including an 8-bit binary counter on the chip, A-D conversion can be obtained simply by adding an external comparator (LM311) and clock inhibit gating (7400).

By simply clocking the counter the ZN425 can be used as a self-contained precision ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig.3.

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

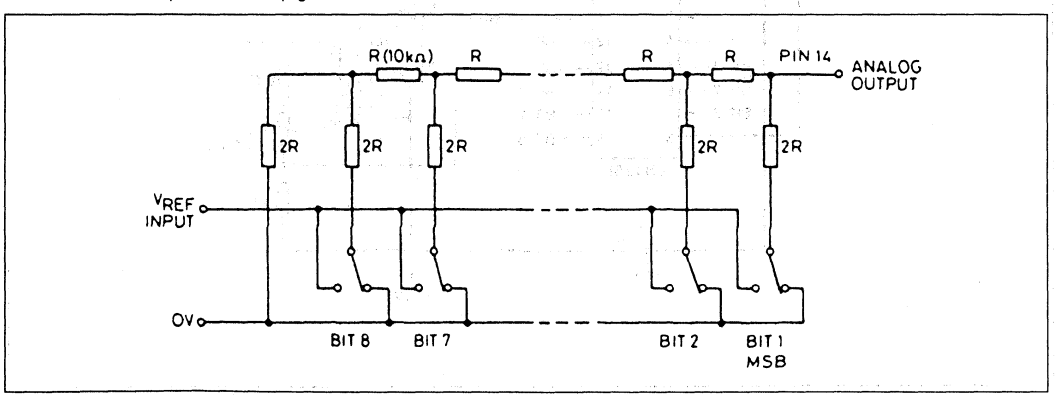


Fig.3 The R-2R ladder network

If pin 2 is high then the output equals the Q output of the corresponding counter.

If pin 2 is low then the output transistor, Tr1 is held off.

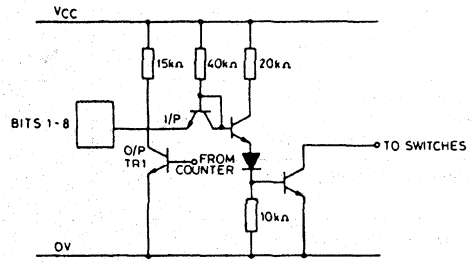


Fig.4 Bit inputs/outputs

OPERATING NOTES

1. 8-bit D-A Converter

The ZN425 gives an analog voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the analog output resistance R_O, will be less than 0.004% per °C (or 1LSB/100°C) if R_L is chosen to be ≥ 650kΩ.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig.5 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{OUT} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{OUT} = Nominal full-scale reading - 1LSB

iii. Repeat i. and ii.

e.g. Set F.S.R. to + 3.840V - 1LSB
=3.825V

$$(1LSB = \frac{3.84}{256} = 15.0mV)$$

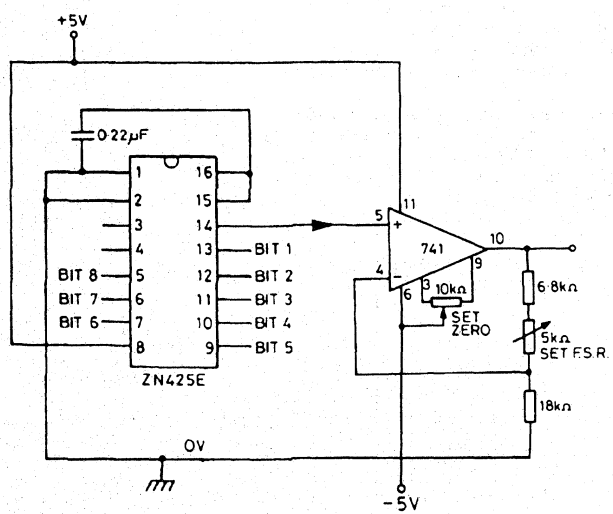


Fig.5 8-bit D-A converter

2. 8-bit A-D Converter

A counter type ADC can be constructed by adding a voltage comparator and a latch as in Fig.6. On the negative edge of the CONVERT COMMAND pulse (15µs minimum) the counter is set to zero and the STATUS latch to logical 1.On the positive edge the gate is opened, enabling clock pulses to be fed to the counter input of the ZN425. The minimum negative clock pulse width of the ZN425 is 100ns. The analog output of the ZN425 ramps until it equals the voltage on the other input of the comparator. At this point the comparator output goes low and resets the STATUS to inhibit further clock pulses. The logical 0 from the status latch indicates that the 8-bit digital output is a valid representation of the analog input voltage.

A small capacitor of 47pF is added to the ZN425 output to stop any positive going glitches prematurely resetting the status latch. This capacitance is in parallel with the ZN425 output capacitance (20-30pF) and they form a time constant with the ZN425 output resistance (10kΩ). This time constant is the main limit to the maximum clock frequency. With a fast comparator the clock frequency can be up to 300kHz. The conversion time varies with the input being a maximum for full-scale input.

Maximum conversion time =

$$\frac{256}{\text{clock frequency in Hz}} \text{ seconds}$$

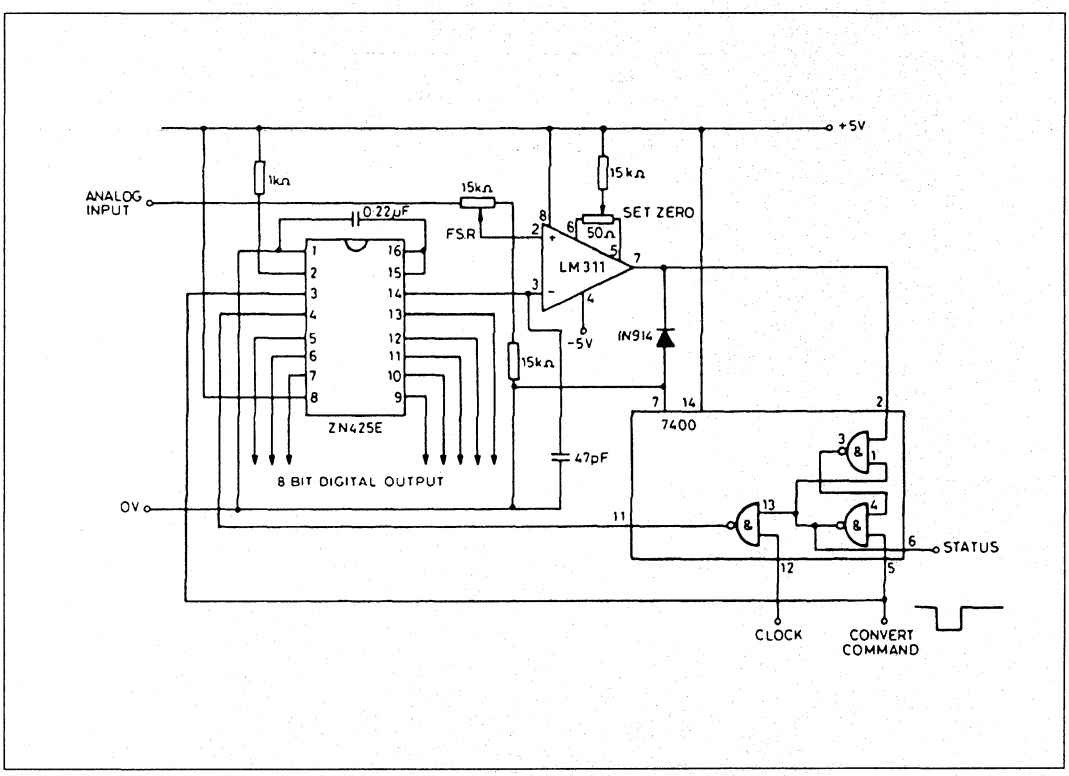


Fig.6 8-bit A-D converter

3. Precision Ramp generator

The inclusion of an 8-bit binary counter on the chip gives the ZN425 a useful ramp generator function. The circuit, Fig. 7, uses the same buffer stages as the D-A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14.

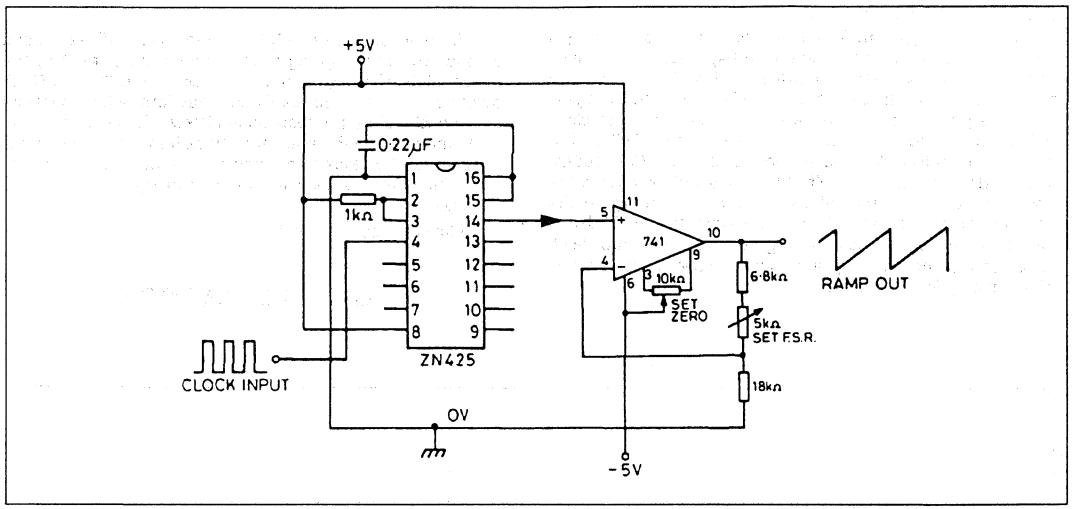


Fig.7 Precision ramp generator

DS3021-2.2

ZN426E8

8-BIT D-A CONVERTER

The ZN426 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and a 2.5V precision voltage reference.

FEATURES

- ±1/2 LSB Linearity Error
- Guaranteed Monolithic over the Full Operating Temperature Range
- 0°C to +70°C
- TTL and 5V CMOS Compatible
- Single 5V Supply
- Settling Time 1 microsecond Typical
- Only Reference Capacitor and Resistor Required

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7.0V
Max.voltage, logic and V_{REF} inputs	+5.5V
Operating temperature range	0°C to +70°C
Storage temperature range	-55°C to +125°C

ORDERING INFORMATION

Ambient operating temperature	0°C to +70°C
Package, ZN426E8	DP14

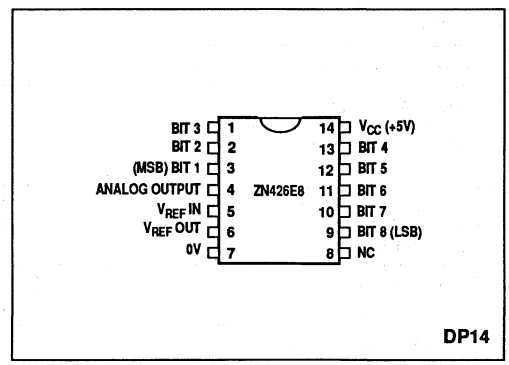


Fig.1 Pin connections (not to scale) - top view

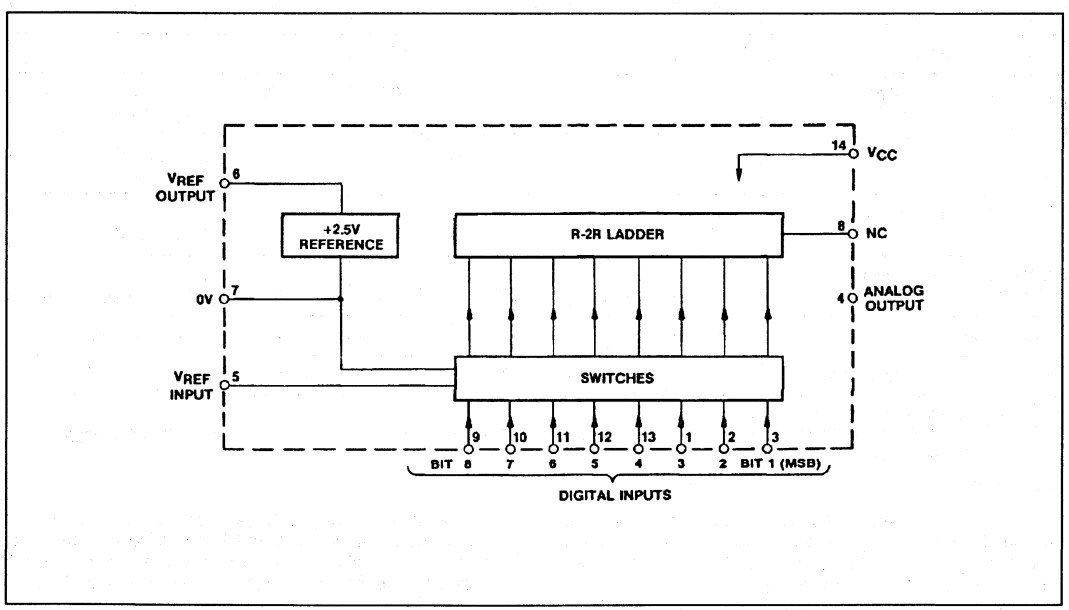


Fig.2 System diagram

ELECTRICAL CHARACTERISTICS

(at T_{amb} = 25°C and V_{CC} = +5V unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	-	-	bits	
Non-linearity		-	-	±0.5	LSB	
Differential non-linearity		-	±0.5	-	LSB	Note 1
Settling time to 0.5LSB		-	1.0	-	µs	1LSB step
Settling time to 0.5LSB		-	2.0	-	µs	All bits ON to OFF or OFF to ON
Offset voltage ZN426E8 and D	V_{OS}	-	3.0	5.0	mV	All bits OFF
V_{OS} temperature coefficient		-	5	-	µV/°C	
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. V_{REF} = 2.560V
Full-scale temp. coefficient		-	3	-	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coefficient		-	7.5	-	ppm/°C	Relative to F.S.R.
Analog output resistance	R_O	-	10	-	kΩ	
External reference voltage		0	-	3.0	V	
Supply voltage	V_{CC}	4.5	-	5.5	V	
Supply current	I_S	-	5	9	mA	
High level input voltage	V_{IH}	2.0	-	-	V	
Low level input voltage	V_{IL}	-	-	0.7	V	
High level input current	I_{IH}	-	-	10	µA	V_{CC} = max. V_I = 2.4V
		-	-	100	µA	V_{CC} = max. V_I = 5.5V
Low level input current	I_{IL}	-	-	-0.18	mA	V_{CC} = max. V_I = 0.3V
Internal voltage reference Output voltage	V_{REF}	2.475	2.55	2.626	V	Note 2 R_{REF} = 390Ω
Slope resistance	R_S	-	1	2	Ω	R_{REF} = 390Ω
V_{REF} temperature coefficient		-	40	-	ppm/°C	R_{REF} = 390Ω

NOTE 1: Monotonic over full temperature range.

NOTE 2:The internal reference requires a 1µF stabilising capacitor between $V_{REF\ OUT}$ and 0V and a 390Ω resistor, R_{REF}, between V_{CC} and $V_{REF\ OUT}$.

INTRODUCTION

The ZN426 is an 8-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches plus a 2.5V precision voltage reference on a single monolithic chip.

The special design of the ladder network results in full 8-bit accuracy using normal defused resistors.

The use of on-chip voltage reference is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. In this case there is no need to supply power to the internal reference so R_{REF} and C_{REF} can be omitted.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig.3.

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

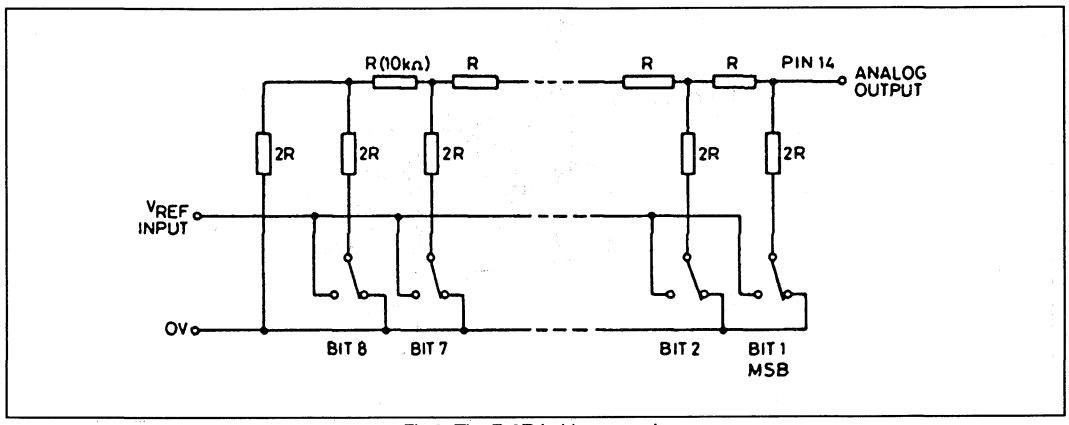


Fig.3 The R-2R ladder network

APPLICATIONS

8-bit D-A Converter

The ZN426 gives an analog voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the analog output resistance R_O, will be less than 0.004% per °C (or 1LSB/100°C) if R_L is chosen to be ≥ 650kΩ.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig.4 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{OUT} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{OUT} = Normal full-scale reading - 1LSB

iii. Repeat i. and ii.

e.g. Set F.S.R. to + 3.840V - 1LSB
=3.825V

$$(1LSB = \frac{3.84}{256} = 15.0mV)$$

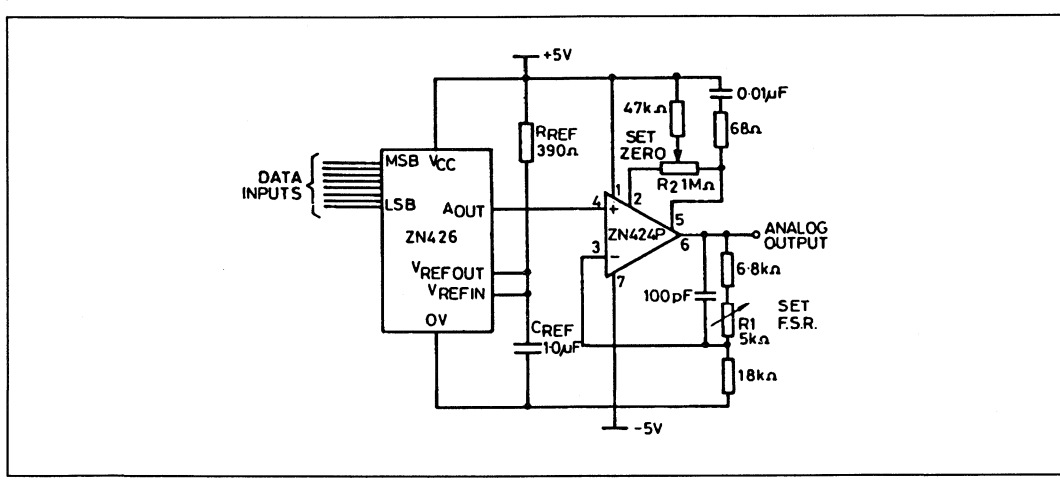


Fig.4 8-bit D-A converter

Alternative Output Buffer Using the 741

The circuit of Fig.5, employing the 741 operational amplifier, may be used as the output buffer.

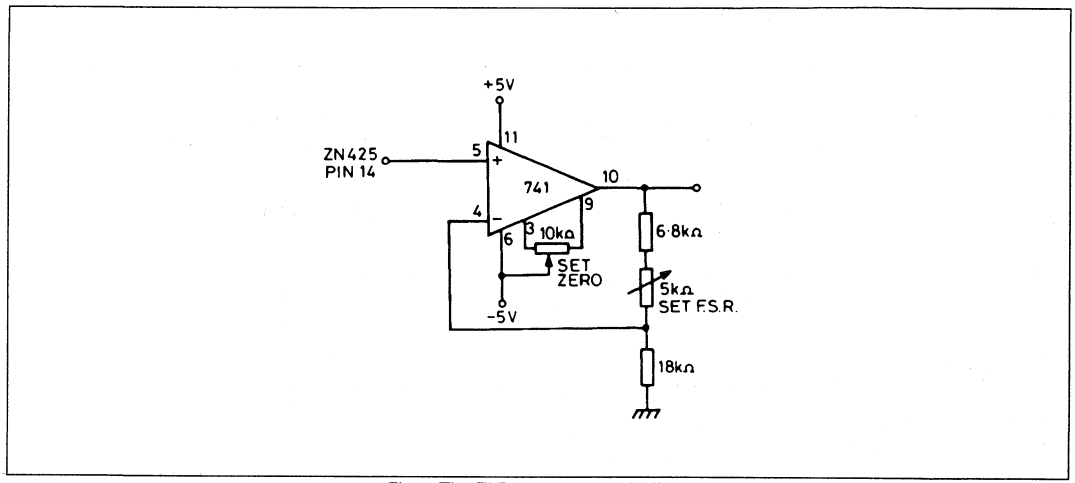


Fig.5 The ZLD741 as output buffer

DS3007-2.1

ZN428E8/ZN428J8/ZN428D

8-BIT LATCHED INPUT D-A CONVERTER

The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when enable is LOW and the data is held when enable is taken HIGH. The ZN428 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

FEATURES

- Contains DAC with Data Latch and On-Chip Reference
- Guaranteed Monotonic over the Full Operating Temperature Range
- Single +5V Supply
- Microprocessor Compatible
- TTL and 5V CMOS Compatible
- 800ns Settling Time
- Complementary to ZN427 A to D Series
- Commercial or Military Temperature Range

ORDERING INFORMATION

Device Type	Operating temperature	Package
ZN428D	0°C to +70°C	MP16W
ZN428E8	0°C to +70°C	DP16
ZN428J8	-55°C to +125°C	DC16

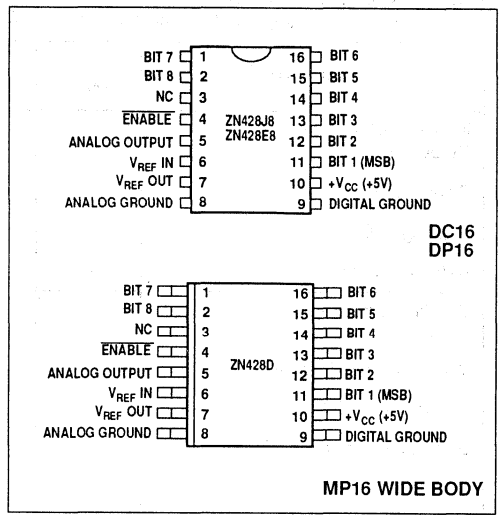


Fig.1 Pin connections (not to scale) - top view

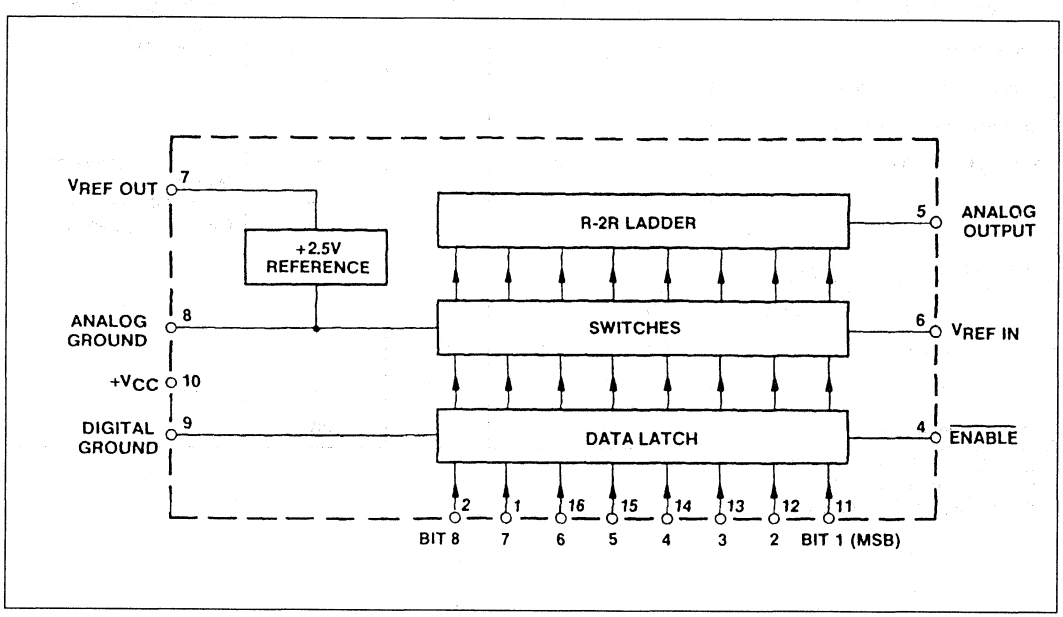


Fig.2 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max.voltage, logic and V_{REF} inputs	$+V_{CC}$
Operating temperature range	0°C to +70°C (ZN428E8, ZN428D) -55°C to +125°C (ZN428J8)
Storage temperature range	-55°C to +125°C
Analog ground to digital ground	±200mV

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_{amb} = 25°C unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference					
Output voltage	2.475	2.550	2.625	V	R_{REF} = 390Ω, C_{REF} = 1μF (123)
Slope resistance	-	0.5	2	Ω	
$V_{REF\ OUT}$ T.C.	-	50	-	ppm/°C	
Reference current	4	-	15	mA	Note 1
D-A Converter					
Linearity error	-	-	±0.5	LSB	2.0V ≤$V_{REF\ IN}$ ≤3.0V
Differential non-linearity	-	±0.5	-	LSB	
Linearity error T.C.	-	±3	-	ppm/°C	
Differential non-linearity T.C.	-	±6	-	ppm/°C	
Offset voltage	-	2	5	mV	All bits off
Offset voltage T.C.	-	±6	-	μV/°C	
Full-scale output	2.545	2.550	2.555		External reference $V_{REF\ IN}$ = 2.560V, all bits ON (123)
Full-scale output T.C.	-	2	-	ppm/°C	
Analog output resistance	-	4	-	kΩ	
External reference voltage	0	-	3.0	V	
Settling time to 0.5 LSB	-	800	-	ns	1 LSB major transition (Note 2)
	-	1.25	-	μs	All bits ON to OFF or OFF to ON (Note 2)
Operating temperature range:					
ZN428D and ZN428 E8	0	-	70	°C	
ZN428J8	-55	-	125	°C	
Supply voltage (V_{CC})	4.5	5.0	5.5	V	
Supply current	-	20	30	mA	Note 3
Power consumption	-	100	-	mW	

Note 1: See REFERENCE
Note 2: R_L = 10MΩ, C_L = 10pF
Note 3: All inputs HIGH (V_{IH} = 3.5V)

ELECTRICAL CHARACTERISTICS (cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
Logic (over specified operating temperature range)					
High level input voltage	2.0	-	-	V	
Low level input voltage	-	-	0.8	V	
High level input current	- -	- -	60 20	µA µA	V_{IN} = 5.5V, V_{CC} = Max. V_{IN} = 2.4V, V_{CC} = Max.
Low level input current	-	-	-5	µA	V_{IN} = 0.4V, V_{CC} = Max.
Input clamp diode voltage	-	-1.5	-	V	I_{IN} = -8mA
Enable pulse width	100	-	-	ns	
Data set-up time	150	-	-	ns	Note 4
Data hold time	10	-	-	ns	Note 5

Note 4: Set up time before $\overline{\text{ENABLE}}$ goes high
Note 5: Hold time after $\overline{\text{ENABLE}}$ goes high

D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig.3. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

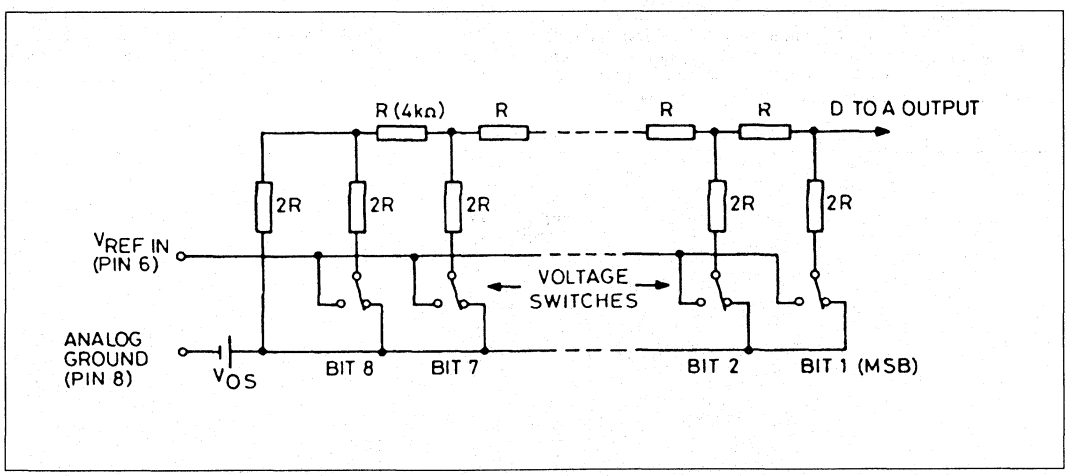


Fig.3 The R-2R ladder network

Analog output = $\frac{n}{256}$ ($V_{REF\ IN}$ - V_{OS}) + V_{OS}

where n is the digital input to the D-A from the data latch.

V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low (±6µV/°C)the effect on accuracy is negligible.

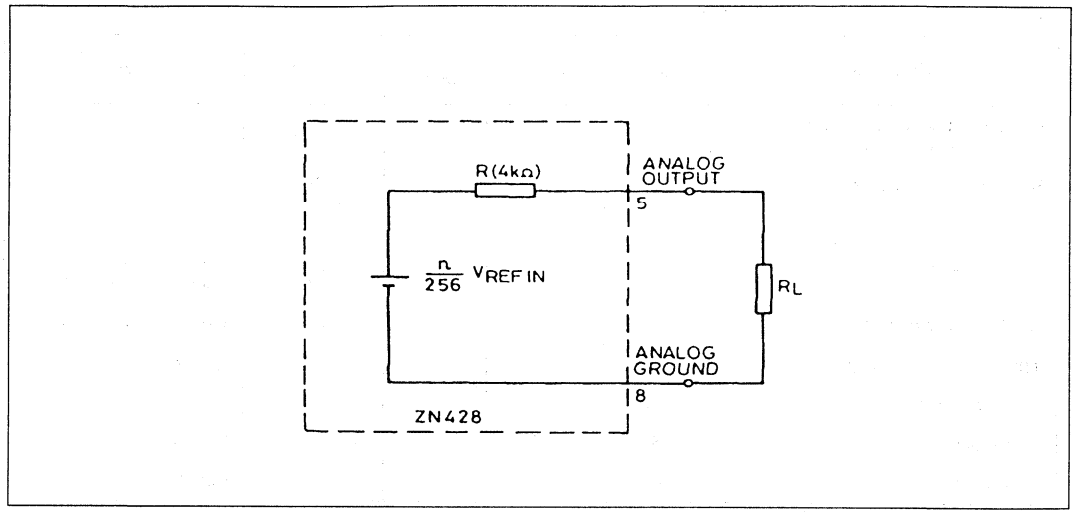


Fig.4 Analog output equivalent circuit

Fig.4 shows equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C.

R_L should be chosen as large as possible to make the gain drift small. As an example if R_L = 400kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN428 can be buffered by an amplifier (see Operating Notes).

REFERENCE

(a) Internal Reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with very low slope impedance (Fig.5). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 10) and pin 7. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor C_{REF} = 1μF is required between pins 7 and 8 for internal reference option, $V_{REF\ OUT}$ (pin 7) being connected to $V_{REF\ IN}$ (pin 6).

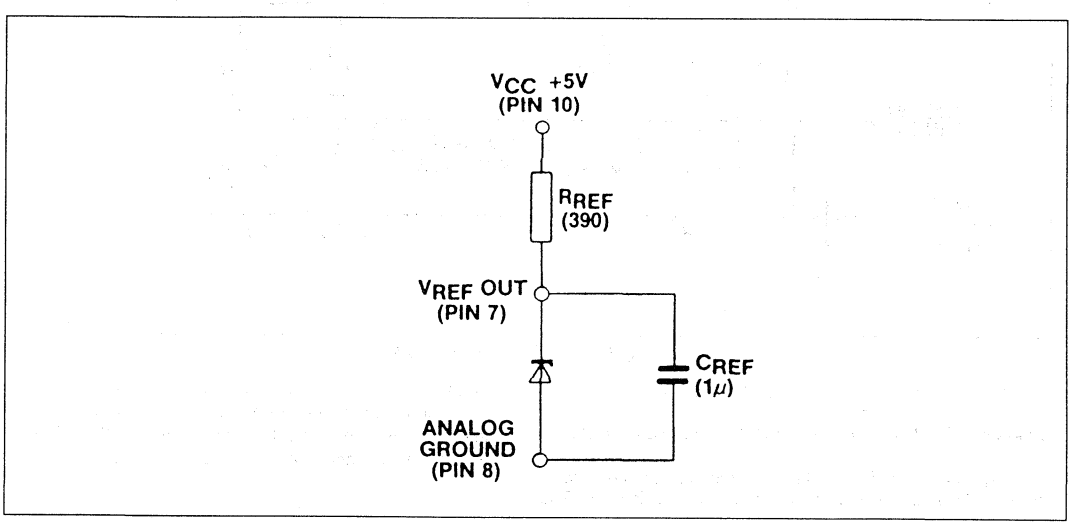


Fig.5 Internal voltage reference

Up to five ZN428s may be driven from one internal reference (there is no need to reduce R_{REF}). This useful feature saves power and gives excellent gain tracking between the converters.

(b) External Reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference should be less than $\frac{2.5}{n}\ \Omega$, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3V for ratiometric operation. The ZN428 is guaranteed monotonic for $V_{REF\ IN}$ above 2V.

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the $\overline{\text{ENABLE}}$ input is low the data inputs drive the D to A directly. When $\overline{\text{ENABLE}}$ goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig.6.

The ZN428 is provided with separate analog and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

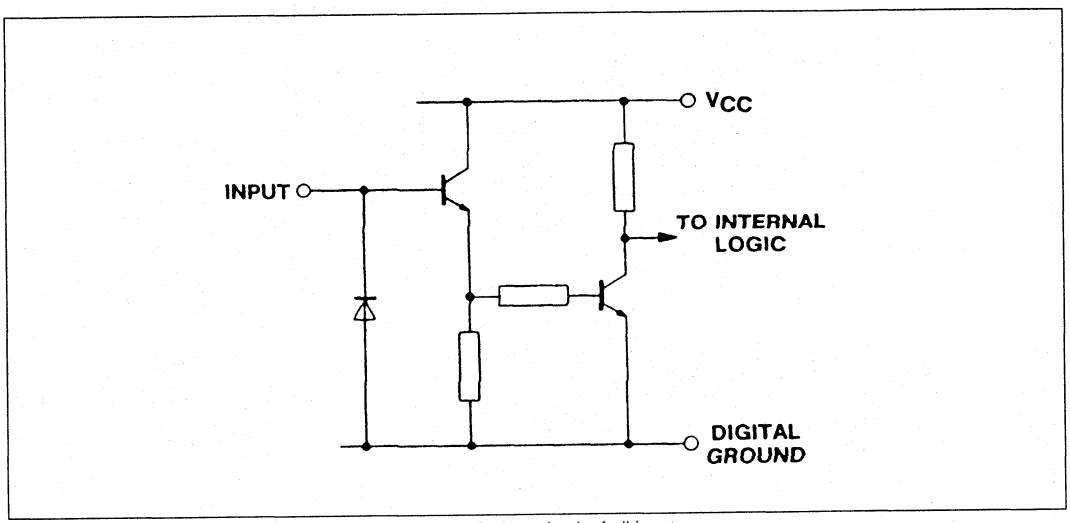


Fig.6 Equivalent circuit of all inputs

OPERATING NOTES

(1) Unipolar D-A Converter

The nominal output range of the ZN428 is 0 to $V_{REF\ IN}$ through a 4Ω resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig.7) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full-scale range is given by:

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ). The required nominal values of R1 and R2 are given by R1 = 4GkΩ and R_2 = 4G/(G-1)kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5V.

Output Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig.8. Settling time for a major transition is 1.5μs typical.

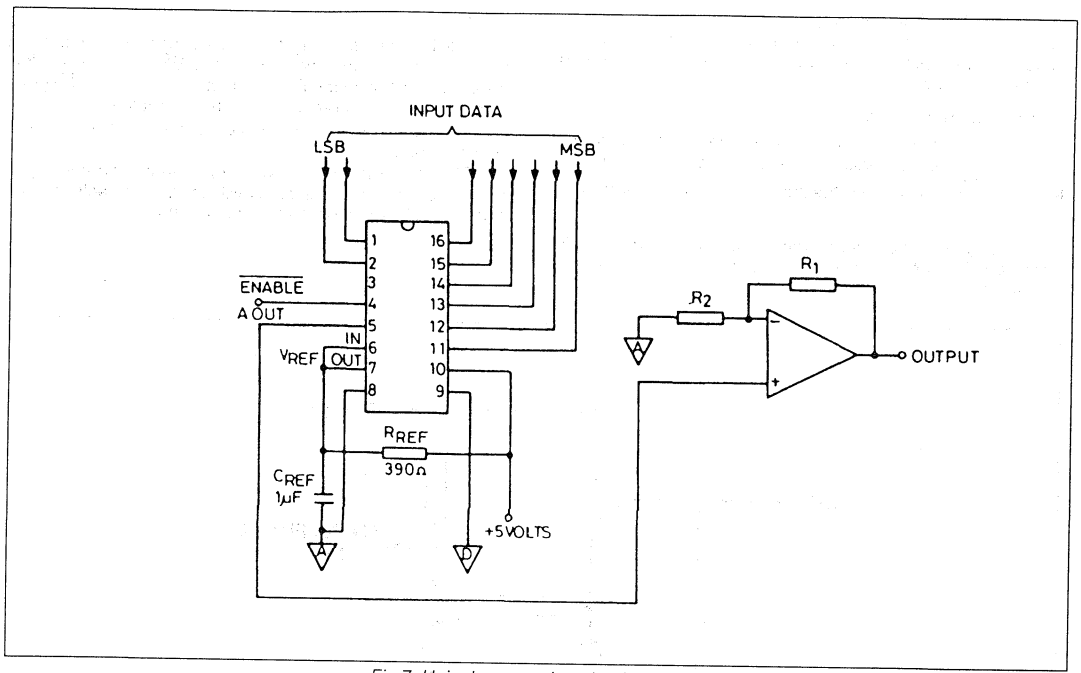


Fig.7 Unipolar operation - basic circuit

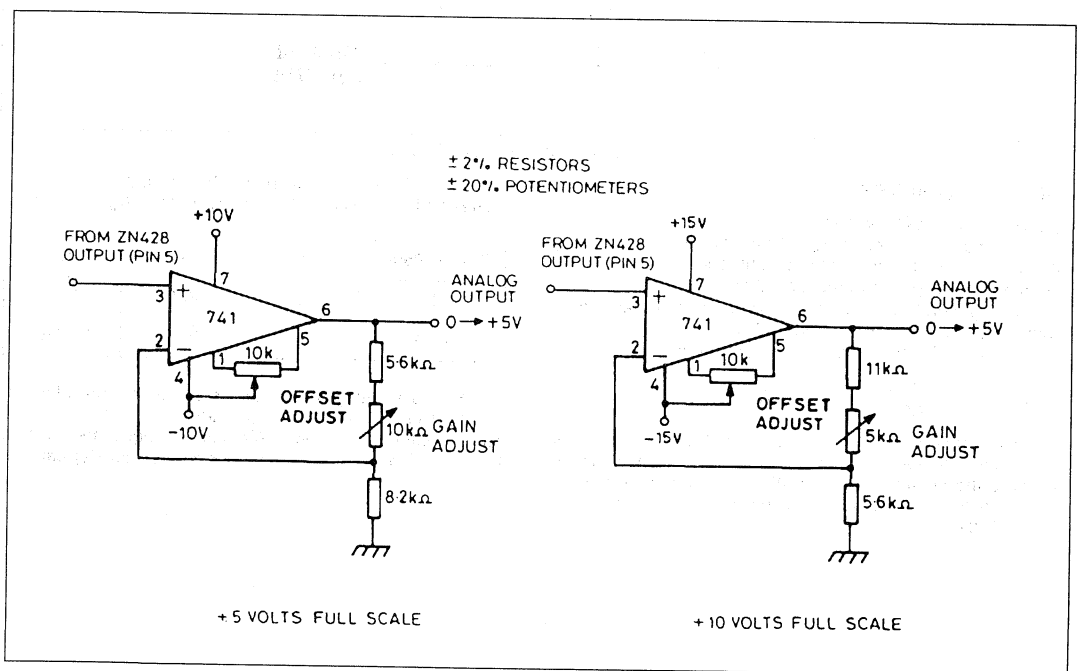


Fig.8 Unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust zero until V_{OUT} = 0.0000V.

(ii) Set all bits ON (high) and adjust gain until V_{OUT} = FS - 1LSB.

UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS - 1LSB
+5V	19.5 mV	4.9805V
+10V	39.1mV	9.9609V

$1LSB = \frac{FS}{256}$

UNIPOLAR LOGIC CODING

Input Code (Binary)	Analog Output (Nominal Value)
11111111	FS - 1LSB
11111110	FS - 2 LSB
11000000	$^3/_4$ FS
10000001	$^1/_2$ FS + 1LSB
10000000	$^1/_2$ FS
01111111	$^1/_2$ FS - 1LSB
01000000	$^1/_4$ FS
00000001	1LSB
00000000	0

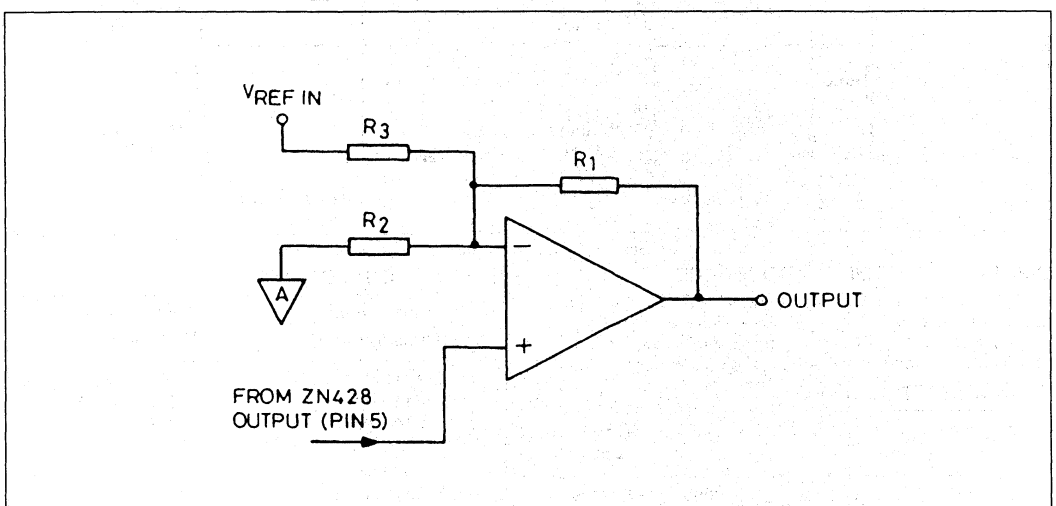


Fig.9 Bipolar operation - basic circuit

(2) Bipolar D-A Converter

For bipolar operation the output from the ZN428 is offset by half full-scale by connecting a resistor R3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig.9).

When the digital input to the ZN428 is zero the analog output is zero and the amplifier output should be -Full-scale. An input of all ones to the D-A will give a ZN428 output of $V_{REF\ IN}$ and the amplifier output required is +Full-scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$ and $R_3 = 8k\Omega$.

where the resultant output range is $\pm G\ V_{REF\ IN}$. A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN}$ = 2.5V the nominal values of resistors for ±5 and ±10V output ranges are given in the following table:

Output Range	G	R_1	R_2	R_3
+5V	2	16kΩ	16kΩ	8kΩ
+10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (0ffset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig.10.

Note that in the ±5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5µs typical.

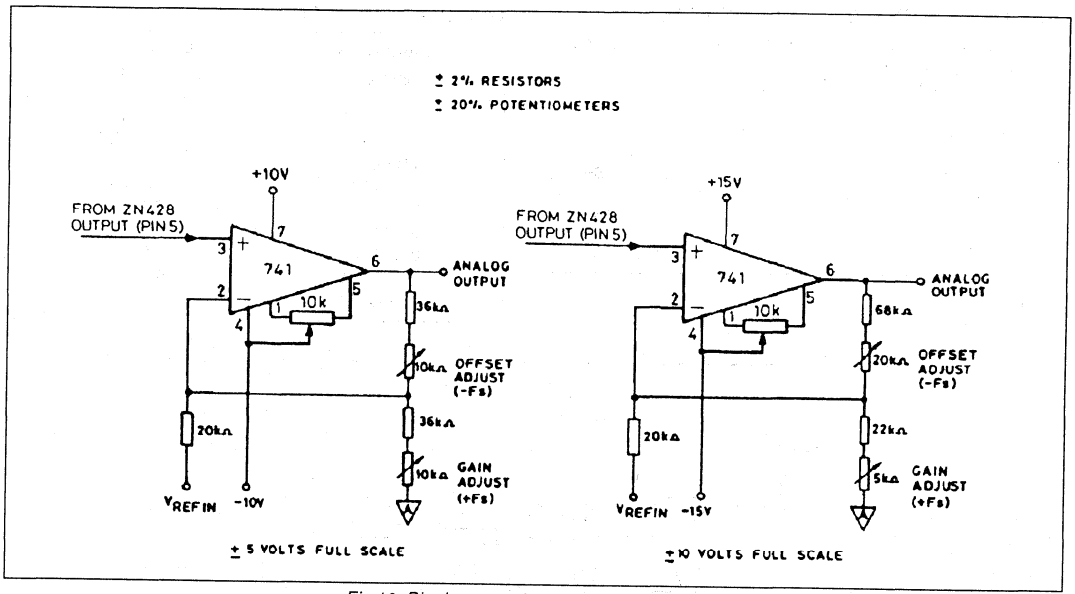


Fig.10 Bipolar operation - component values

BIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust offset until the amplifier output reads -full-scale.

(ii) Set all bits ON (high) and adjust gain until the amplifier output reads +(full-scale - 1LSB).

BIPOLAR SETTING UP POINTS

Input Range, ± FS	LSB	-FS	+(FS - 1LSB)
±5V	39.1 mV	-5.0000V	+4.9609V
±10V	78.1mV	-10.0000V	9.9219V

$1LSB = \frac{2FS}{256}$

BIPOLAR LOGIC CODING

Input Code (Offset Binary)	Analog Output (Nominal Value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2 LSB)
11000000	$+^1/_2$ FS
10000001	+ 1LSB
10000000	0
01111111	-1 LSB
01000000	$-^1/_2$ FS
00000001	-(FS - 1LSB)
00000000	-FS

DS3008-2.0

ZN429E8/ZN429D

LOW COST 8-BIT D-A CONVERTER

The ZN429 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

FEATURES

- Linearity Error $\pm^1/_2$ LSB
- Single +5V Supply
- Low Power Consumption 25mW Typical
- Settling Time 1 Microsecond Typical
- TTL and 5V CMOS Compatible
- Designed for Low Cost Applications

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+7.0V
Max. voltage, logic and V_{REF} inputs	+5.5V
Storage temperature range	-55°C to +125°C

ORDERING INFORMATION

Ambient operating temperature	-40°C to +85°C
Package, ZN429D	MP14
Package, ZN429E8	DP14

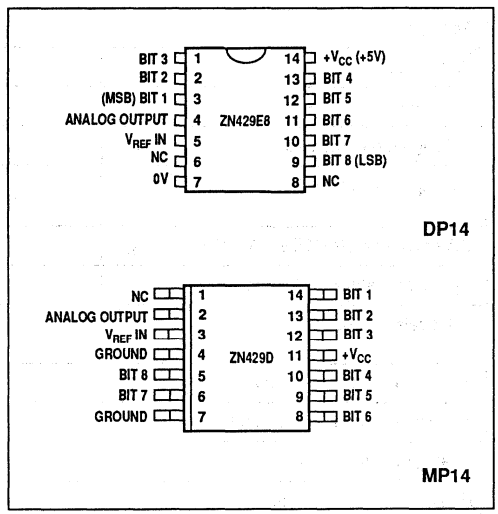


Fig.1 Pin connections (not to scale) - top view

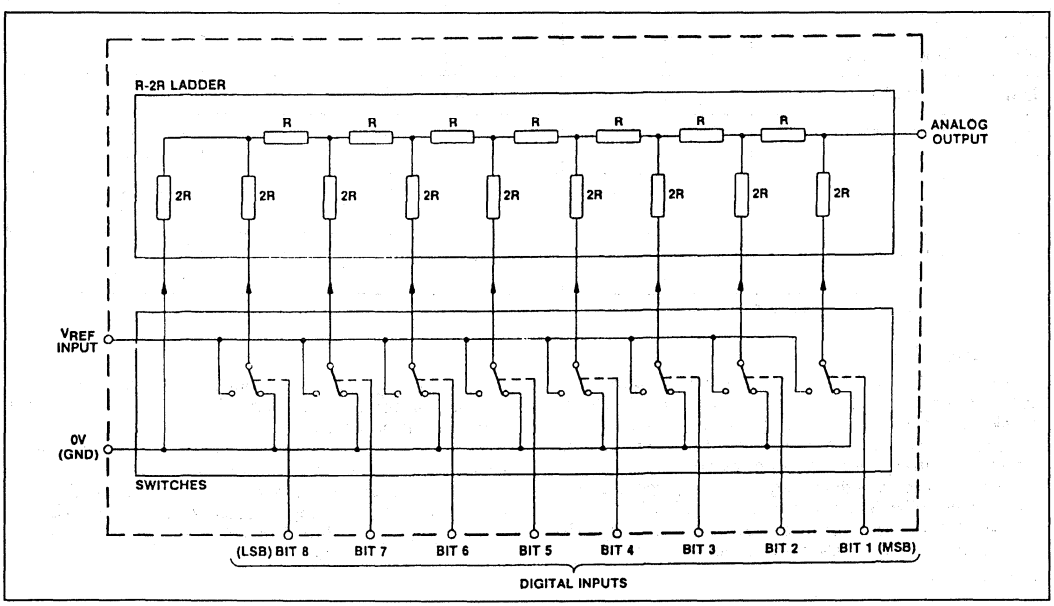


Fig.2 System diagram (see pin connection diagrams above for pin outs)

ELECTRICAL CHARACTERISTICS

(at T_{amb} = 25°C and V_{CC} = +5V unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	-	-	bits	
Accuracy		8	-	-	bits	
Non-linearity		-	-	±0.5	LSB	
Differential non-linearity		-	±0.5	-	LSB	Note 1
Settling time to 0.5LSB		-	1.0	-	µs	1 LSB step
Settling time to 0.5LSB		-	2.0	-	µs	All bits ON to OFF or OFF to ON
Offset voltage ZN429E8, ZN429D	V_{OS}	-	3.0	5.0	mV	All bits OFF
V_{OS} temperature coefficient		-	5	-	µV/°C	
Full-scale output		2.545	2.550	2.555	V	All bits ON Ext. V_{REF} = 2.56V
Full-scale temp. coefficient		-	3	-	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coefficient		-	7.5	-	ppm/°C	Relative to F.S.R.
Analog output resistance	R_O	-	10	-	kΩ	
External reference voltage		0	-	3.0	V	
Supply voltage	V_{CC}	4.5	-	5.5	V	
Supply current	I_S	-	5	9	mA	
High level input voltage	V_{IH}	2.0	-	-	V	
Low level input voltage	V_{IL}	-	-	0.7	V	
High level input current	I_{IH}	-	-	10	µA	V_{CC} = max. V_I = 2.4V
		-	-	100	µA	V_{CC} = max. V_I = 5.5V
Low level input current	I_{IL}	-	-	-0.18	mA	V_{CC} = max. V_I = 0.3V

NOTE 1: Monotonic over full temperature range.

INTRODUCTION

The ZN429 is an 8-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of the ladder network results in full 8-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig.3.

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2Ω.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN429 circuits and this is increased to ten for the ZN458 range.

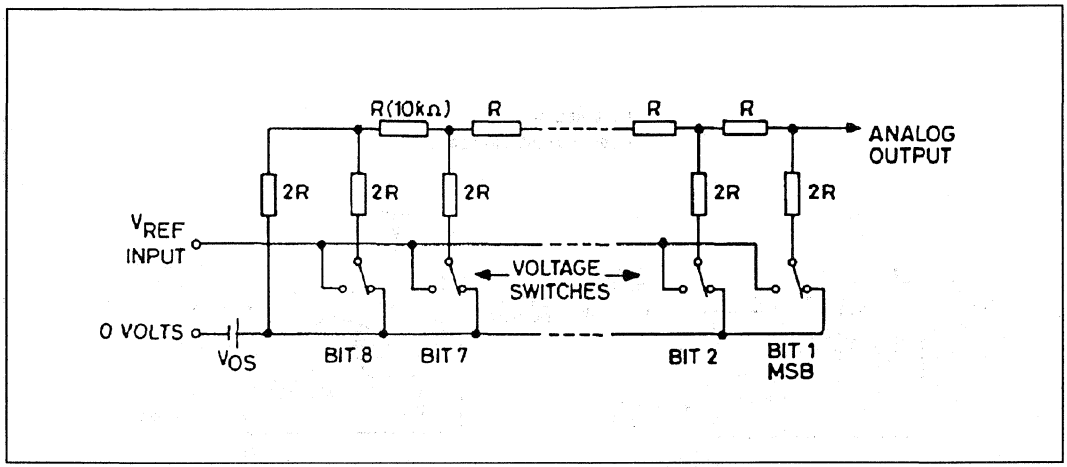


Fig.3 The R-2R ladder network

APPLICATIONS

(1) Unipolar D-A Converter

The nominal output range of the ZN429 is 0 to $V_{REF\ IN}$ through a 10Ω resistance. Other output ranges can readily be obtained by using an external amplifier.

The resulting full-scale range is given by

$$V_{OUT\ FS} = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (10kΩ). The required nominal values of R1 and R2 are given by

R1 = 10GkΩ and R_2 = 10G/(G-1)kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5V.

Output Range	G	R_1	R_2
+5V	2	20kΩ	20kΩ
+10V	4	40kΩ	13.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig.5. Settling time for a major transition is 2.5µs typical.

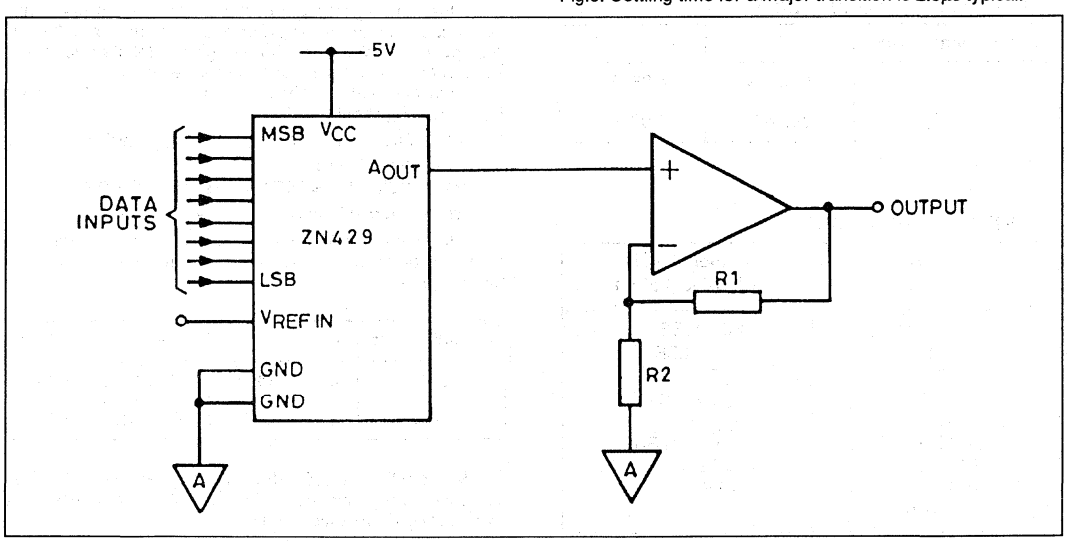


Fig.4 Unipolar operation - basic circuit

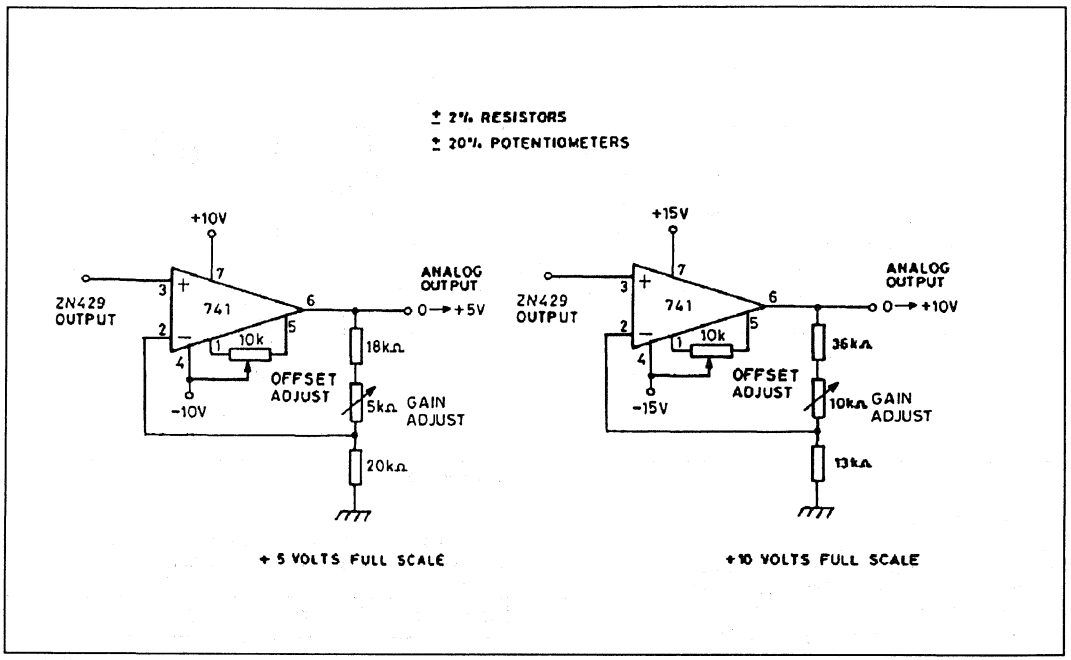


Fig.5 Unipolar operation - component values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (LOW) and adjust zero until V_{OUT} = 0.0000V.

(ii) Set all bits ON (HIGH) and adjust gain until V_{OUT} = FS - 1LSB.

UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS - 1LSB
+5V	19.5 mV	4.9805V
+10V	39.1mV	9.9609V

$1LSB = \frac{FS}{256}$

UNIPOLAR LOGIC CODING

Input Code (Binary)	Analog Output (Nominal Value)
11111111	FS - 1LSB
11111110	FS - 2 LSB
11000000	$^3/_4$ FS
10000001	$^1/_2$ FS + 1LSB
10000000	$^1/_2$ FS
01111111	$^1/_2$ FS - 1LSB
01000000	$^1/_4$ FS
00000001	1LSB
00000000	0

(2) Bipolar D-A Converter

For bipolar operation the output from the ZN429 is offset by half full-scale by connecting a resistor R3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig.6).

When the digital input of the ZN429 is zero the analog output is zero and the amplifier output should be -full-scale. An input of all ones to the D-A will give a ZN429 output of $\frac{255}{256}$ $V_{REF\ IN}$ and the amplifier output required is +full-scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 10kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

R1 = 20GkΩ, R2 = 20G/(G-1)kΩ and R3 = 20kΩ.

where the resultant output range is $\pm G.V_{REF\ IN}$.

Assuming that $V_{REF\ IN}$ = 2.5V the nominal values of resistors for ±5 and ±10V output ranges are given in the following table:

Output Range	G	R_1	R_2	R_3
±5V	2	40kΩ	40kΩ	20kΩ
±10V	4	80kΩ	26.67kΩ	20kΩ

Minus full scale (0FFSET) is set by adjusting R1 about its nominal value relative to R3. Plus full-scale (GAIN) is set by adjusting R2 relative to R1.

Settling time for a major transistion is 2.5µs typical.

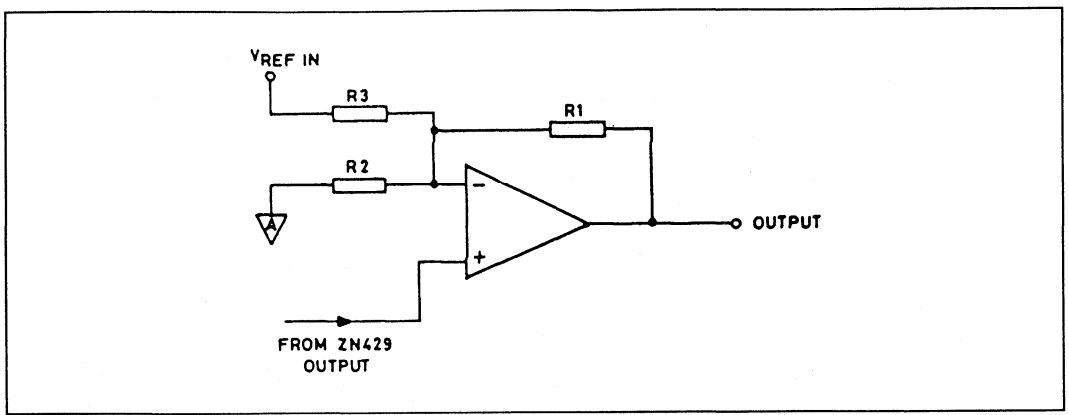


Fig.6 Bipolar operation - basic circuit

BIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (LOW) and adjust OFFSETuntil the amplifier output reads -FULL-SCALE.

(ii) Set all bits ON (HIGH) and adjust gain until the amplifier reads +(FULL-SCALE - 1LSB).

BIPOLAR SETTING UP POINTS

Input Range, ± FS	LSB	-FS	+(FS - 1LSB)
±5V	39.1 mV	-5.0000V	+4.9609V
±10V	78.1mV	-10.0000V	9.9219V

$1LSB = \frac{2FS}{256}$

BIPOLAR LOGIC CODING

Input Code (Offset Binary)	Analog Output (Nominal Value)
11111111	+(FS - 1LSB)
11111110	+(FS - 2 LSB)
11000000	$+^1/_2$ FS
10000001	+ 1LSB
10000000	0
01111111	-1 LSB
01000000	$-^1/_2$ FS
00000001	-(FS - 1LSB)
00000000	-FS

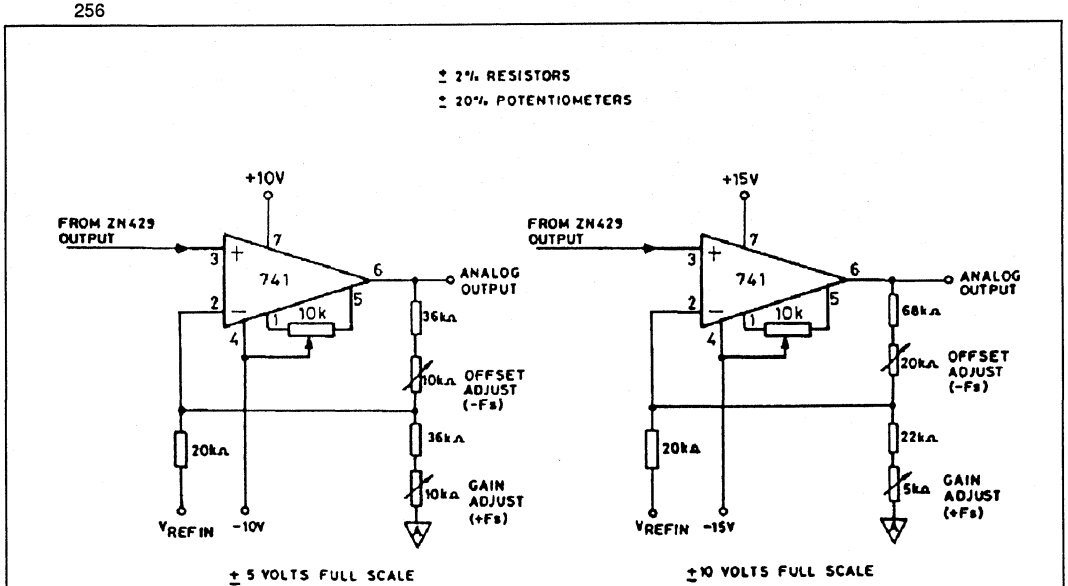


Fig.7 Bipolar operation - component values

Section 3
Advanced Function ADCs

GEC PLESSEY
SEMICONDUCTORS

ZN427E8 / ZN427J8

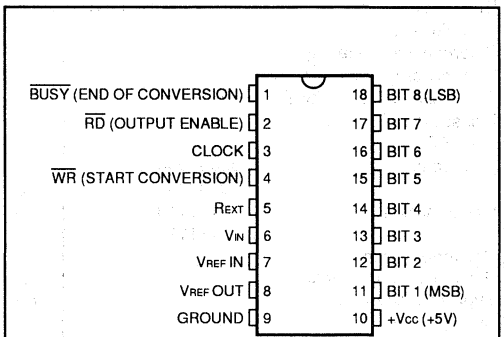
MICROPROCESSOR COMPATIBLE 8-BIT SUCCESSIVE APPROXIMATION A-D CONVERTER

The ZN427 is an 8-bit successive approximation converter with three-state outputs to permit easy interfacing to a common data bus. The IC contains a voltage switching DAC, a fast comparator, successive approximation logic and a 2.56V precision bandgap reference, the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted, thus allowing ratiometic operation

Only passive external components are required for operation of the converter.

FEATURES

- Easy Interfacing to Microprocessor, or Operates as a 'Stand-Alone' Converter
- Fast: 10 microseconds Conversion time Guaranteed
- No Missing Codes over Operating Temperature Range
- Data Outputs Three-State TTL Compatible, other Logic Inputs and Output TTL and CMOS Compatible
- Choice of On-Chip or External Reference Voltage
- Ratiometric Operation
- Unipolar or Bipolar Input Ranges
- Complementary to ZN428 DAC
- Commercial or Military Temperature Range



ZN427J8 (DC18)
ZN427E8 (DP18)

Fig.1 Pin connection - top view

ORDERING INFORMATION

Device type	Operating temperature	Package
ZN427E8	0°C to +70°C	DP18
ZN427J8	-55°C to +125°C	DC18

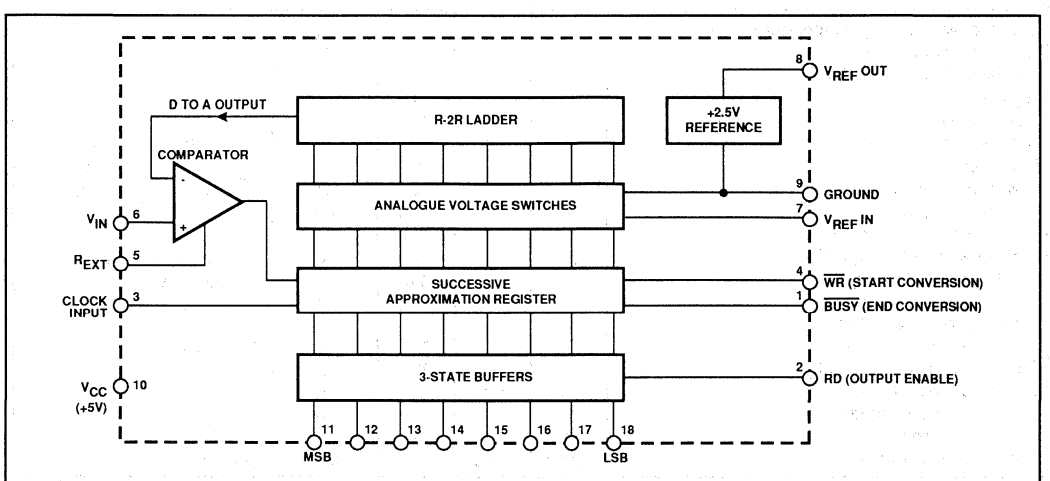


Fig.2 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7.0V
Max. voltage, logic and V_{REF} input	+V_{CC}
Operating temperature range	0°C to +70°C (ZN427E8)
	-55°C to +125°C (ZN427J8)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C unless otherwise specified).

Parameter		Min.	Typ.	Max.	Units	Conditions
Converter						
Resolution		8	-	-	Bits	
Linearity error		-	-	±0.5	LSB	
Differential non-linearity		-	±0.5	-	LSB	
Linearity error T.C.		-	±3	-	ppm/°C	
Differential non-linearity T.C.		-	±6	-	ppm/°C	
Full-scale (gain) T.C.		-	±2.5	-	ppm/°C	External Ref. 2.5V
Zero T.C.		-	±8	-	µV/°C	
Zero transition	00000000	12	15	18	mV	DC Package
	to 00000001	10	13	16	mV	DP Package
F.S. transition	11111110	2.545	2.550	2.555	V	$V_{REF\ IN}$ = 2.560V
	to 11111111					
Conversion time		-	-	10	µs	See note 1
External reference voltage		1.5	-	3.0	V	
Supply voltage (V_{CC})		4.5	-	5.5	V	
Supply current		-	25	40	mA	
Power consumption		-	125	-	mW	
Comparator						
Input current		-	1	-	µA	V_{IN} = +3V, R_{EXT} = 82kΩ
Input resistance		-	100	-	kΩ	V - = -5V
Tail current, I_{EXT}		25	-	15	µA	
Negative supply, V–		-3.0	-	-30.0	V	See comparator (page x-xx)
Input voltage		-0.5	-	3.5	V	
Internal voltagee reference						
Output voltage		2.475	2.560	2.625	V	R_{REF} = 390Ω, C_{REF} = 4µ7
Slope resistance		-	0.5	2	Ω	
V_{REF} temperature coefficient		-	50	-	ppm/°C	
Reference current		4	-	15	mA	See reference (page x-xx)
Logic (over operating temperature range)						
High level input voltage V_{IH}		2.0	-	-	V	
Low level input voltage V_{IL}		-	-	0.8	V	
High level input current,		-	-	50	µA	V_{IN} = 5.5V, V_{CC} = max.
$\overline{WR}$ and RD inputs I_{IH}		-	-	15	µA	V_{IN} = 2.4V, V_{CC} = max.
High level input current,		-	-	100	µA	V_{IN} = 5.5V, V_{CC} = max.
Clock input I_{IH}		-	-	30	µA	V_{IN} = 2.4V, V_{CC} = max.
Low level input current I_{IL}		-	-	-5	µA	V_{IN} = 0.4V, V_{CC} = max.
High level output current I_{OH}		-	-	-100	µA	
Low level output current I_{OL}		-	-	1.6	mA	
High level output voltage V_{OH}		2.4	-	-	V	I_{OH} = max., V_{CC} = min.
Low level output voltage V_{OL}		-	-	0.4	V	I_{OL} = max., V_{CC} = min.
Disable output leakage		-	-	2	µA	V_O = 2.4V
Input clamp diode voltage		-	-	-1.5	V	
Read input to data output		-	-	250	ns	See Fig.9
Enable/disable delay time t_{RD}		-	180	250	ns	
Start pulse width tWR		250	160	-	ns	See Fig.9
$\overline{WR}$ to $\overline{BUSY}$ propagation delay t_{BD}		-	-	250	ns	
Clock pulse width		500	-	-	ns	
Maximum clock frequency		900	1000	-	kHz	See note 1

Note 1: A 900kHz clock gives a conversion time of 10µs (9 clock periods).

GENERAL CIRCUIT OPERATION

The ZN427 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the

MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$.

Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the ninth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held high to keep the three-state buffers in their high impedance state. Data can be read out by taking RD high, thus enabling the three-state output. Readout is non-destructive. The $\overline{BUSY}$ output may be tied to the RD input to automatically enable the outputs when the data is valid.

For reliable operation of the converter the start pulse applied to the $\overline{WR}$ input must meet certain timing criteria with respect to the converter clock. These are detailed in the timing diagram of Fig.3.

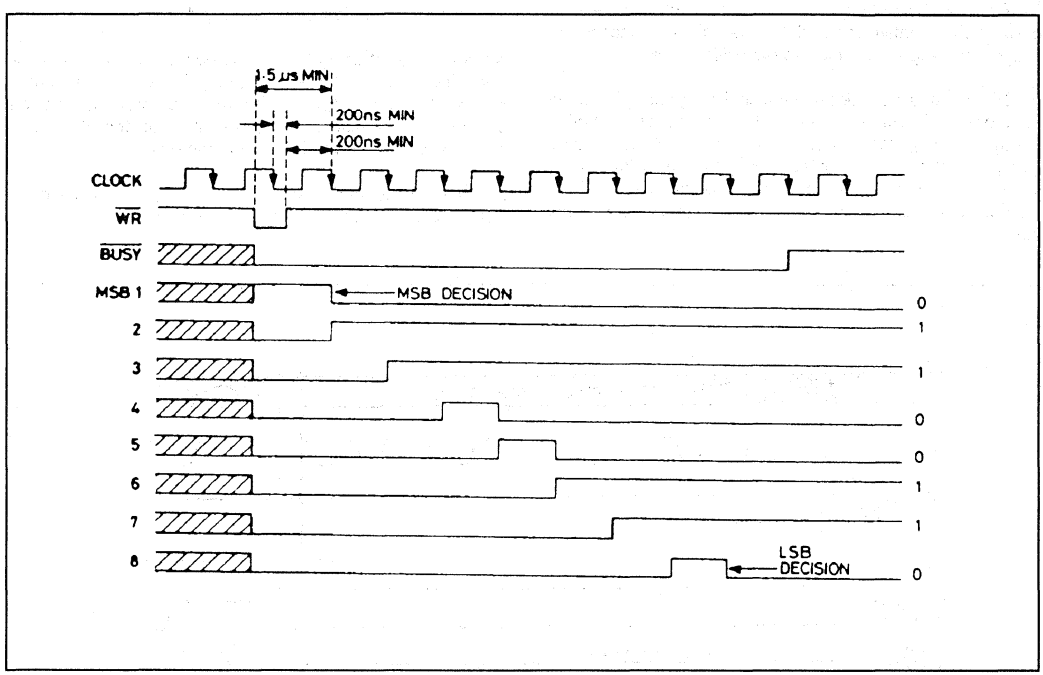


Fig.3 Timing diagram

NOTES ON TIMING DIAGRAM

1. A conversion sequence is shown for the digital word 01100110. For clarity the three-state outputs are shown as being enabled during the conversion, but normal practice would be to disable them until the conversion was complete.

2. The $\overline{BUSY}$ output goes low during a conversion. When $\overline{BUSY}$ goes high at the end of a conversion the output data is valid. In a microprocessor system the $\overline{BUSY}$ output can be used to generate an interrupt request when the conversion is complete.

3. In the timing diagram cross hatching indicates a 'don't care' condition.

4. The start pulse operates as an asynchronous (independent of clock) reset that sets the MSB output to 1 and sets all other outputs and the end of conversion flag to 0. This resetting occurs on the low-going edge of the start pulse and as long as $\overline{WR}$ is low the converter is inhibited. Conversion commences on the first active (negative going) clock edge after the $\overline{WR}$ input has gone high again, when the MSB decision is made. A number of timing constraints thus supply to the start pulse.

(a) The minimum duration of the start pulse is 250ns, to allow reliable resetting of the converter logic circuits.

(b) There is no limit to the maximum duration of the start pulse.

(c) To allow the MSB to settle at least 1.5µs must elapse between the negative going edge of the start pulse and the first active clock edge that indicates the MSB desicion.

(d) To ensure relaible clocking the positive-going edge of the start pulse should not occur within 200ns of an active (negative-going) clock edge. The ideal place for the positive-going edge of the start pulse is coincident with a positive-going clock edge. As a special case of the above conditions that start pulse may be synchronous with a negative-going clock pulse.

PRACTICAL CLOCK AND SYNCHRONISING CIRCUITS

The actual method of generating the clock signal and synchronising it to the start conversion system in which the ZN427 is incorporated.

When used with a microprocessor the ZN427 can be treated as RAM and can be assigned a memory address using an address decoder. If the µP clock is used to drive the ZN427 and the µP write pulse meets the ZN427 timing criteria with respect to the µP clock then generating the start pulse is simply a matter of gating the decoded address with the microprocessor write pulse. Whilst the conversion is being performed the microprocesor can perform other instructions or No operation (NOP). when the conversion is complete the outputs can be enabled onto the bus by gating the decoded address with the read pulse. A timing diagram for this sequence of operation is given in Fig.4.

An advantage of using the microprocessor clock is that the conversion time is known precisely in terms of machine cycles. the data outputs may therefore be read after a fixed delay of at least nine clock cycles after the end of the $\overline{WR}$ pulse, when the conversion will be complete.

Alternatively the read operation may be initiated by using the $\overline{BUSY}$ output to generate interrupt request.

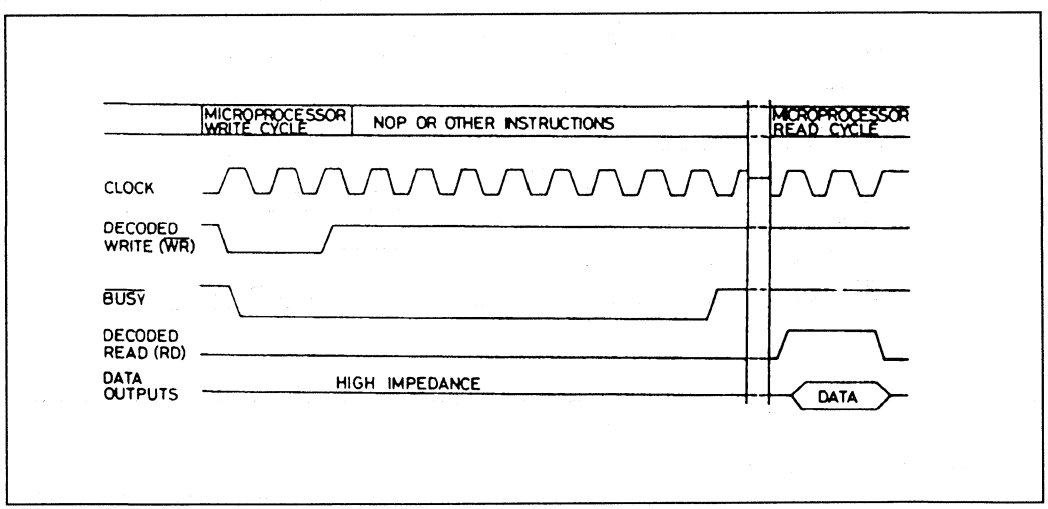


Fig.4 Typical timing diagram using µP clock and write pulse

In some systems, for example single-chip microcomputers such as the 8048, this simple method may not be feasible for one or more of the following reasons:

(a) The MPU clock is not available externally.

(b) The clock frequency is too high.

(c) The write pulse timing criteria make it unsuitable for direct use as a start conversion pulse.

If any of these conditions apply then the self-synchronising clock circuit of Fig.5a is recommended.

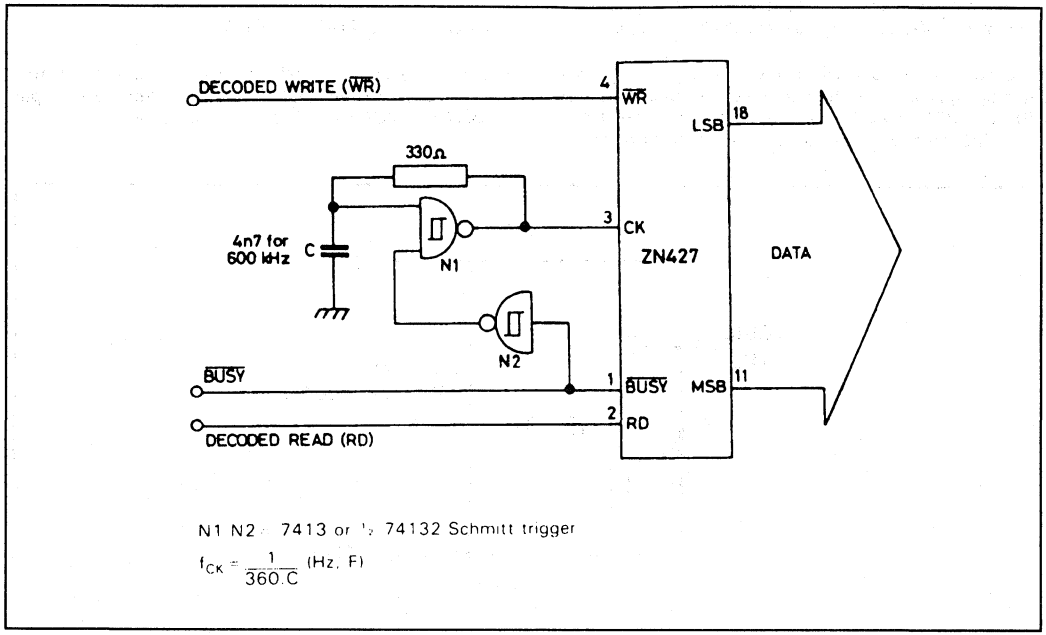


Fig.5a Self-synchronising clock circuit

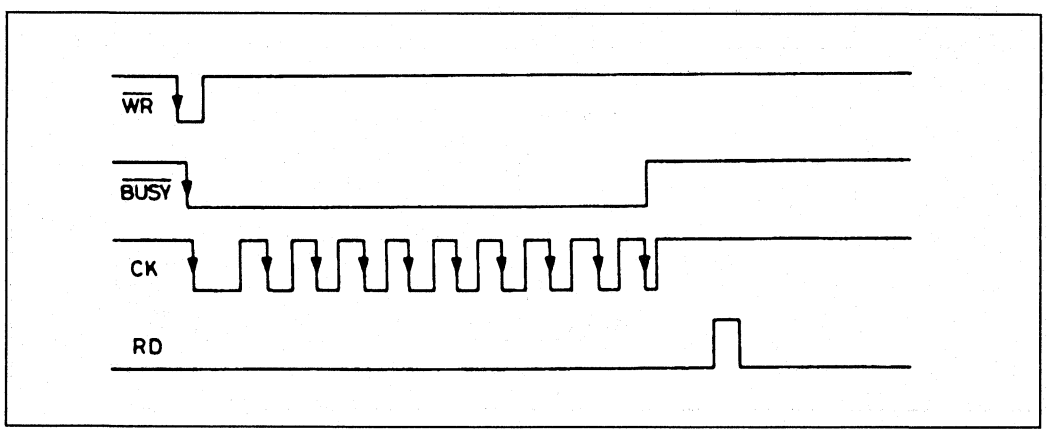


Fig.5b Timing diagram for circuit of Fig.5a

N1 is connected as an astable multivibrator which, when the $\overline{BUSY}$ output is high, is inhibited by the output of N2 holding one of its inputs low. The start conversion pulse resets the $\overline{BUSY}$ flag and N1 begins to oscillate. When the conversion is complete $\overline{BUSY}$ goes high and the clock is inhibited.

Since the start pulse starts the clock it may occur at any time. The only constraints on the start pulse are that it must be longer than 250ns but at least 200ns shorter than the first clock pulse. The first clock pulse is in fact longer than the rest since C1 starts from a fully charged condition whereas on subsequent cycles it changes between the upper and lower threshold (V_{T+} and V_T) of the Schmitt trigger.

LOGIC INPUTS AND OUTPUTS

The logic inputs of the ZN427 utilise the emitter-follower configuration shown in Fig.6. This gives extremely low input currents for CMOS as well as TTL compatibility.

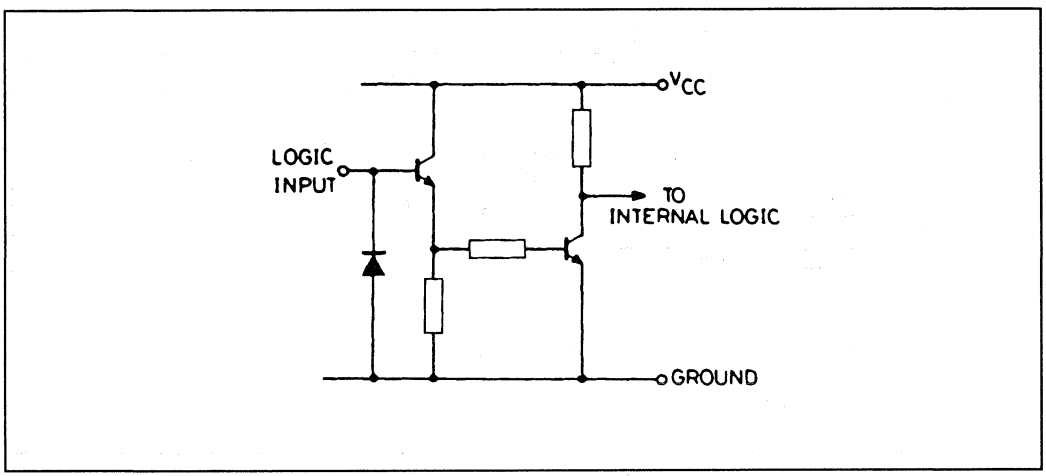


Fig.6 Equivalent circuit of all inputs

The $\overline{BUSY}$ output, shown in Fig.7, utilises a passive pullup for CMOS/TTL compatibility.

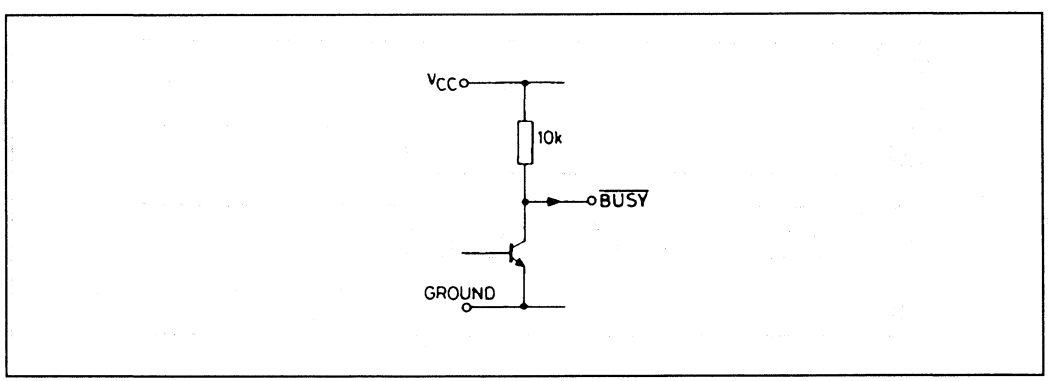


Fig.7

The data outputs have three-state buffers, an equivalent circuit of which is shown in Fig.8. Whilst the RD input is low both output transistors are turned off and the output is in a high impedance state. When RD is high the data output will assume the appropriate logic state (0 or 1).

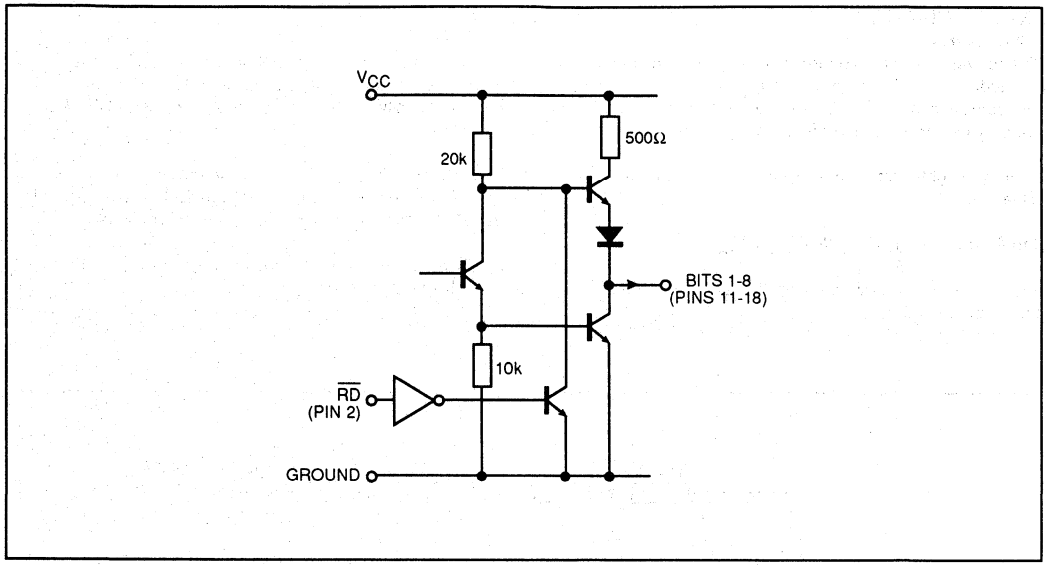


Fig.8 Equivalent circuit of data outputs

A test circuit and timing diagram for the output enable/disable delays are given in Fig.9.

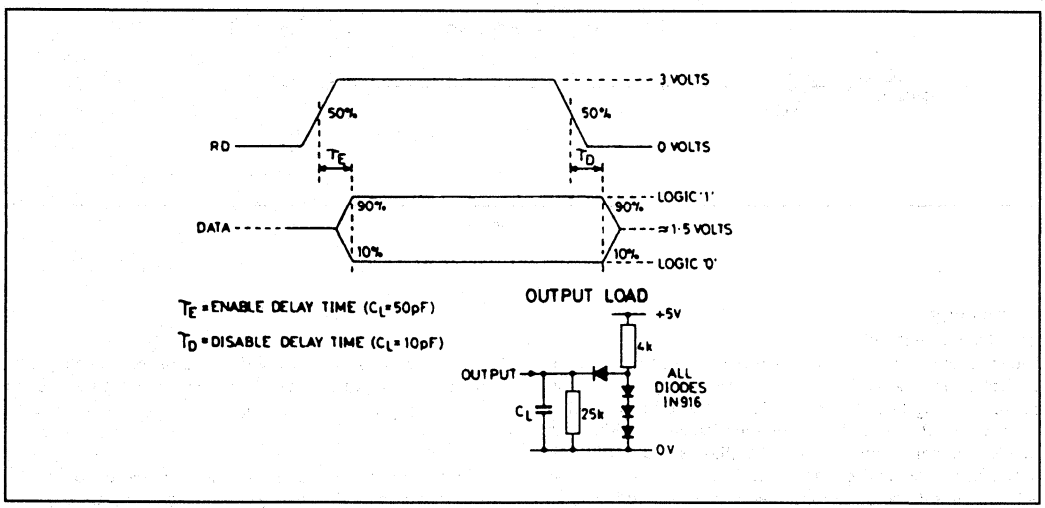


Fig.9 Output enable/disable waveforms

ANALOG CIRCUITS

D-A converter

IThe converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig.10. Each element is connected to either 0V or V_{REF} IN by transistor voltage switches specially designed for low offset voltage (<1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

D to A output = $\frac{n}{256}$ (V_{REF} IN -V_{OS}) + V_{OS}

where n is the digital input to the D-A from successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 2mV for the ZN427E8 and 4mV for the ZN427J8.

This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8μV/°C), the effect on accuaracy will be negligible.

The D-A output range can be considered to be 0 - $V_{REF\ IN}$ through an output resistance R (4k).

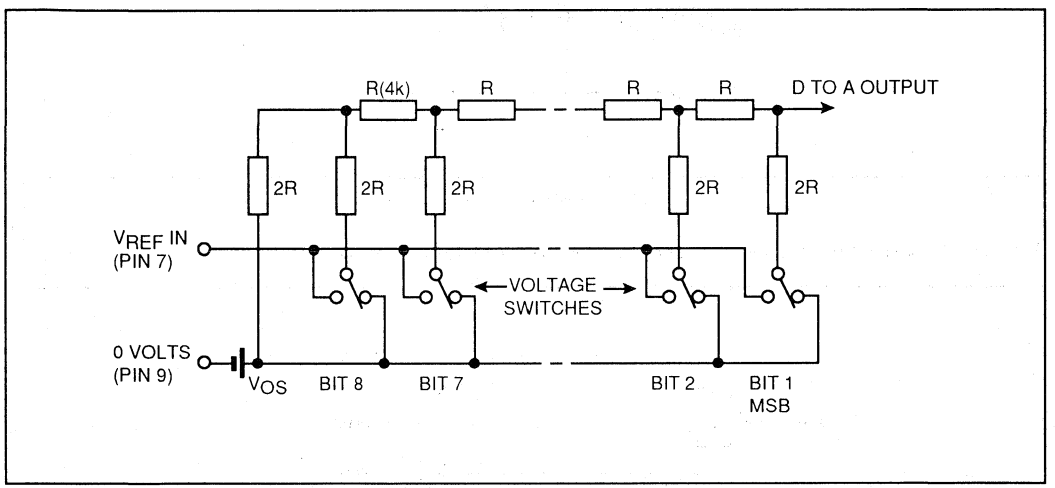


Fig.10 R-2R ladder network

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.11). A Resistor (R_{REF}) should be connected between pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of (5.0 - 2.5)/0.39=6.4mA. A stabilising/decoupling capacitor, C_{REF} (4μ7), is required between pins 8 and 9. For internal reference operation V_{REF} OUT (pin 8) is connected to V_{REF} IN (pin 7).

UP to five ZN427's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

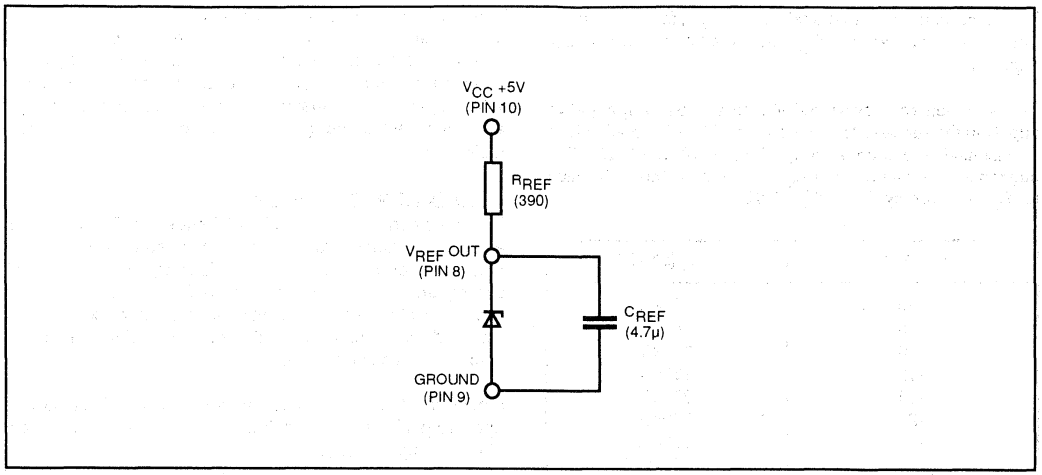


Fig.11 Internal voltage reference

(b) External reference

If required an external reference in the range +1.5 to +3.0V may be connected to V_{REF} IN. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN427 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN448/9 will operate if V_{REF} IN is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN427 contains a fast comparator, the equivalent input circuit of which is shown in Fig.12.

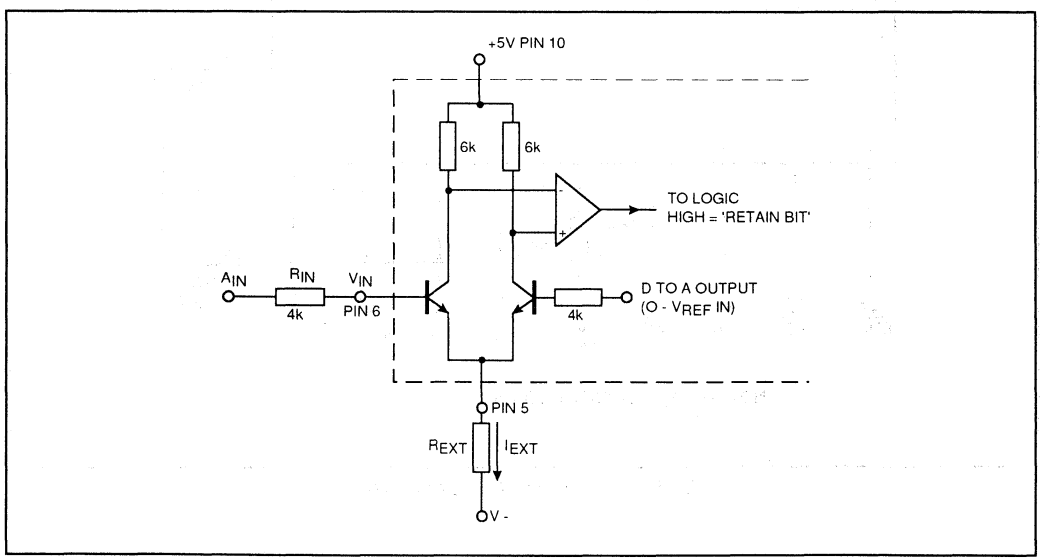


Fig.12 Comparator equivalent circuit

The comparator derives the tail current, I_{EXT}, for its first stage from an external resistor, R_{EXT}, which is taken to a negative supply V–.

This arrangement allows the ZN427 to work with any negative supply in the range -3 to -30 volts. the ZN427 is designed to be insensitive to changes in I_{EXT} from 25µA to 150µA. The suggested nominal value of I_{EXT} is 65µA and a suitable value for R_{EXT} is given by $R_{EXT} = |V\_|15k\Omega$.

V_ (volts)	R_{EXT} (±10%)
-3	47kΩ
-5	82kΩ
-10	150kΩ
-12	180kΩ
-15	220kΩ
-20	330kΩ
-25	390kΩ
-30	470kΩ

The output from the D-A converter is connected through the 4kΩ ladder resistance to one side of the comparator. The analog input to be converted could be connected directly to the other comparator input (V_{IN}, pin 6) but for optimum stability with temperature the analog input should be applied through a source resistance (R_{IN} = 4kΩ) to match the ladder resistance).

ANALOG INPUT RANGES

The basic connection of the ZN427 shown in Fig.13 has an analog input range 0 to V_{REF} IN which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analog input input range so that the comparator always sees a positive input voltage.

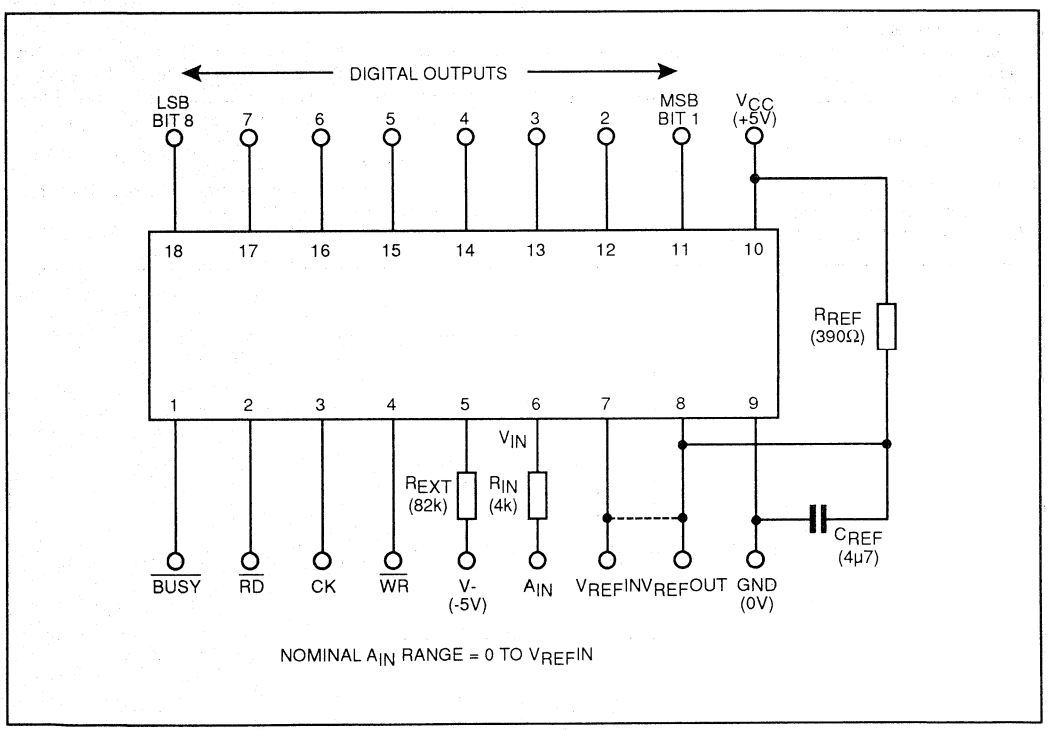


Fig.13 External components for basic operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig.14.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF}IN$ when the analogue input (A_{IN}) is at full-scale.

The resulting full-scale range is given by:

$$A_{IN}FS = \left(1 + \frac{R_1}{R_2}\right), V_{REF}IN = G.V_{REF}IN.$$

To match the ladder resistance R_1/R_2 (R_{IN}) = 4kΩ.

The required nominal values of R_1 and R_2 are given by $R_1 = 4Gk$, $R_2 = \frac{4G}{G-1}$ kΩ

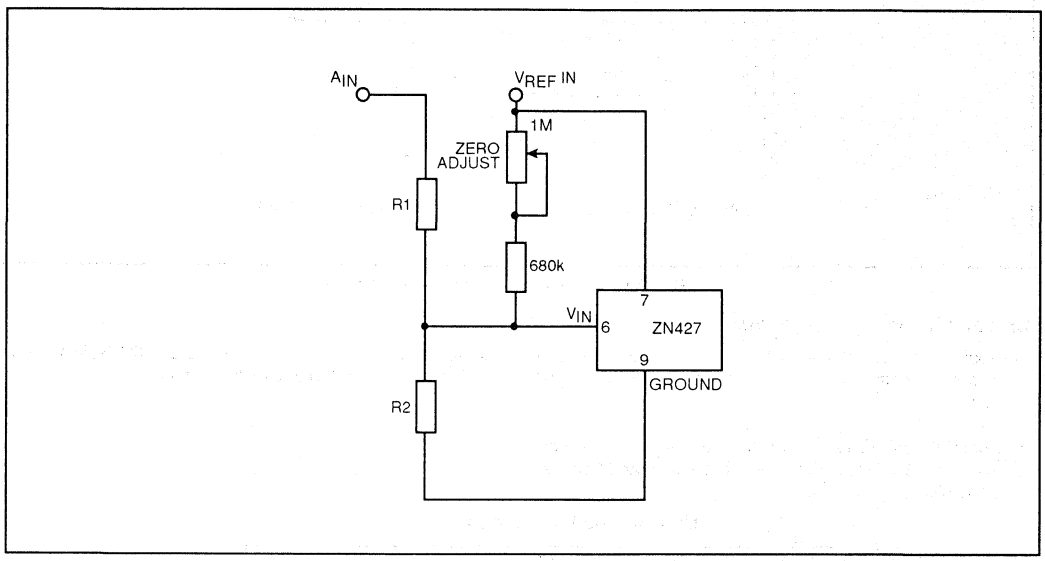


Fig.14 Unipolar operation - general connection

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF}IN$ = 2.5V.

Input range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

Gain adjustment

Due to tolerance in R_1 and R_2, tolerance in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

Zero adjustment

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which correpsonds to 1.5LSB with a 2.56V reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of +0.5LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1.5 times $V_{REF}IN$.

Practical circuit values for +5 and +10V input ranges are given in Fig.15, which incorporates both zero and gain adjustments.

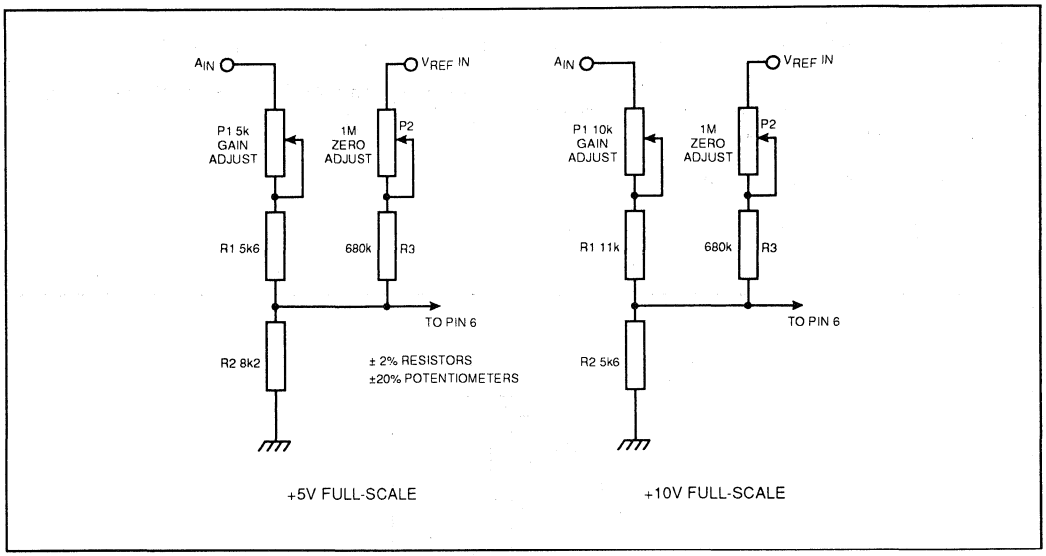


Fig.15 Unipolar operation - component values

Unipolar adjustment prodedure

(i) Apply continuous convert pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full-scale minus 1.5LSB to A_{IN} and adjust off-set until the 8 bit (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply 0.5LSB) to A_{IN} and adjust zero until 8 bit just flickers between 0 and 1 with all other bits at 1.

Unipolar setting up points

Input range, +FS	0.5LSB	FS - 1.5LSB
+5V	9.8mV	4.9707V
+10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

Unipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (offset binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
0.75FS	11000000
0.5FS + 1LSB	10000001
0.5FS	10000000
0.5FS - 1LSB	01111111
0.25FS	01000000
1LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN427 is offset by half full-scale by connecting a resistor R_3 between V_{REF} IN and V_{IN} (Fig.16).

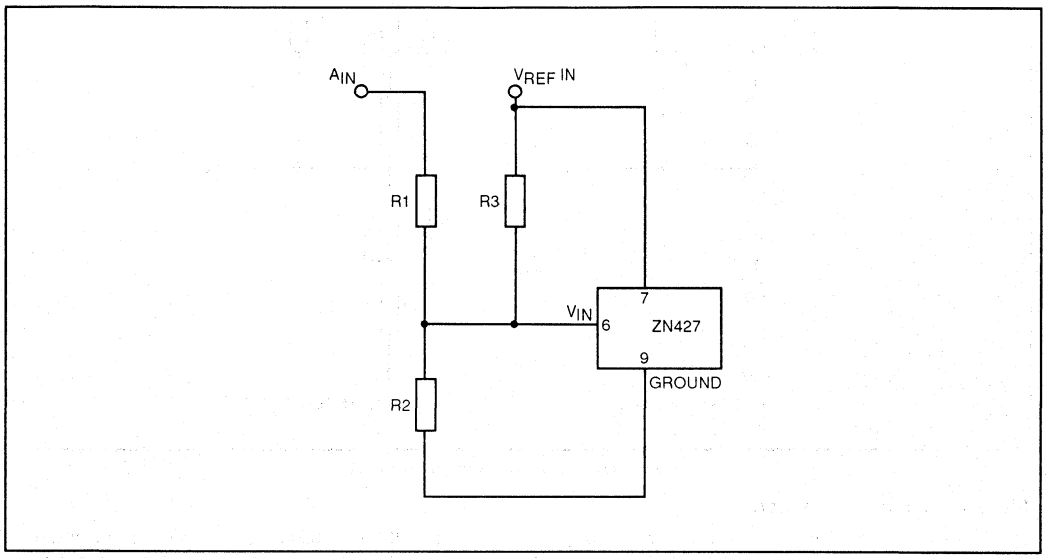


Fig.16 Bipolar operation - general connection

When A_{IN} = -FS, V_{IN} needs to be equal to zero.

When A_{IN} = +FS, V_{IN} needs to be equal to V_{REF} IN.

If the full-scale range is $\pm$G. V_{REF} IN then $R_1 = (G - 1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ ($=R_{IN}$) = 4k.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8$ GkΩ, $R_2 = 8G/(G - 1)$k, $R_3 = 8$kΩ.

A bipolar range of $\pm V_{REF}$ IN (which corresponds to the basic unipolar range 0 to $+V_{REF}$ IN) results if $R_1 = R_3 = 8$kΩ and $R_2 = \infty$.

Assuming the $V_{REF\,IN} = 2.5$V the nominal values of resistors for ±5 and ±10V input ranges are given in the following table.

Input range	G	R_1	R_2	R_3
+5V	2	16kΩ	16kΩ	8kΩ
+10V	4	32kΩ	10.66kΩ	8kΩ

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig.17.

Note that in the ±5V case R_3 has been chosen as 7.5k (instead of 8.2k) to obtain a more symmetrical range of adjustment using standard potentiometers.

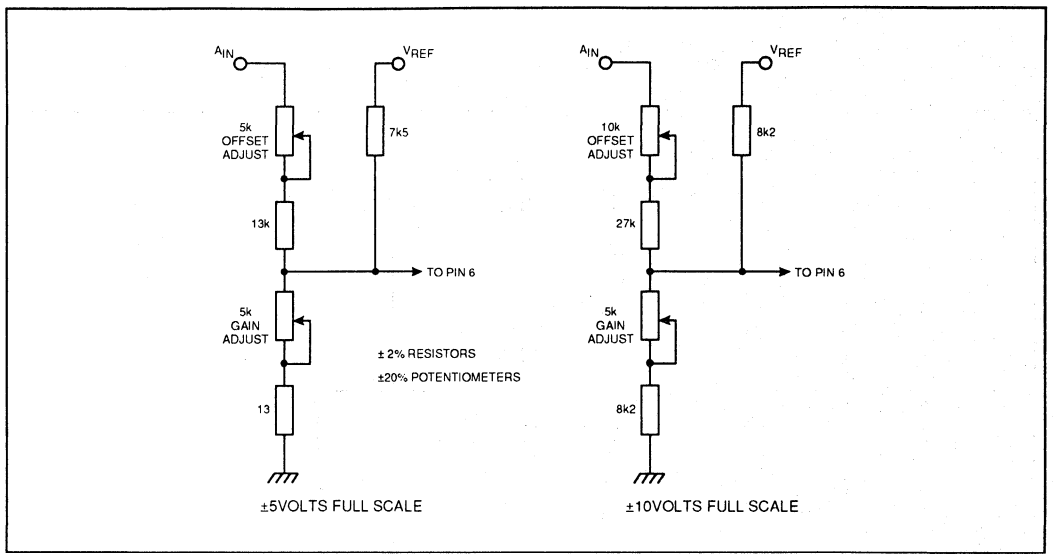


Fig.17 Bipolar operation - component values

Bipolar adjustment prodedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply -(FS -0.5LSB) to A_{IN} and adjust off-set until the 8 bit (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS -1.5LSB) to A_{IN} and adjust gain until the 8 bit just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

Bipolar setting up points

Input range, ±FS	-(FS -0.5LSB)	+(FS -1.5LSB)
+5V	-4.9805V	+4.9414V
+10V	-9.9609V	+9.8828V

$$1LSB = \frac{2FS}{265}$$

Bipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (offset binary)
+(FS - 1LSB)	11111111
+(FS - 2LSB)	11111110
+0.5FS	11000000
+1LSB	10000001
0	10000000
-1LSB	01111111
-0.5FS	01000000
-(FS - 1LSB)	00000001
-FS	00000000

SINGLE 5 V SUPPLY RAIL OPERATION

The ZN427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig.18 works with any clock frequency from 10kHz to 1MHz and can supply up to five ZN427's.

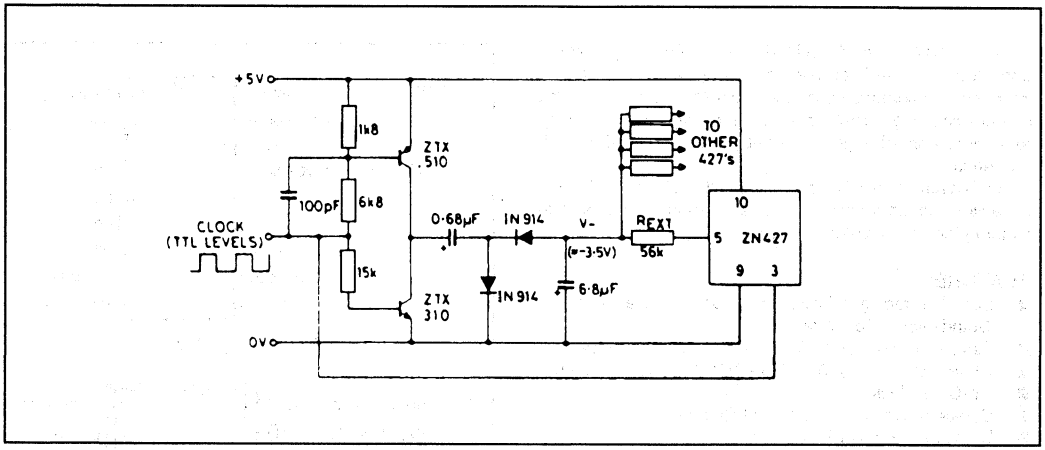


Fig.18 single 5V supply operation

ZN448/ZN449

8-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTER

The ZN448 and ZN449 are 8-bit successive approximation A-D converters designed to be easily interfaced to microprocessors. All active circuitry is contained on-chip including a clock generator and stable 2.5V bandgap reference, control logic and double buffered latches with reference.

Only a reference resistor and capacitor, clock resistor and capacitor and input resistors are required for operation with either unipolar or bipolar input voltage.

FEATURES

- Easy Interfacing to Microprocessor, or operates as a 'Stand-Alone' Converter
- Fast: 9 microseconds Conversion time Guaranteed
- Choice of Linearity: 0.5 LSB - ZN448, 1 LSB - ZN449
- On-Chip Clock
- Choice of On-Chip or External Reference Voltage
- Unipolar or Bipolar Input Ranges
- Commercial Temperature Range

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN448E	0.5	0°C to +70°C	DP18
ZN449D	1	0°C to +70°C	MP18
ZN449E	1	0°C to +70°C	DP18

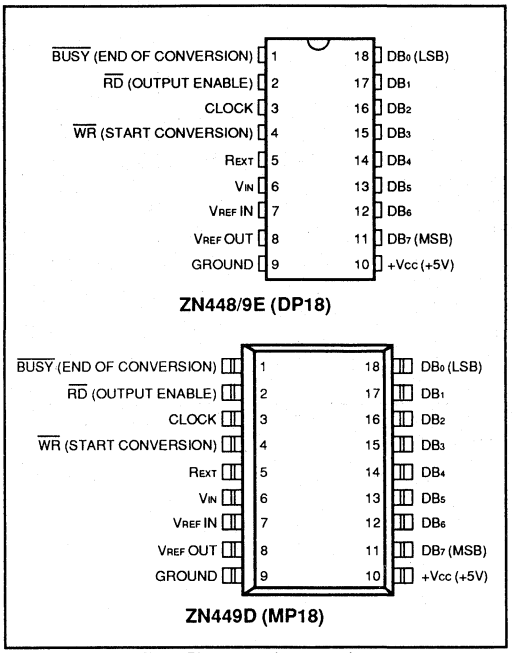


Fig.1 Pin connection - top view

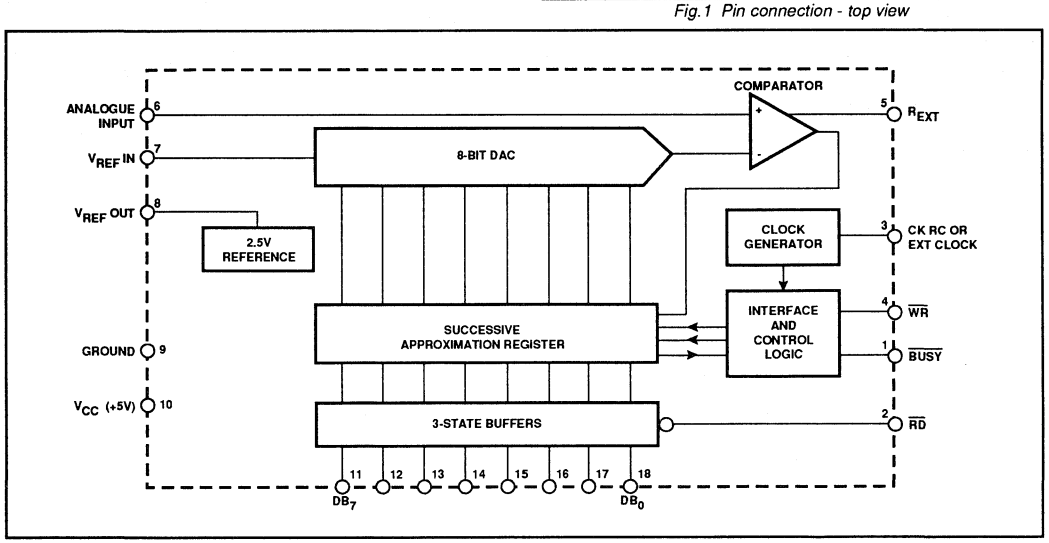


Fig.2 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	+7
Max. voltage, logic and V_{REF} input	$+V_{CC}$
Operating temperature range	0°C to +70°C (MP and DP package)
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C and f_{CLK} = 1.6MHz unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
ZN448					
Linearity error	-	-	±0.5	LSB	
Differential linearity error	-	-	±0.75	LSB	
Zero transition (00000000→00000001)	12	15	18	mV	DP package
Full-scale→transition (11111110 11111111)	2.545	2.550	2.555	V	V_{REF} = 2.560V
ZN449					
Linearity error	-	-	±1	LSB	
Differential linearity error	-	-	±1	LSB	
Zero transition	7	12	17	mV	MP package
(00000000→00000001)	10	15	20	mV	DP package
Full-scale→transition (11111110 11111111)	2.542	2.550	2.558	V	V_{REF} = 2.560V
All Types					
Resolution	8	-	-	bits	
Linearity temperature coefficient	-	±3	-	ppm/°C	
Differential linearity temperature coefficient	-	±6	-	ppm/°C	
Full-scale temperature coefficient	-	±2.5	-	ppm/°C	
Zero temperature coefficient	-	±8	-	µV/°C	
Reference input range	1	-	3	V	
Supply voltage	4.5	5	5.5	V	
Supply current	-	25	40	mA	
Power consumption	-	125	200	mW	
Comparator					
Input current	-	1	-	µA	V_{IN} = +3V, R_{EXT} = 82kΩ
Input resistance	-	100	-	kΩ	
Tail current	25	65	150	µA	V - = -5V
Negative supply	-3	-5	-30	V	
Input voltage	-0.5	-	+3.5	V	
On-chip reference					
Output voltage ZN448	2.520	2.550	2.580	V	R_{REF} = 390Ω
ZN449	2.520	2.550	2.600		C_{REF} = 4µ7
Slope resistance	-	0.5	2	Ω	
V_{REF} temperature coefficient	-	50	-	ppm/°C	
Reference current	4	-	15	mA	

ELECTRICAL CHARACTERISTICS (Cont.)

Parameter	Min.	Typ.	Max.	Units	Conditions
Clock					
On-chip clock frequency	-	-	1	MHz	
Clock frequency temperature coefficient	-	+0.5	-	%/°C	
Clock resistor	-	-	2	kΩ	
Maximum external clock frequency	0.9	-	1	MHz	
Clock pulse width	500	-	-	ns	
High level input voltage V_{IH}	4	-	-	V	
Low level input voltage V_{IL}	-	-	0.8	V	
High level input current I_{IH}	-	-	800	µA	V_{IN} = +4V, V_{CC} = MAX
Low level input current I_{IL}	-	-	-500	µA	V_{IN} = +0.8V, V_{CC} = MAX
Logic (over operating temperature range)					
Convert input					
High level input voltage V_{IH}	2	-	-	V	
Low level input voltage V_{IL}	-	-	0.8	V	
High level input current I_{IH}	-	300	-	µA	V_{IN} = +2.4V, V_{CC} = MAX
Low level input current I_{IL}	-	±10	-	µA	V_{IN} = +0.4V, V_{CC} = MAX
$\overline{RD}$ **input**					
High level input voltage V_{IH}	2	-	-	V	
Low level input voltage V_{IL}	-	-	0.8	V	
High level input current I_{IH}	-	+150	-	µA	V_{IN} = +2.4V, V_{CC} = MAX
Low level input current I_{IL}	-	-300	-	µA	V_{IN} = +0.4V, V_{CC} = MAX
High level output voltage V_{OH}	2.4	-	-	V	I_{OH} = +2.4V, V_{CC} = MAX
Low level output voltage V_{OL}	-	-	0.4	V	I_{OL} = +0.4V, V_{CC} = MAX
High level output current I_{OH}	-	-	-100	µA	
Low level output current I_{OL}	-	-	1.6	mA	
Three-state disable output leakage	-	-	2	µA	V_{OUT} = +2V
Input clamp diode voltage	-	-	-1.5	V	
$\overline{RD}$ input to data output	-	180	250	ns	
Enable/disable delay times T_{E1}	180	210	260	ns	
T_{E0}	60	80	100	ns	
T_{D1}	80	110	140	ns	
T_{D0}	60	80	100	ns	
Convert pulse width $t_{\overline{WR}}$	200	-	-	ns	
$\overline{WR}$ input to $\overline{BUSY}$ output	-	-	250	ns	

GENERAL CIRCUIT OPERATION

The ZN448/9 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} < V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$.

Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the eighth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held high to keep the three-state buffers in their high impedance state. Data can be read out by taking $\overline{RD}$ low, thus enabling the three-state output. Readout is non-destructive.

CONVERSION TIMING

The ZN448/9 will accept a low-going CONVERT pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 7.5 and 8.5 clock pulses later depending on the relative timing of the clock and CONVERT signals. Timing diagrams for the conversion are shown in Fig.3.

The converter is cleared by a low-going CONVERT pulse, which sets the most significant bit and results all the other bits and the $\overline{BUSY}$ flag. Whilst the CONVERT input is low the MSB output of the DAC is continuously compared with the analogue input, but otherwise the converter is inhibited.

After the CONVERT input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The CONVERT pulse can be as short as 200ns; however the MSB must be allowed to settle for at least 550ns before the MSB decision is made. To ensure that this criterion is met even with short CONVERT pulses the converter waits, after the CONVERT input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 550ns at maximum clock frequency. The CONVERT input is not locked out during a conversion and if it is oulsed low at any time the converter will restart.

The $\overline{\text{BUSY}}$ output goes high simultaneously with the LSB decision, at the end of a conversion indicating data valid. Note that if the three-state data outputs are enabled during a conversion the valid data will be available at the outputs after the rising edge of the $\overline{\text{BUSY}}$ signal. If, however the outputs are not enabled until after $\overline{\text{BUSY}}$ goes high then the data will be subject to the propagation delay of the three-state buffers. (See under DATA OUTPUTS).

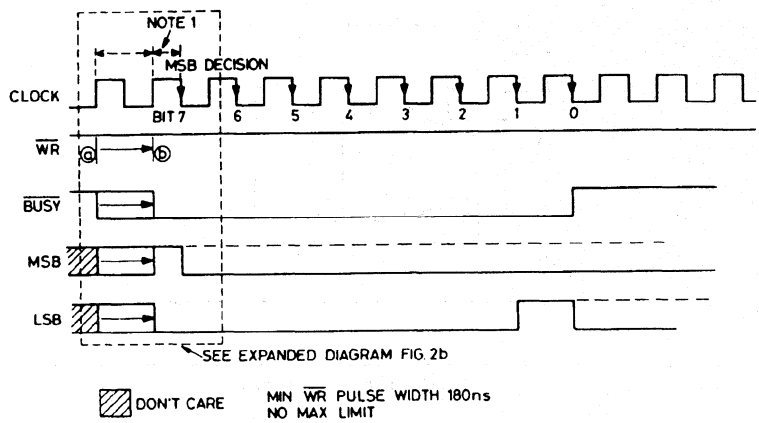


Fig. 2a

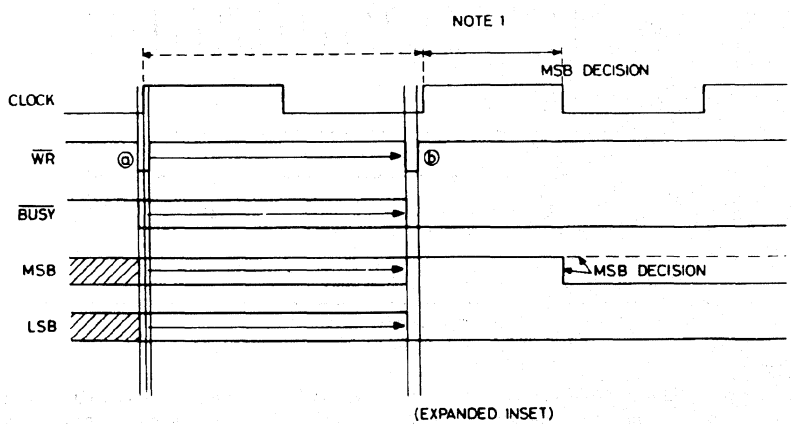


Fig. 2b

Fig.3 ZN448/9 timing diagram

If a free-running conversion is required, then the converter can be made to cycle by inverting the $\overline{BUSY}$ output and feeding it to $\overline{WR}$. To ensure that the converter starts reliably after power-up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive-going pulse which can be derived from a simple RC network that gives a single pulse when power is applied, as shown in Fig.4a.

The ADC will complete a conversion on every eighth clock pulse, with the $\overline{BUSY}$ output going high for a period determined by the propagation delay of the NOR gate, during which time the data can be stored in a latch. The time available for storing data can be increased by inserting delays into the inverter path.

A timing diagram for the continuous conversion mode is shown in Fig.3b.

As the $\overline{BUSY}$ output uses a passive pull-up the rise time of this output depends on the RC time constant of the pull-up resistor and load capacitance. In the continuous conversion mode the use of a 4k7 external pull-up resistor is recommended to reduce the risetime and ensure that a logic 1 level is reached.

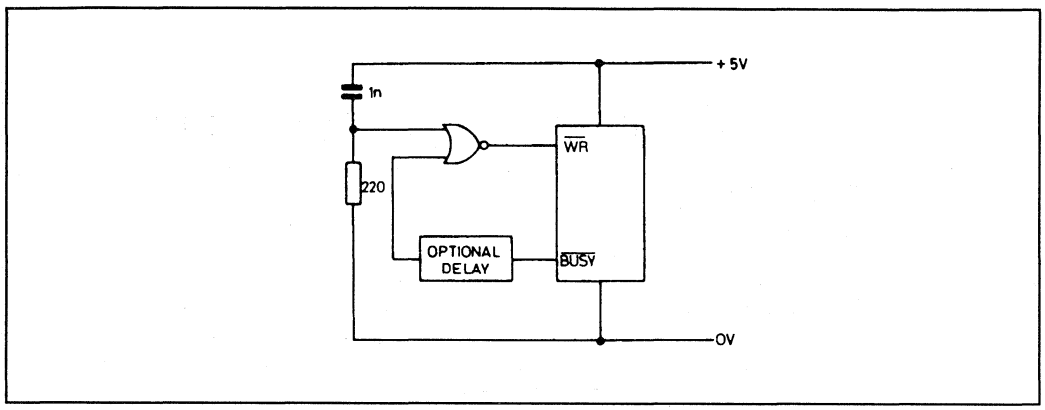


Fig.4a Circuit for continuous conversion

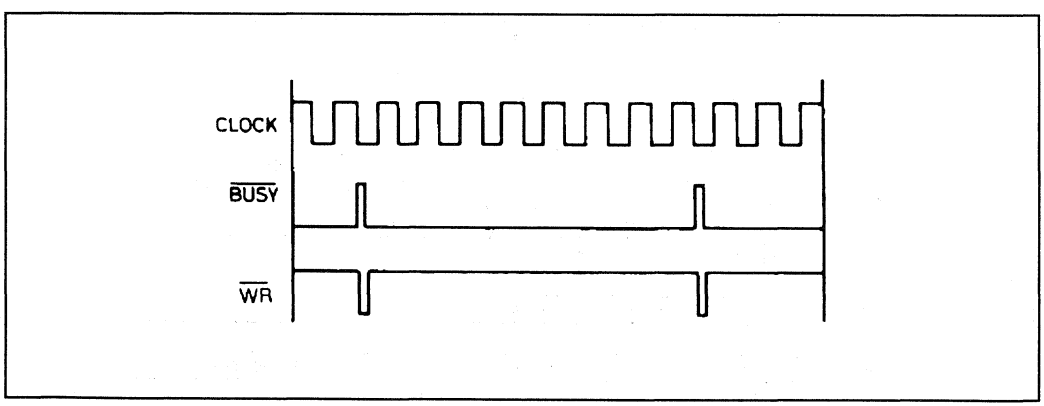


Fig.4b Timing for continuous conversion

DATA OUTPUTS

The data outputs are provided with three-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig.5. Whilst the $\overline{RD}$ input is high both output transistors are turned off and the ZN448/9 presents only a high impedance load to the bus.

When $\overline{RD}$ is low the data outputs will assume the logic states present at the outputs of the successive register.

A test circuit and timing diagram for the output enable/disable delays are given in Fig.6.

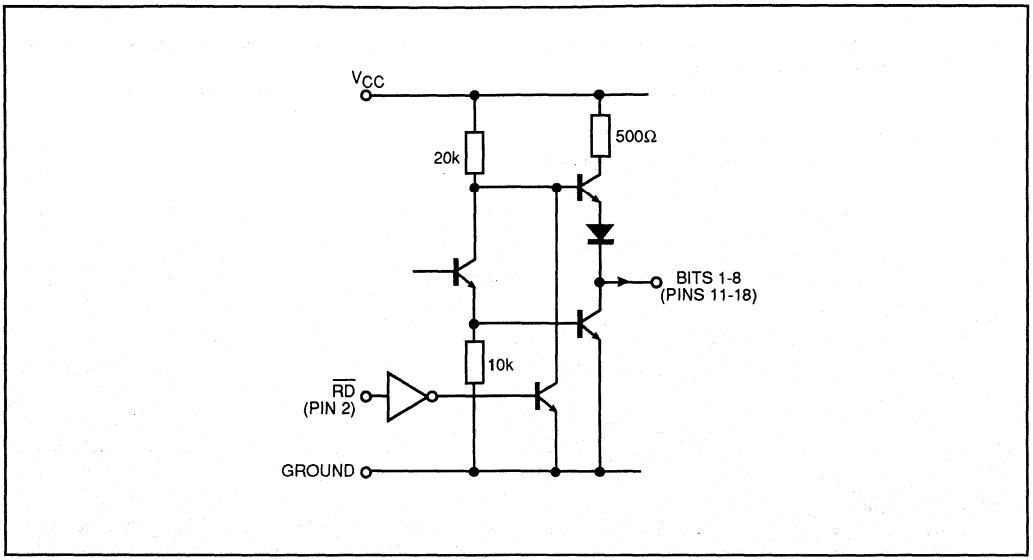


Fig.5 Data output

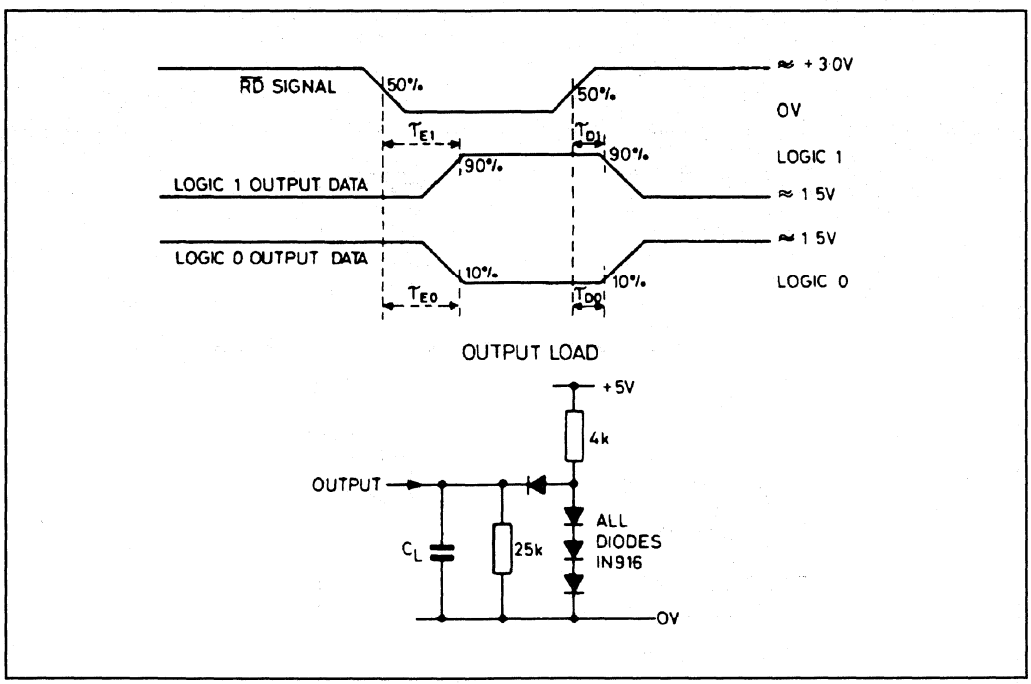


Fig.6 Output enable/disable delays

$\overline{\text{BUSY}}$ OUTPUT

The $\overline{\text{BUSY}}$ output, shown in Fig.7, utilises a passive pull-up for CMOS/TTL compatibility. This allows up to four $\overline{\text{BUSY}}$ outputs to be wire-ANDed together to form a common interrupt line.

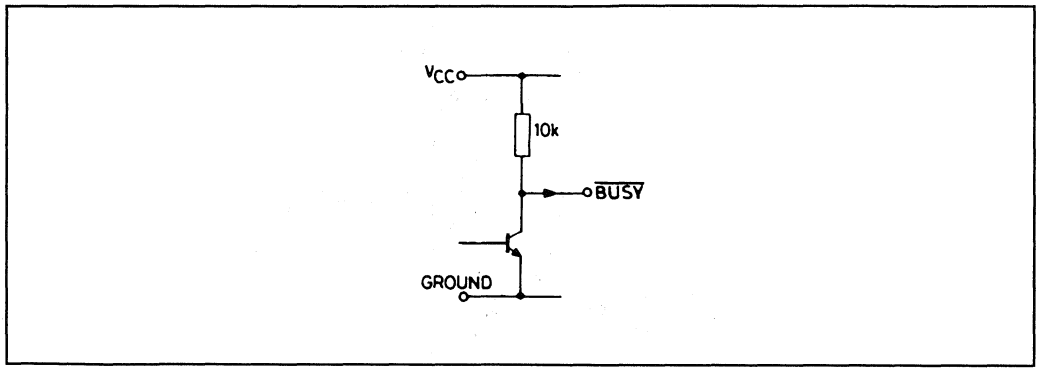


Fig.7 $\overline{\text{BUSY}}$ output

ON-CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 3 and ground, as shown in Fig.8a. A graph of typical oscillator frequency versus capacitance is given in Fig.9. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in Fig.8b. However, due to processing tolerance, the absolute clock frequency may vary considerably between devices. For optimum accuracy and stability of the oscillator frequency, it may be possible to use a crystal or ceramic resonator with suitable load components, as shown in Fig.8c. The final option is to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate, as shown in Fig.8d.

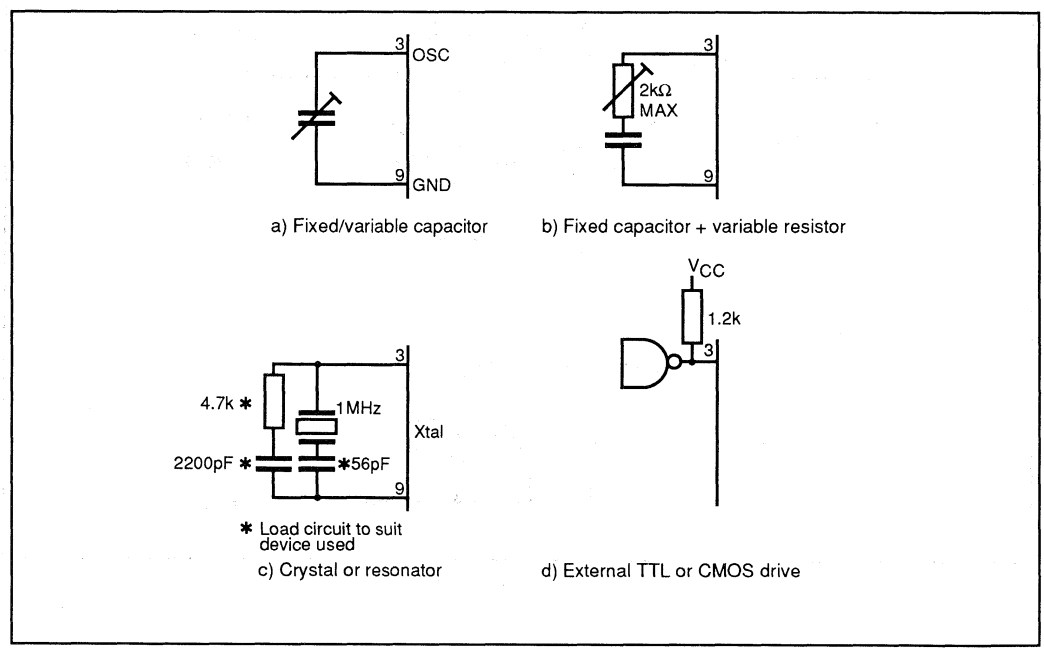


Fig.8 Clock circuit external components

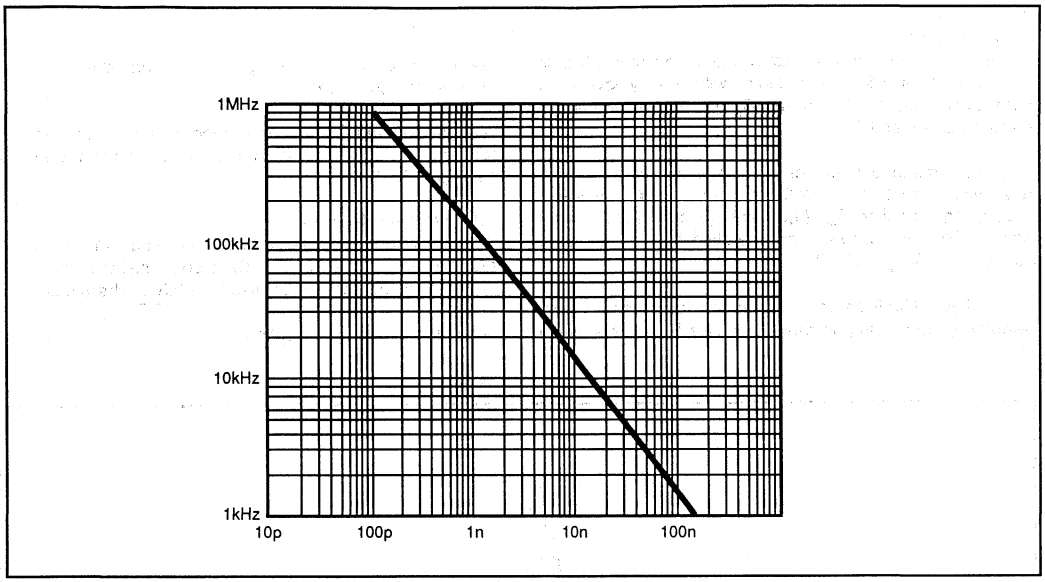


Fig.9 Typical clock frequency v C_{CK} (R_{CK} = 0)

ANALOG CIRCUITS

D-A converter

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig.10. Each element is connected to either 0V or $V_{REF\,IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

D to A output = $\frac{n}{256}(V_{REF\,IN} - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8μV/°C) the effect on accuracy will be neglible.

The D-A output range can be considered to be 0 - $V_{REF\,IN}$ through an output resistance R (4k).

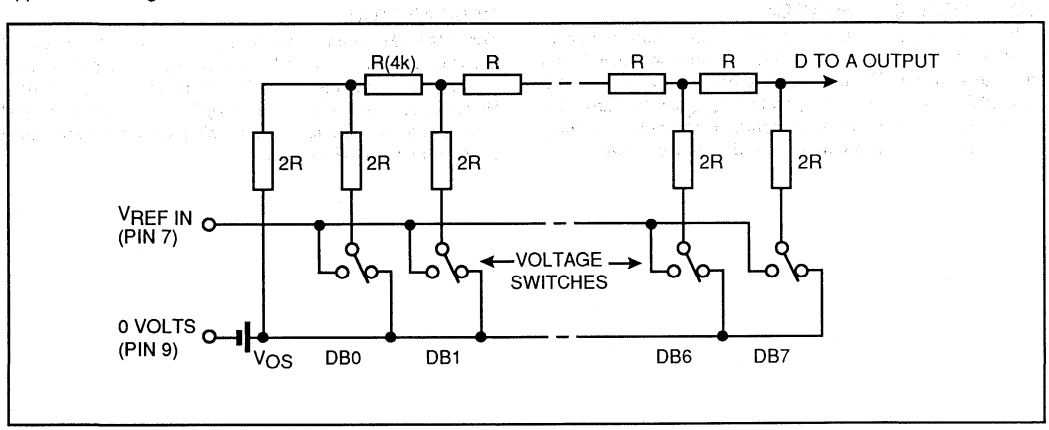


Fig.10 R-2R ladder network

REFERENCE

(a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.11). A Resistor (R_{REF}) should be connected between pins 8 and 10.

The recommended value of 390Ω will supply a nominal reference current of (5 - 2.5)/0.39=6.4mA. A stabilising/ decoupling capacitor, C_{REF} (4μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (pin 8) is connected to $V_{REF\ IN}$ (pin 7).

UP to five ZN448/9's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

(b) External reference

If required an external reference in the range +1.5 to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

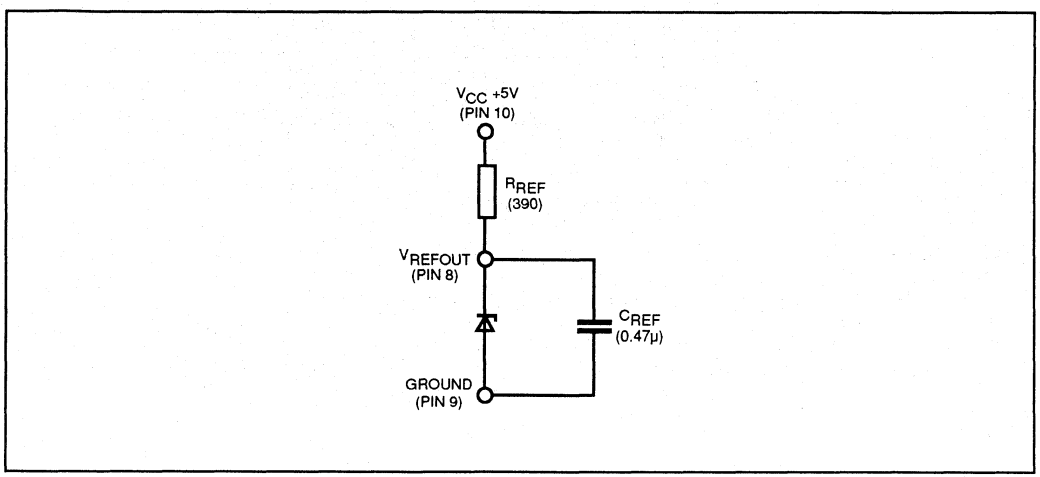


Fig.11 Internal voltage reference

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN4448/9 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN448/9 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN448/9 contains a fast comparator, the equivalent input circuit of which is shown in Fig.12. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150μA and need not be well stabilised it can be supplied by a simple diode pump circuit driven from the $\overline{BUSY}$ output.

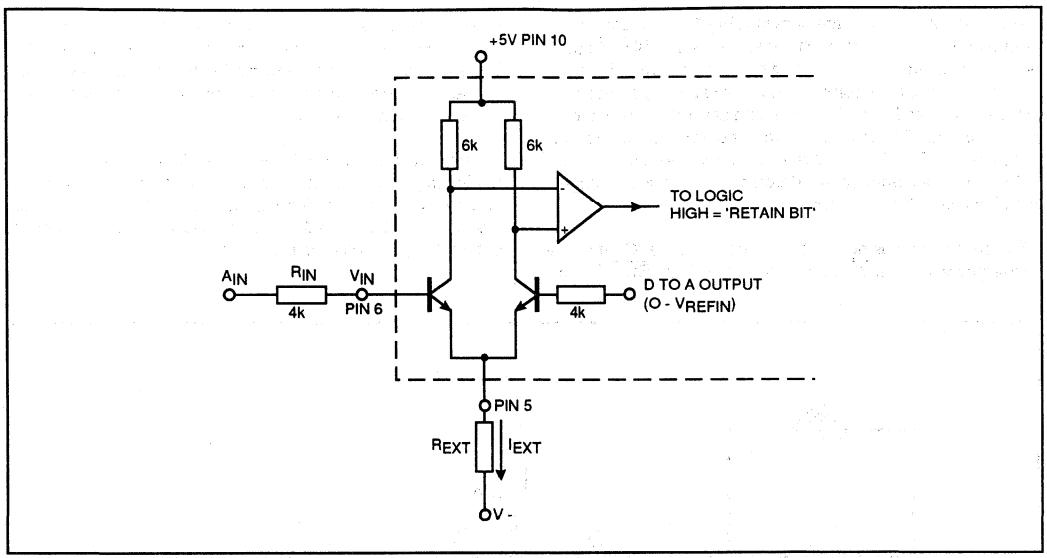


Fig.12 Comparator equivalent circuit

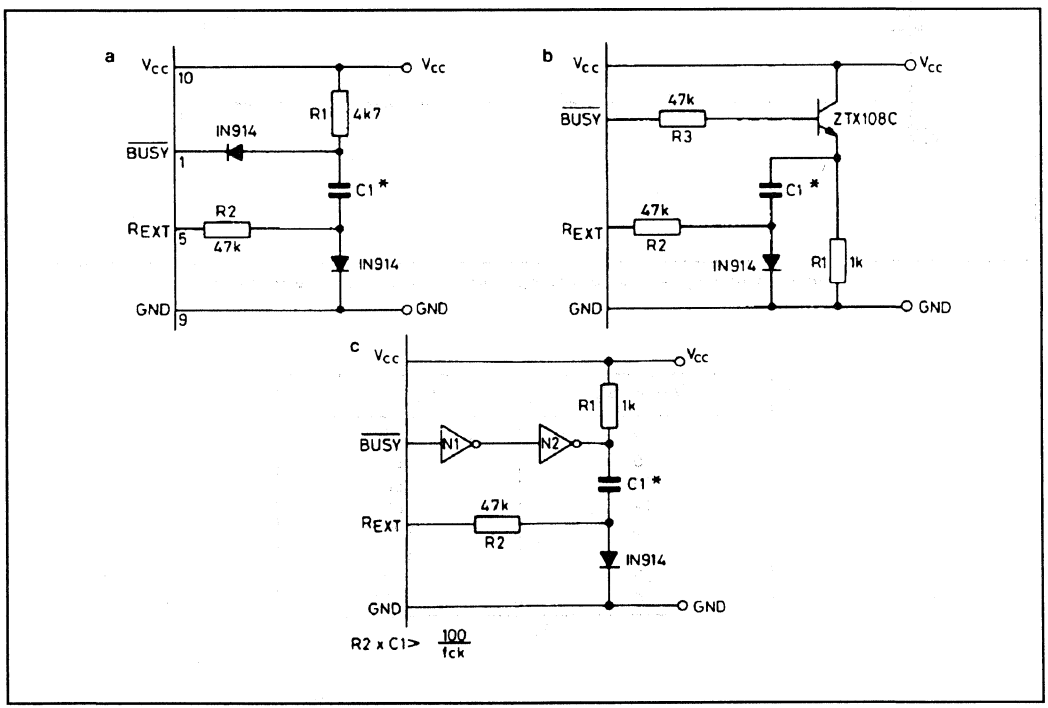


Fig.13 Diode pump circuits to supply comparator tail current

Several suitable circuits are shown in Fig.13. The principle of operation is the same in each case. Whilst the $\overline{BUSY}$ output is high, capacitor C1 is charged to about 4-4.5V. During a conversion the $\overline{BUSY}$ output goes low and the upper end of C1 is thus also pulled low. The lower end of C1 therefore applies about -4V to R2, thus providing the tail current for the comparator. The time constant R2. C1 is chosen according to the clock frequency so that droop of the capacitor voltage is not significant during a conversion.

The constraint on using this type of circuit is that C1 must be recharged whilst the $\overline{BUSY}$ output is high. If the $\overline{BUSY}$ output is high for greater than one converter clock period then the circuit of Fig.13a will suffice. If this is not the case, for example, in the continuous conversion mode, then the circuits of Figs. 13b and 13c are recommended, since these can pump more current into the capacitor.

Where several ZN448/9's are used in a system the self-oscillating diode pump circuit Fig.14 is recommeded. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistor values for different supply voltages is given in Table 1.

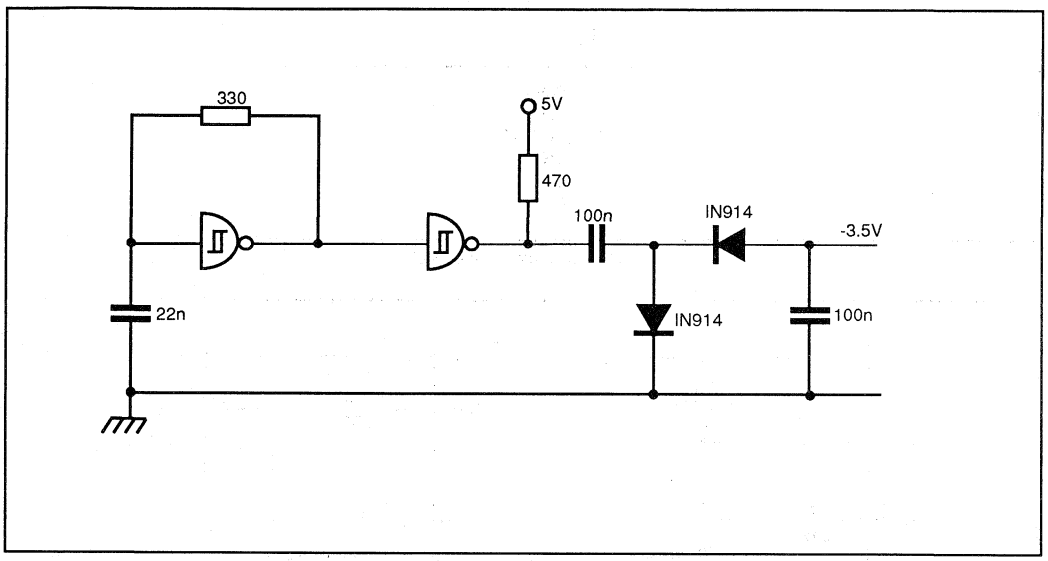


Fig.14 Diode pump circuit to supply comparator tail current for up to five ZN448/9's

V – (volts)	R_{EXT} (kΩ)
3	47
5	82
10	150
12	180
15	220
20	330
25	390
30	470

Table 1

ANALOG INPUT RANGES

The basic connection of the ZN448/9 shown in Fig.15 has an analogue input range 0 to $V_{REF\,IN}$ which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input input range so that the comparator always sees a positive input voltage.

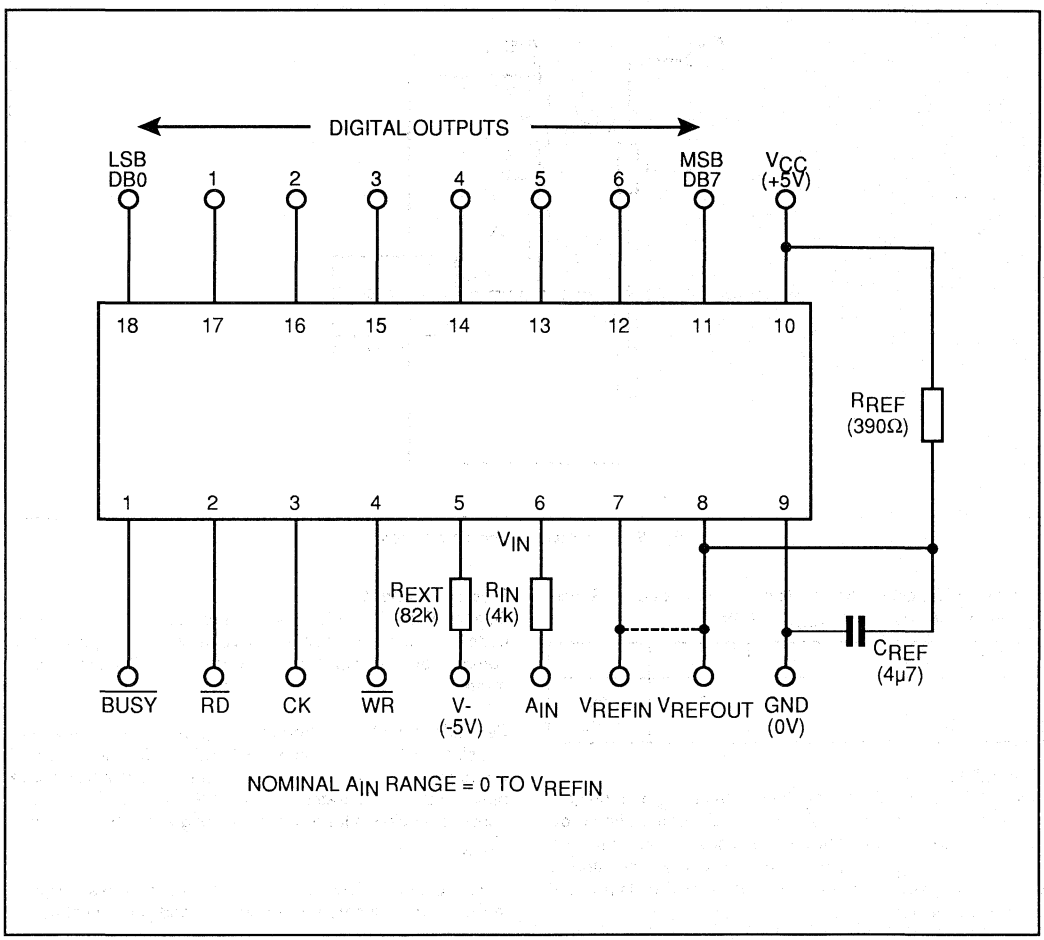


Fig.15 External components for basic operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig.16.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the analog input (A_{IN}) is at full-scale.

The resulting full-scale range is given by:

$$A_{IN}FS = \left(1 + \frac{R_1}{R_2}\right),\ V_{REF\ IN} = G.V_{REF\ IN}.$$

To match the ladder resistance R_1/R_2 (R_{IN}) = 4k.

The required nominal values of R_1 and R_2 are given by R_1 = 4Gk, $R_2 = \frac{4G}{G-1}$ k

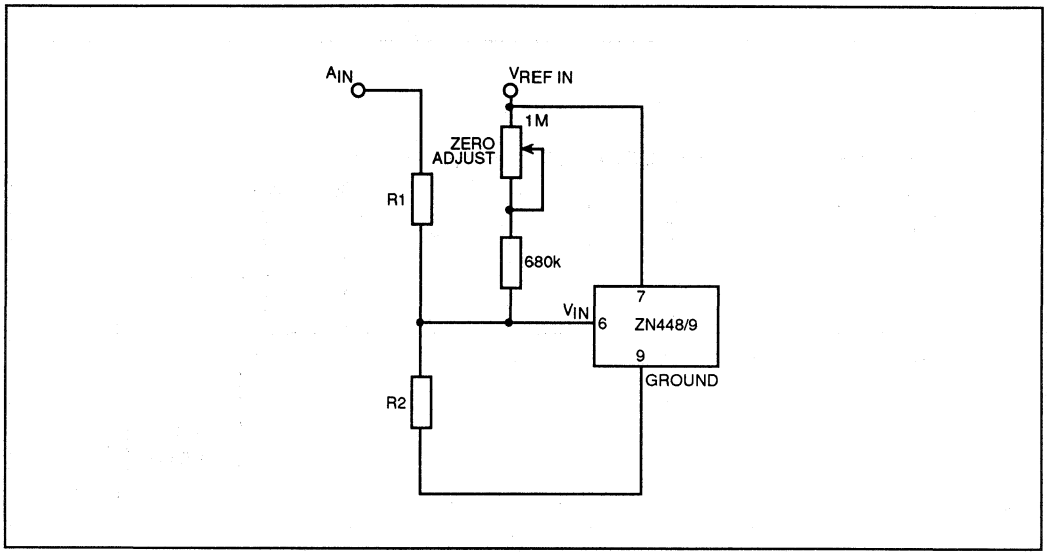


Fig.16 General unipolar input connections

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5V.

Input range	G	R_1	R_2
+5V	2	8k	8k
+10V	4	16k	5.33k

Gain adjustment

Due to tolerance in R_1 and R_2, tolerance in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

Zero adjustment

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which correpsonds to 1.5LSB with a 2.56V reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of +0.5LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1.5 times $V_{REF\ IN}$.

Practical circuit values for +5 and +10V input ranges are given in Fig.17, which incorporates both zero and gain adjustments.

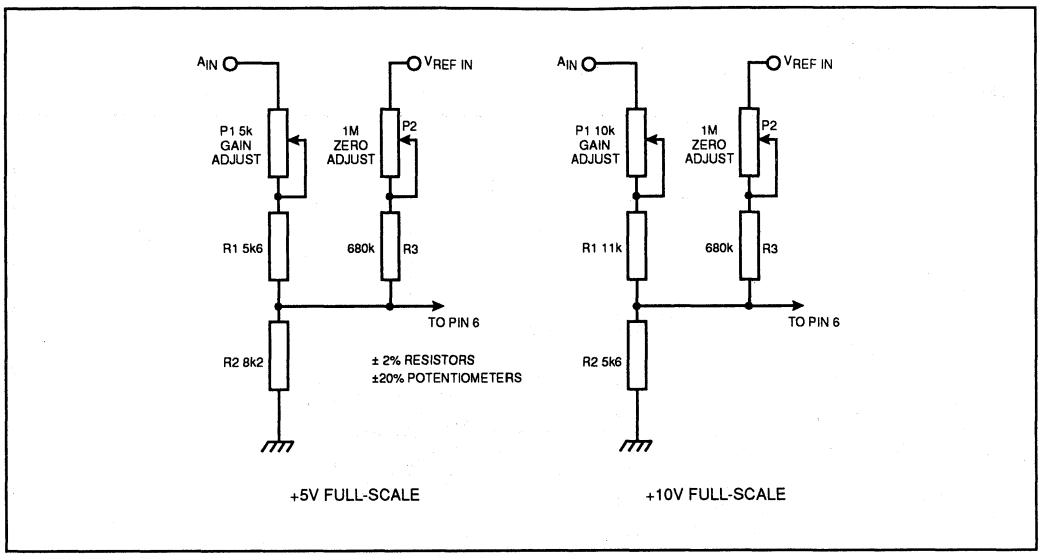


Fig.17 Unipolar operation component values

Unipolar adjustment prodedure

(i) Apply continuous convert pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full-scale minus 1.5LSB to A_{IN} and adjust off-set until the bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply 0.5LSB to A_{IN} and adjust zero until 8 bit just flickers between 0 and 1 with all other bits at 1.

Unipolar setting up points

Input range, +FS	0.5LSB	FS - 1.5LSB
+5V	9.8mV	4.9707V
+10V	19.5mV	9.9414V

$$1LSB = \frac{FS}{256}$$

Bipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (offset binary)
FS - 1LSB	11111111
FS - 2LSB	11111110
0.75FS	11000000
0.5FS + 1LSB	10000001
0.5FS	10000000
0.5FS - 1LSB	01111111
0.25FS	01000000
1LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN448/9 is offset by half full-scale by connecting a resistor R_3 between $V_{REF\,IN}$ and V_{IN} (Fig.18).

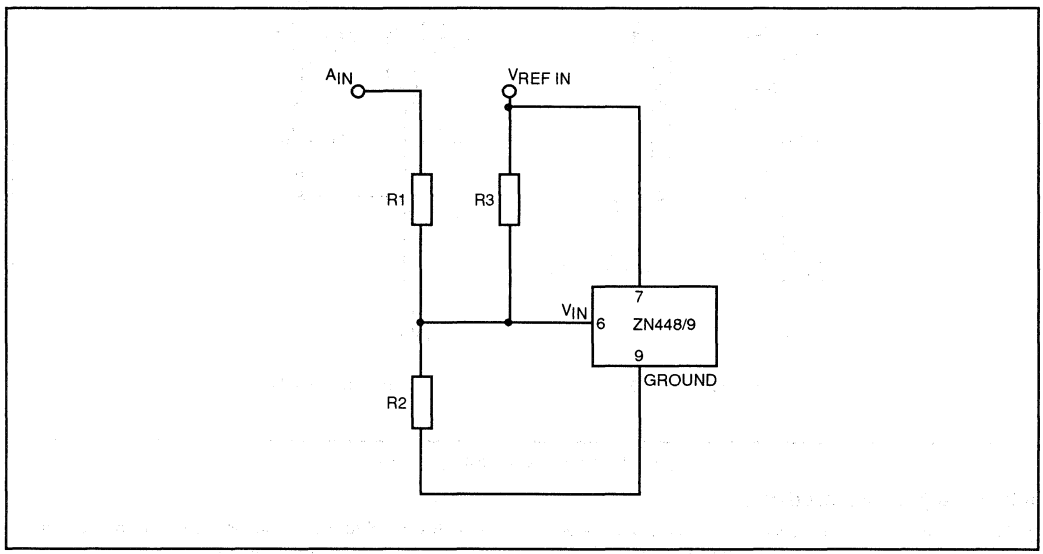


Fig.18 Basic bipolar input connection

When A_{IN} = -FS, V_{IN} needs to be equal to zero.

When A_{IN} = +FS, V_{IN} needs to be equal to $V_{REF\,IN}$.

If the full-scale range is $\pm$ G. $V_{REF\,IN}$ then R_1 = (G - 1). R_2 and R_1 = G. R_3 fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ (=R_{IN}) = 4k.

Thus the nominal values of R_1, R_2, R_3 are given by R_1 = 8 Gk, R_2 = 8G/(G - 1)k, R_3 = 8k.

A bipolar range of $\pm V_{REF\,IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\,IN}$) results if $R_1 = R_3$ = 8k and $R_2 = \infty$.

Assuming the $V_{REF\,IN}$ = 2.5V the nominal values of resistors for $\pm$5 and $\pm$10V input ranges are given in the following table.

Input range	G	R_1	R_2	R_3
+5V	2	16k	16k	8k
+10V	4	32k	10.66k	8k

Minus full-scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full-scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig.19.

Note that in the $\pm$5V case R_3 has been chosen as 7.5k (instead of 8.2k) to obtain a more symmetrical range of adjustment using standard potentiometers.

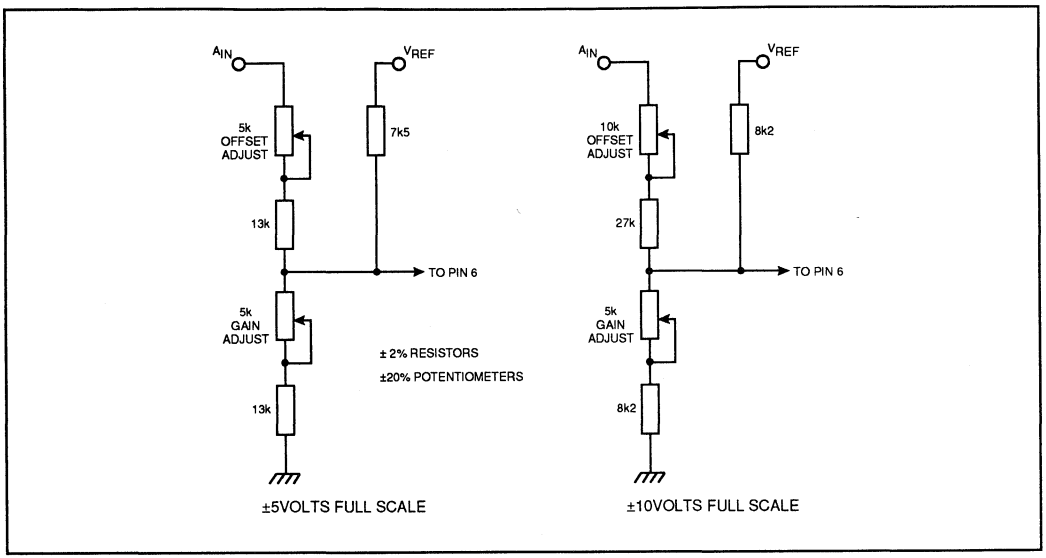


Fig.19 Bipolar operation component values

Bipolar adjustment prodedure

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply -(FS -0.5LSB) to A_{IN} and adjust off-set until the bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS -1.5LSB) to A_{IN} and adjust gain until the 8 bit just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

Bipolar setting up points

Input range, ±FS	-(FS -0.5LSB)	+(FS -1.5LSB)
+5V	-4.9805V	+4.9414V
+10V	-9.9609V	+9.8828V

$$1LSB = \frac{2FS}{256}$$

Bipolar logic coding

Analogue input (A_{IN}) (Nominal code centre value)	Output code (offset binary)
+(FS - 1LSB)	11111111
+(FS - 2LSB)	11111110
+0.5FS	11000000
+1LSB	10000001
0	10000000
-1LSB	01111111
-0.5FS	01000000
-(FS - 1LSB)	00000001
-FS	00000000

Section 4

Video and High Speed ADCs

SP973T8

30MHz 8-BIT FLASH ADC (TTL/CMOS OUTPUTS)

The SP973T8 is a wideband, full flash analog-to-digital converter that requires no preceding sample and hold. The device contains a full 8-bit D-type latch which ensures that the 8 TTL/CMOS outputs are accurately registered and have a good data valid time at high clock speeds.

Operating from a single +5 volt supply the device is capable of conversion rates well in excess of 30MHz and its wideband input allows signals with frequencies up to the Nyquist limit to be digitised with high accuracy. An internal bandgap voltage regulator gives low DC drift over a wide operating temperature range.

The SP973T8 is designed for applications where power consumption and package size is at a premium.

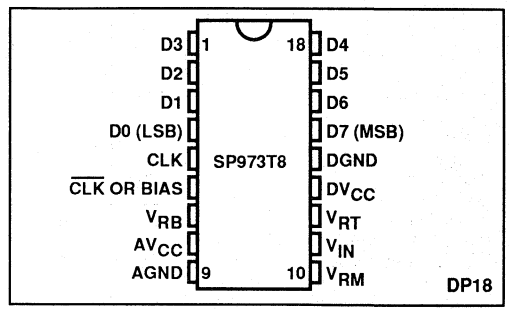


Fig.1 Pin connections - top view

FEATURES

- Flash Converter, No Sample and Hold Required
- Wideband Analog Input 70MHz, 3dB (Typ.)
- Low Power Consumption (600mW Typ.)
- Latched TTL/CMOS Compatible Outputs
- No Missing Codes - Guaranteed
- Designed for Wideband Operation
- Single 5V Supply
- Production Tested at 30MHz

ORDERING INFORMATION

SP973T8 C DP (Commercial - Plastic DIL package)

APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	7V
Output Current	10mA
Input Voltage, V_{IN}	V_{CC}
Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C

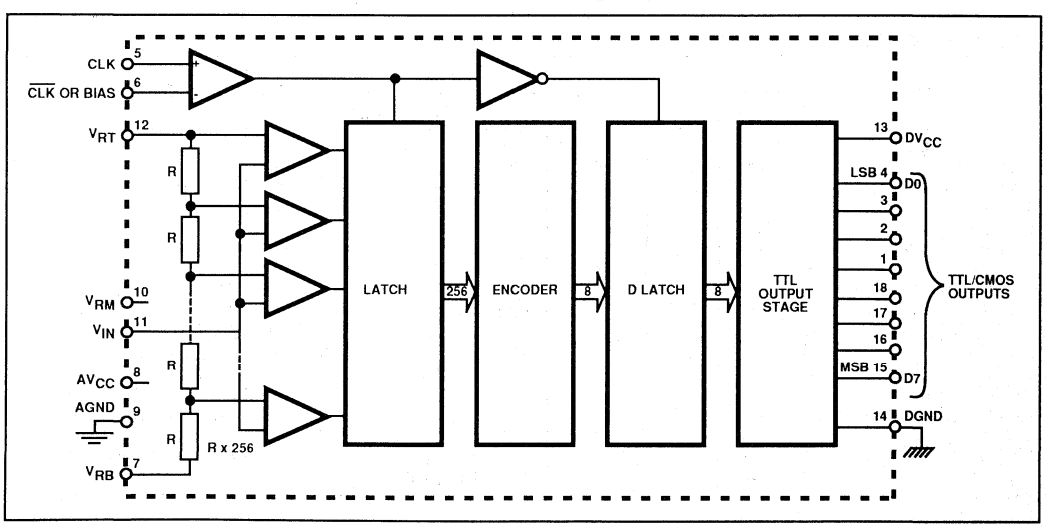


Fig.2 Internal block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{amb} = 25°C, V_{CC} = +5V ± 0.25V

Full temperature range = 0°C to +70°C

DC CHARACTERISTICS

Characteristic	Symbol	Temp.	Test level	Value			Units	Conditions
				Min.	Typ.	Max.		
Power Supply								
Supply current	I_{CC}	Full	4	100		140	mA	
		25	1	110	120	130	mA	
Power dissipation	P_D	Full	4	475		735	mW	
		25	1	520	600	680	mW	
Analog Input								
Input range	V_{IN}	Full	4	1.8		V_{CC}-0.7	V	
Input bias current	I_{IN}	25	1	150	390	1100	µA	$V_{IN} = V_{RT}$
3dB bandwidth	f_{3db}	25	4		70		MHz	
Input capacitance	C_{IN}	25	4		30		pF	
Reference Ladder								
Ladder resistance	R_D	25	1	325	440	550	Ω	
Ladder voltage (top)	V_{RT}	Full	4		4.3	V_{CC}-0.7	V	
Ladder voltage (bottom)	V_{RB}	Full	4	1.8	2.3		V	
Ladder offset (top)	V_{RTO}	25	5		-4		mV	
Ladder offset (bottom)	V_{RBO}	25	5		+3		mV	
Ladder temp. coeff.	R_{TC}	Full	5		1.5		Ω/°C	
Clock Input								
Logic '1' voltage	V_{IH}	Full	4	2.75	4.3	V_{CC}	V	A swing of 1V centred on the voltage applied to the $\overline{CLK}$ pin
Logic '1' current	I_{IH}	25	1			25	µA	
Logic '0' voltage	V_{IL}	Full	4	1.75	3.3	V_{CC}-1.0	V	
Logic '0' current	I_{IL}	25	1			2	µA	
Digital Outputs								
Logic '1' voltage	V_{OH}	Full	4	3.3			V	Into Standard LS TTL Load
		25	1	3.5	3.8		V	
Logic '0' voltage	V_{OL}	Full	4			0.4	V	
		25	1		0.1	0.4	V	
Static performance								
Differential non-linearity	DNL	Full	4			±1	LSB	
		25	4			±0.5	LSB	
Integral non-linearity	INL	Full	4			±1	LSB	
		25	4			±1	LSB	

AC CHARACTERISTICS (Refer to Fig.7)

Characteristic	Symbol	Temp.	Test level	Value			Units	Conditions
				Min.	Typ.	Max.		
Clock min. high	t_{PW1}	25	4	10			ns	
Clock min. low	t_{PW0}	25	4	10			ns	
Max. conversion rate		Full	4	30	50		MHz	A_{IN} = 15MHz at FS
Aperture delay	t_{AD}	25	5		3		ns	
Output data delay	t_D	25	4		7		ns	
Output rise time	t_R	25	4		6		ns	
output fall time	t_F	25	4		8		ns	
Dynamic Performance								With F_{CLK} = 30MHz
Differential non-linearity	DNL	25	1	-0.85	±0.5	+1	LSB	$A_{IN\,MAX}$ = 10MHz at FS
Integral non-linearity	INL	25	1		±1	±2	LSB	$A_{IN\,MAX}$ = 10MHz at FS
S/N ratio	SNR	25	1	40.9	44.5		dBc	$A_{IN\,MAX}$ = 1MHz at FS
			4		44.1		dBc	$A_{IN\,MAX}$ = 5MHz at FS
			4		43.3		dBc	$A_{IN\,MAX}$ = 10MHz at FS
Effective No. of bits	ENOB	25	1	6.5	7.1		bits	$A_{IN\,MAX}$ = 1MHz at FS
			4		7.0		bits	$A_{IN\,MAX}$ = 5MHz at FS
			4		6.9		bits	$A_{IN\,MAX}$ = 10MHz at FS
Bit Error Rate	BER	25	4		1 in 10^9			

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis is 3dB down on the DC level.

Aperture Delay

The delay between the falling edge of the CLOCK signal and the instant at which the analog input is sampled.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency. In this case it is the number of codes occuring outside the histogram cusp for a $^3/_4$ F.S. sinewave.

Differential Non-Linearity (DNL)

The deviation of any code width from an ideal 1LSB step.

Effective Number of Bits (ENOB)

This is a measure of the dynamic performance and is calculated from the following expression.

$$ENOB = \frac{SNR-1.76}{6.02}$$

SNR is the signal-to-noise ratio, in decibels, at the test frequency.

Integral Non-Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Output Data Delay

The delay between the 50% point of the falling edge of the clock signal and the 50% point of any data output change.

Reference Ladder Offset

The voltage error at the ends of the resistor chain caused by the lead frame and bond wire.

Signal-to-Noise Ratio (SNR)

The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components including harmonics but excluding DC with a full scale analog input signal.

Test Levels

Level 1 - 100% production tested
Level 2 - 100% production tested at 25°C and sample tested at specified temperatures
Level 3 - Sample tested only
Level 4 - Parameter is guaranteed by design and characteristics testing
Level 5 - Parameter is a typical value only

PIN DESCRIPTIONS

Pin No.	Function	Description
1, 2, 3, 4	D3, D2, D1, D0	Output data bits 3, 2, 1, 0
5	CLK	Clock input pin
6	$\overline{CLK}$	Clock threshold level pin
7	V_{RB}	Bottom of reference resistor chain
8	AV_{CC}	} 5 Volt power to all circuitry except the TTL output
9	AGND	}
10	V_{RM}	Middle of reference resistor chain
11	V_{IN}	Analog input voltage pin
12	V_{RT}	Top of reference resistor chain
13	DV_{CC}	} 5 Volt power supply to the TTL output stage
14	DGND	}
15	D7	Most significant bit (output data bit 7)
16, 17, 18	D6, D5, D4	Output data bits 6, 5, 4

RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}	+5.0V
Reference V_{RT}	+4.3V
Reference V_{RB}	+2.3V
AV_{CC} to DV_{CC}	0mV
AGND to DGND	0mV
Analog Input V_{IN}	2 Vp-p max

THERMAL CHARACTERISTICS

	DP	
Thermal resistance, chip-to-case θ_{jc}	20	°C/W
Thermal resistance, chip-to-ambient θ_{jA}	75	°C/W

APPLICATION NOTES

Analog Input Pin (Fig.3)

The analog input of the SP973T8 is connected to 256 comparators which have a combined capacitance of about 30pF. The sample/latch operation of the comparators causes the input capacitance to vary slightly as the comparator input transistors turn on/off. For this reason the input driver circuit should provide a low impedance signal to keep the harmonic distortion levels of the driver to a minimum.

The maximum amplitude of the analog input is defined by the setting of the two reference voltages V_{RT} and V_{RB}. Optimum performance will be obtained with the input signal biased midway between V_{RT} and V_{RB} with a peak to peak amplitude of V_{RT}-V_{RB}. The SP973T8 has excellent overload tracking of input signals with amplitudes greater than V_{RT}-V_{RB}, and will not be damaged if the absolute maximum ratings are adhered to.

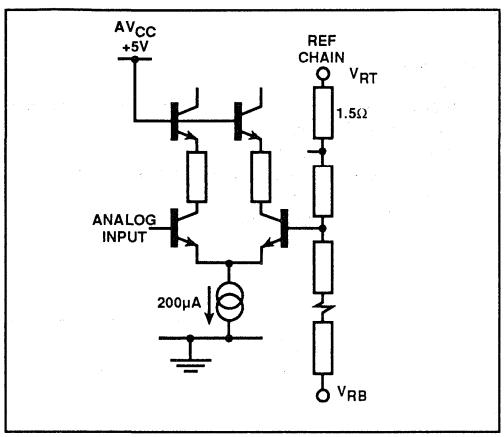


Fig.3 One of 255 analog inputs connected to pin 11

Voltage Reference Pins (Fig.4)

The SP973T8 converts analog signals in the range V_{RB}<V_{IN}<V_{RT} into digital format, where V_{RB} produces code 0 and V_{RT} produces code 255. Between the pins V_{RT} and V_{RB} are a series of 256 resistors forming a reference chain with a total resistance of 425Ω (typically). The centre point of the reference chain is also connected to an external pin named V_{RM} by which it is possible to provide precision trimming of the integral linearity of the device.

The maximum value of V_{RT} is V_{CC}-0.7 volts since values above this figure will start to saturate the comparator, resulting in noticeable distortion. Optimum performance from a +5 Volt power supply is obtained with V_{RT}<+4.3V and V_{RB} a further 2 volts below V_{RT}. In addition the V_{RT}, V_{RB} and V_{RM} pins should be decoupled to ground close to the device pins using good quality 10nf capacitors. A simple method for providing the reference voltages is shown in Fig.4, and further information may be found in applications note AN72. With a reference ladder voltage of less than 2V the reduced LSB size causes a larger differential linearity error. Operation of the device below 1.5V may therefore cause missing codes.

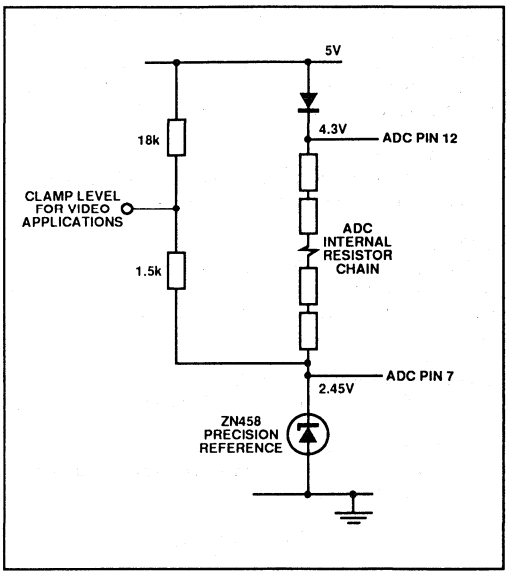


Fig.4 Simple reference voltage generation

TTL/CMOS Outputs (Fig.5)

The data output levels of the SP973T8 are TTL/CMOS compatible and switch from 0V to +4V. The output circuit is capable of operation at clock frequencies in excess of 60MHz when driving into a standard LSTTL load.

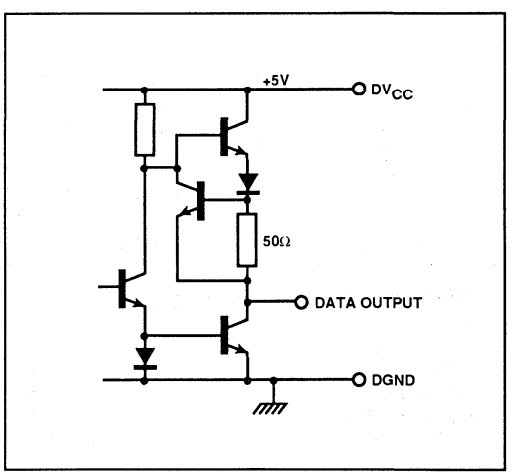


Fig.5 TTL output stage

Clock Input (Fig.6)

The SP973T8 will operate at clock frequencies up to and above 30MHz. The clock input has been designed to accept a 1Vpp signal, in either differential or single-ended mode, between the $V_{IH(MAX)}$ and $V_{IL(MIN)}$ levels indicated in the electrical specification. At $V_{IH(MAX)}$ or $V_{IL(MIN)}$ the $\overline{CLK}$ input will sink 800µA or source 3.2mA of current, respectively. (See Fig.6).

When used in single-ended operation, $\overline{CLK}$ may be decoupled to ground so that this input will then self-bias at approximately 1.2V below the supply Vcc. It may then be used to bias the $\overline{CLK}$ input, through a termination resistor, for AC-coupled applications as shown in Fig.8.

Alternatively a TTL level clock may be used by inserting an appropriate value resistor in series with the coupling capacitor.

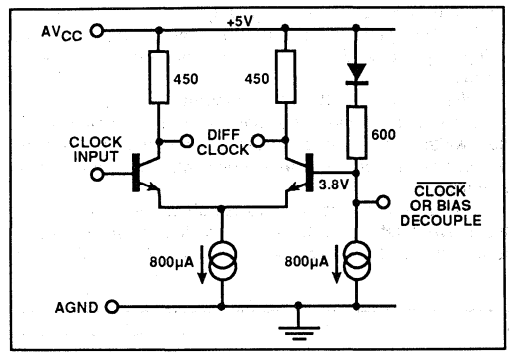


Fig.6 Clock input stage

TIMING (Fig.7)

The analog input is sampled by the SP973T8 approximately 3ns (t_{AD}) after the falling edge of the clock. Due to the pipeline operation of the device, a further one clock cycle is required to produce the output data. As shown in Fig.7, the output has a good data valid time, enabling the data to be latched at both the rising and falling edges of the clock.

However, for clock frequencies above 25MHz the clock-to-output delay time may lead to an inadequate data set up time relative to the rising clock edge and it is therefore recommended that the output data is latched on the falling clock edge.

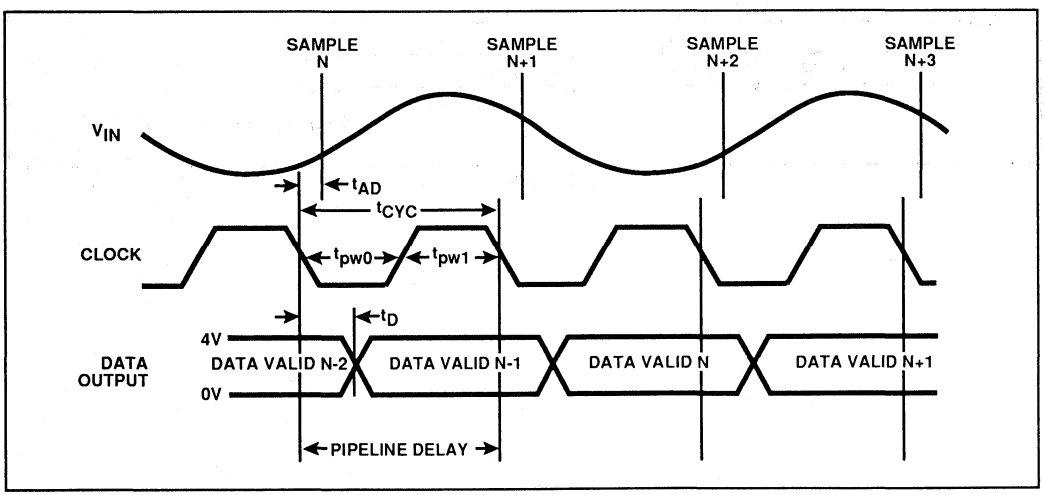


Fig.7 Timing diagram

Circuit Board Construction (Fig.8)

Excellent performance can be obtained from this ADC using only one solid ground plan for both analog and digital signals.

With all flash ADCs it is important to restrict digital crosstalk into the input, not only within the wanted signal bandwidth but also at frequencies between Nyquist and clock, as such signals will be aliased down into the wanted signal bandwidth.

We can give the designer two useful suggestions to reduce the above. First, due to the on-chip clock regeneration circuit, a low level clock can be fed to the ADC 1V p-p is recommended. The second suggestion is the addition of a small bead inductor in series with and close to the device analog input.

Supply line decoupling is very important when dealing with a mix of analog and digital signals as they can provide a source of digital feedback from the digital output currents. It is wise, therefore, to decouple the SP973T8 close to the device supply pins with good quality, high frequency, low inductance capacitors.

Due to the high clock rates involved, long clock lines to the device should be avoided to reduce the noise pick up.

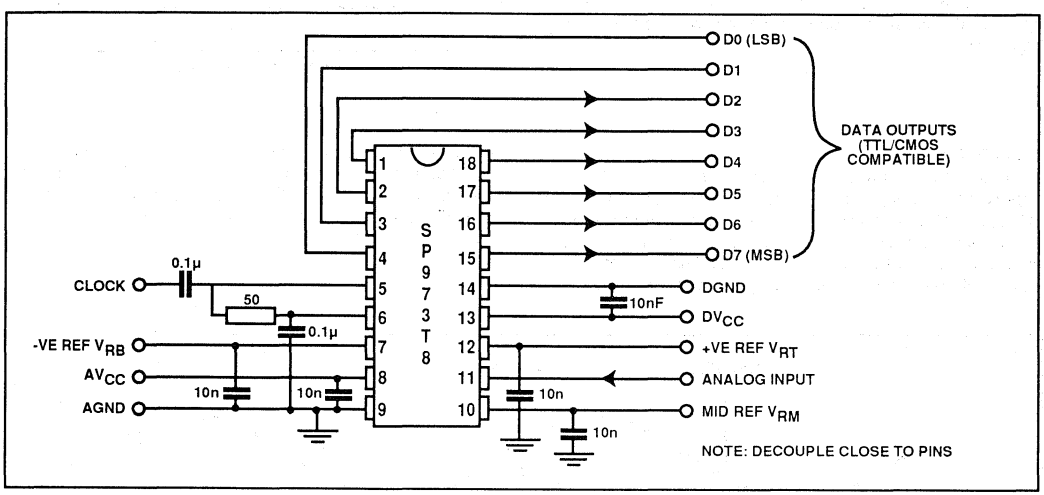


Fig.8 Test/application circuit

SP97504

HIGH SPEED FOUR BIT EXPANDABLE A TO D CONVERTER

The SP97504 is a fast 4-bit ECL A-D converter, expandable up to 8 bits without additional encoding circuitry. It has been designed to maintain high accuracy at high analog input frequencies.

It can convert at sample rates from DC to 110MHz, with analog inputs above Nyquist frequencies. All output levels are ECL compatible.

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous.

The SP97504 operates from a +5V, -7V supply.

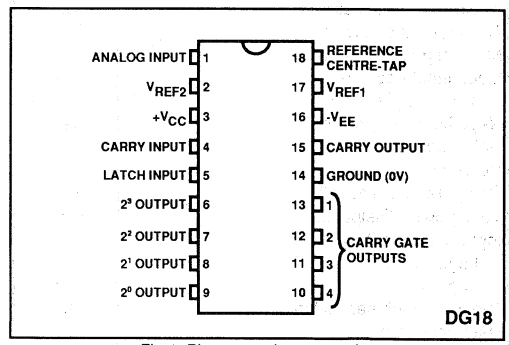


Fig.1 Pin connections - top view

FEATURES

- Operating Temperature Range -30°C to +85°C
- No External Components for 4-Bit Conversion
- 110MHz Conversion Rate
- On-Chip Encoding for Expansion to 8 Bits
- No External Sample and Hold Needed
- Bit Size 10-100mV
- Over 100MHz Full Power Bandwidth
- 10ps Aperture Uncertainty Time
- 8-Bit Accuracy (When Expanded)

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	-7.5V
Storage temperature range	-65°C to +150°C
Junction operating temperature	<175°C
Lead temperture (soldering 60 sec)	300°C

ORDERING INFORMATION

SP97504 DG (Industrial - Ceramic DIL package)

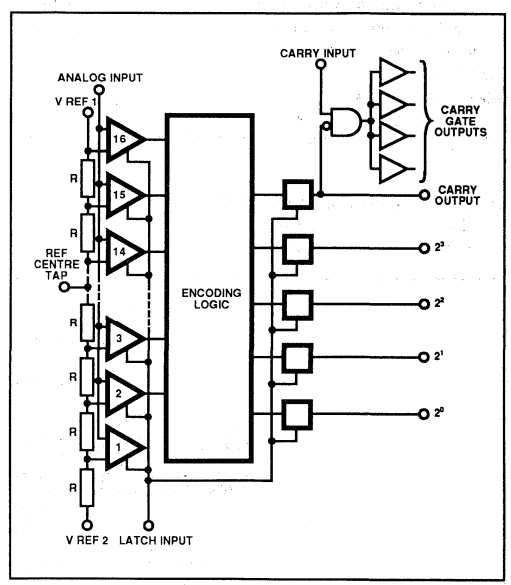


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{amb} = 25°C, V_{CC} = +5V ± 0.25V, V_{EE} = -7V ± 0.25V, R_L = 100Ω to -2V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analog input current	I_B		30	100	µA	V_{IN} = 0V
Analog input capacitance	C_{IN}		10		pF	
Common mode range	V_{CM}	-2		+2	V	
Maximum input slew rate			1000		V/µs	
Latch input capacitance	C_{IN}		2		pF	
Positive supply current	I_{CC}		72	92	mA	
Negative supply current	I_{EE}		75	96	mA	
Reference resistor chain			25		Ω	Total
Reference bit size		10		100	mV	
Comparator offset voltage	V_{OS}	-5		+5	mV	
Total power dissipation	P_{DISS}		935	1230	mW	All outputs loaded
Input and output logic levels						
Logic high	V_{OH}	-0.930		-0.720	V	For 100Ω load
Logic low	V_{OL}	-1.90		-1.620	V	to -2V
Minimum latch set-up time	ts		1.5	2	ns	10mV overdrive
Data uncertain			5		ns	<1mV overdrive
Latch to output propagation delay						
Latch enable to output high	t_{pd} + (E)		6	8	ns	} 10mV overdrive
Latch enable to output low	t_{pd} - (E)		5	8	ns	
Carry input to carry gate	t_{pd} (C)		3	5	ns	
O/P delay						
Maximum sample rate	$F_{C\,MAX}$	100	110		MHz	
Aperture uncertainty time	ta		10		ps	

THERMAL CHARACTERISTICS

θ_{JA}	90°C/W
θ_{JC}	20°C/W

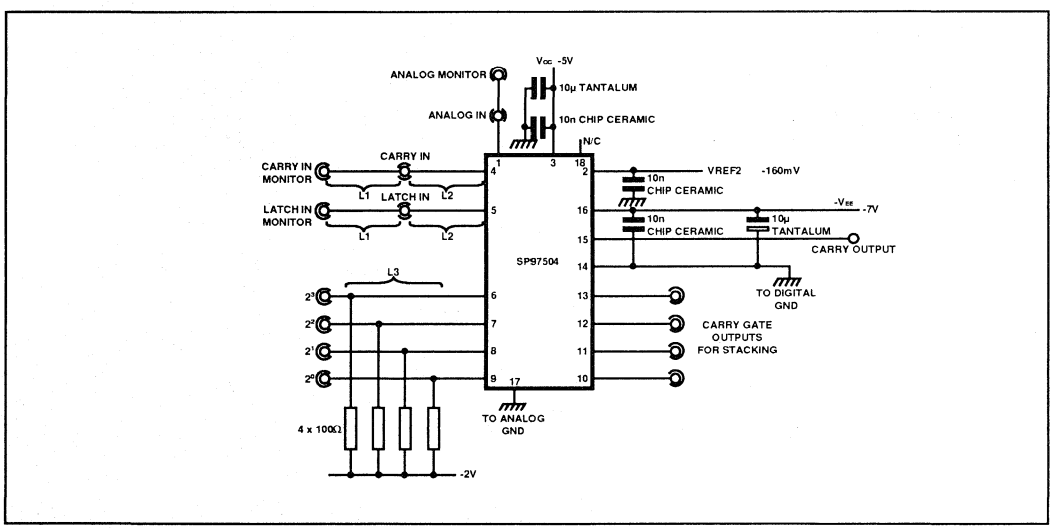


Fig.3 High frequency test circuit

PERFORMANCE CURVES

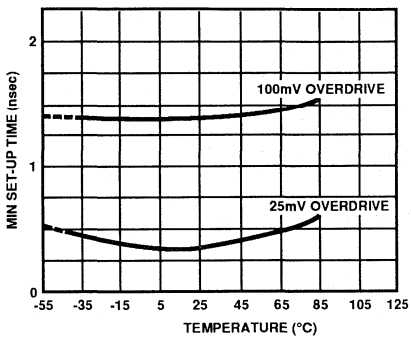


Fig.4 Set-up time as a function of temperature

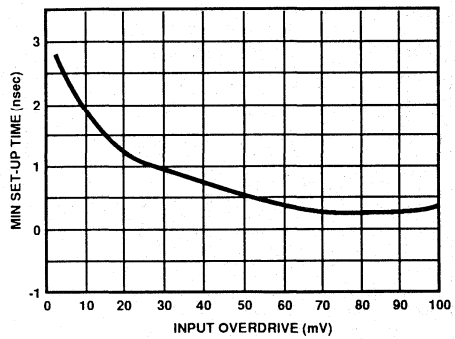


Fig.5 Set-up time as a function of overdrive

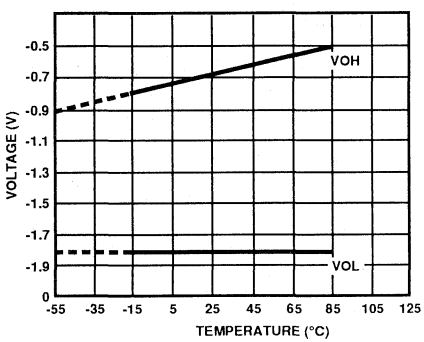


Fig.6 Output logic levels as a function of temperature

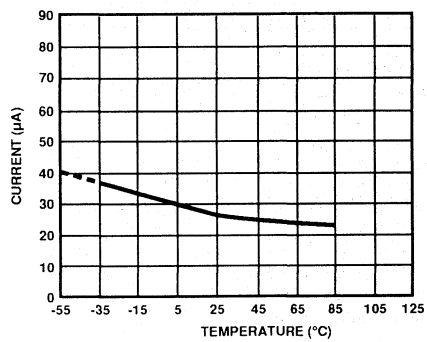


Fig.7 Analog input current as a function of temperature

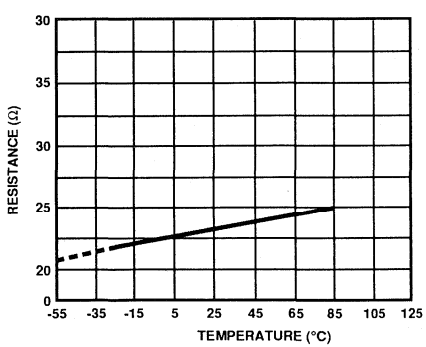


Fig.8 Network resistance as a function of temperature

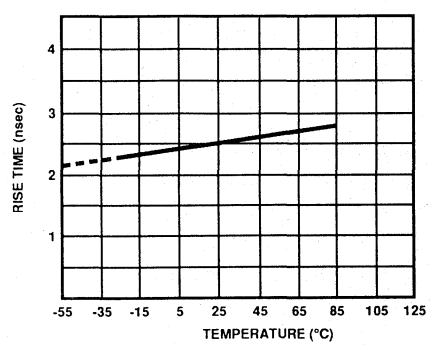


Fig.9 MSB output edge speeds as a function of temperature

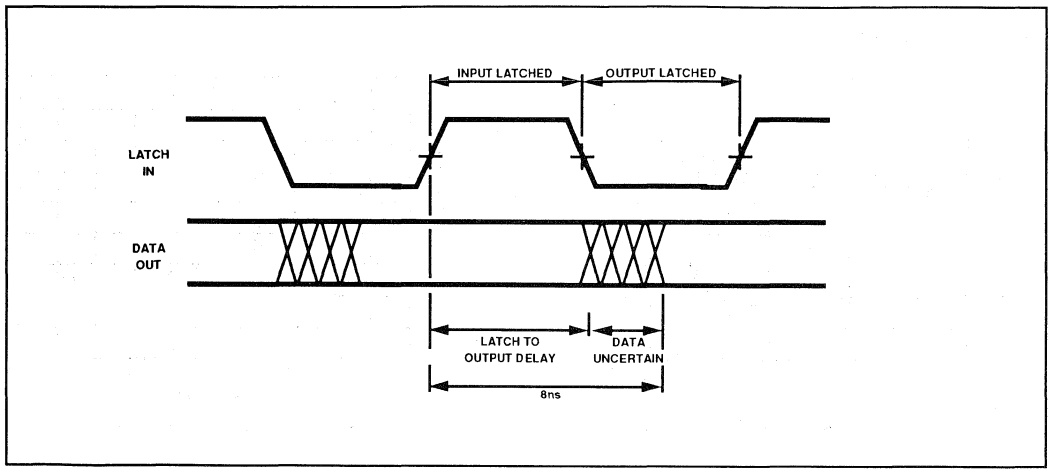


Fig.10 Timing diagram

OPERATING NOTES

1. Carry output (pin 15) is high when the analog input exceeds the top reference voltage (pin 17)

Then the carry gate outputs (pins 10 to 13) go low regardless of carry input (pin 4), when the analog input is between V_{REF} and V_{REF2} and the carry output is low. The carry gate output will be high if the carry input is also high. Similarly if the carry input is low then the carry gate outputs will be low.

2. When used in an ambient temperature in excess of 65°C the SP97504 must be provided with an external heatsink or forced air cooling. This will ensure that the junction temperature does not exceed 175°C.

APPLICATION NOTES

1. The SP97504 is ideally suited to subranging systems as it maintains good accuracy at low reference voltages. This enables the second rank to be driven at higher speed from the subtracting Op-Amp
2. For applications that require low bit error rates at high frequency, the clock signal should be adjusted for 60% ECL low, 40% ECL high mark to space ratio.
3. The SP97504 is ideally suited to applications in communication systems that incorporate multi-level coding (quadrature amplitude modulation).
4. The SP97504 requires a fast edge speed clock. Rise and fall times of <4ns are recommended.

SP97508

110MHz 8-BIT FLASH ADC

The SP97508 is an 8-bit flash ECL analog-to-digital converter. It incorporates 256 individual comparators, a reference chain and a full D-type output latch. The ADC is capable of sampling at 100MHz with full (Nyquist) analog bandwidth and has an excellent dynamic performance. A conventional unity mark/space ratio clock can be used and the output data can be programmed for true or inverse binary and twos' complement coding.

FEATURES

- Full Scale Input Bandwidth 120MHz (3dB)
- No Missing Codes
- Production Tested with 30MHz Analog Input
- Low Input Capacitance: 32pF (Max.)
- No External Sample and Hold Needed
- Low Power Consumption: 1.4W (Typ.)
- True/Inverse Binary and Twos' Complement Coding
- Operating Temperature Range: -40°C to +85°C

APPLICATIONS

- Radar Video Digitising
- Instrumentation
- Nucleonics
- Studio Quality Video

ORDERING INFORMATION

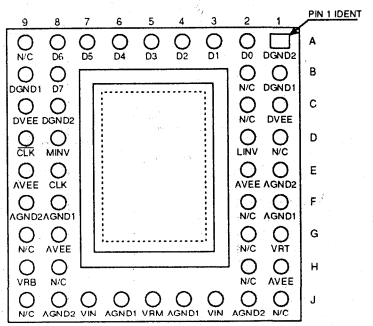
SP97508B HG (Industrial - J-Lead Quad Cerpac)
SP97508B AC (Industrial - Pin Grid Array)

ABSOLUTE MAXIMUM RATINGS

Power supply V_{EE}	0V to -7V
Analog input V_{IN}	+0.5V to V_{EE}
Reference voltages V_{RT}, V_{RM}, V_{RB}	+0.5V to V_{EE}
Reference range V_{RT} - V_{RB}	2.5V
Digital inputs CLK, $\overline{CLK}$, MINV, LINV	+0.5V to -4V
MidRef input current I_{VRM}	-10mA to +10mA
Digital output current I_D	0 to -20mA
Voltage between AGND and DGND	-50mV to +50mV
Voltage between AV_{EE} and DV_{EE}	-50mV to +50mV

THERMAL CHARACTERISTICS

Storage temperature range		-65°C to +150°C
Max. junction operating temperature		+175°C
Lead temperature (soldering 60s)		300°C
SP97508B HG	θ_{JA}	46°C/W
	θ_{JC}	11°C/W
SP97508B AC	θ_{JA}	40°C/W



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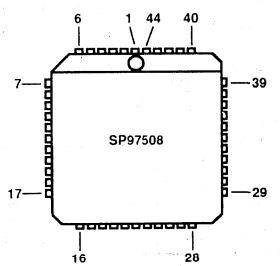


HG44

Pin	Function	Pin	Function	Pin	Function
1	NC	16	DGND	31	AGND
2	LINV	17	DGND	32	V_{IN}
3	NC	18	NC	33	AGND
4	DV_{EE}	19	DV_{EE}	34	V_{RM}
5	DGND	20	MINV	35	AGND
6	DGND	21	NC	36	V_{IN}
7	NC	22	$\overline{CLK}$	37	AGND
8	D0 LSB	23	CLK	38	NC
9	D1	24	NC	39	NC
10	D2	25	V_{RB}	40	NC
11	D3	26	AV_{EE}	41	AV_{EE}
12	D4	27	AV_{EE}	42	AV_{EE}
13	D5	28	NC	43	NC
14	D6	29	NC	44	V_{RT}
15	D7 MSB	30	NC		

Fig.1 Pin connections - top view

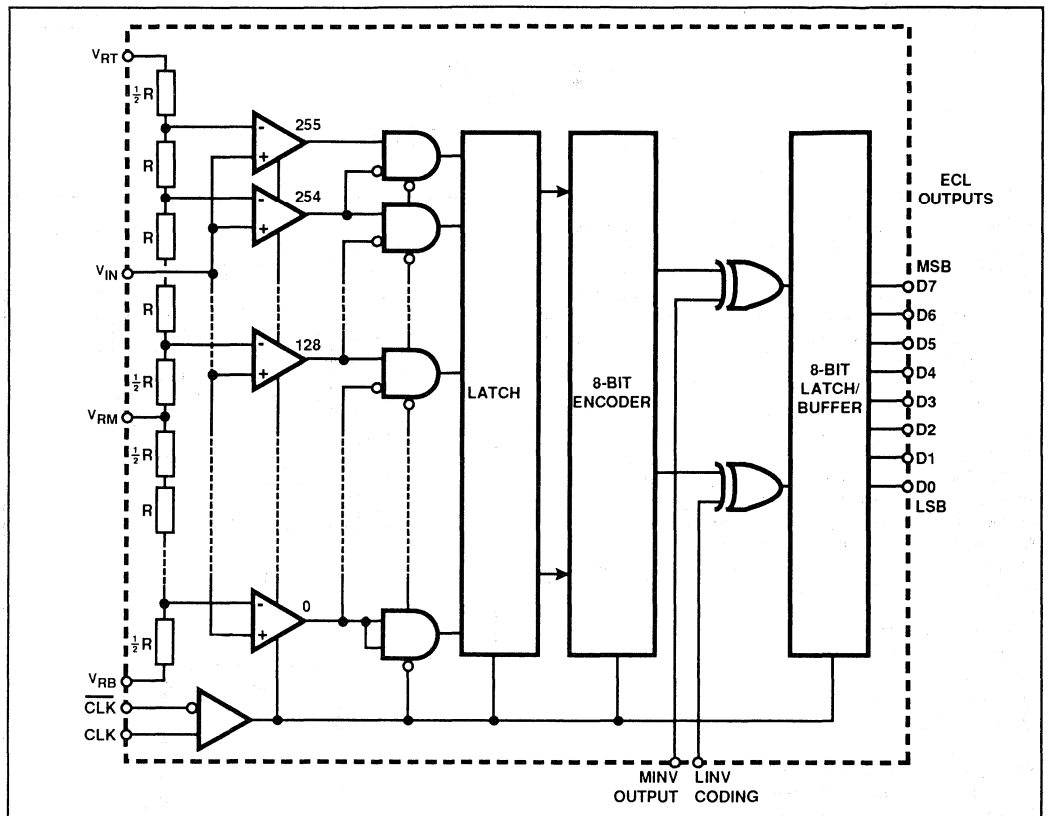


Fig.2 SP97508 functional block diagram

PIN DESCRIPTIONS (Pin numbers refer to HG44 package only)

Pin name	Function
AV_{EE}	Analog V_{EE}, -5.2V (typ.).
LINV	Input pin for polarity inversion of output data bits D0 to D6 (see Table 1).
DV_{EE}	Digital V_{EE}, -5.2V (typ.).
DGND	Digital ground, separated from the analog ground (AGND).
D0-D7	data output pins, ECL levels, D7 = MSB, D0 = LSB. External pulldown resistors are required, e.g. 680Ω to DV_{EE}.
MINV	Input pin for polarity inversion of D7 (MSB) (see Table 1). ECL '0' level is held when MINV is open circuit.
CLK	Clock input pin, ECL levels. Analog input signal, V_{IN}, acquired on rising edge (see Fig.8).
$\overline{CLK}$	Inverse clock input pin , ECL levels.
V_{RB}	Reference voltage (bottom), -2V (typ).
AGND	Analog ground.
V_{IN}	Analog input, range (V_{RT} - V_{RB}) p-p.
V_{RM}	Midpoint of the reference voltage; can be used for linearity adjustment.
V_{RT}	Reference voltage (top), 0V (typ.).
NC	Not Connected. Pins 1 and 18 should be connected to DGND, all others AGND.

RECOMMENDED OPERATING CONDITIONS

Supply voltage	-5.2V ± 0.25V	AGND to DGND	0mV ± 50mV
Reference (V_{RT})	0V ± 0.1V	Analog input	2V p-p max.
Reference (V_{RB})	-2.0V ± 0.2V	Output load	680Ω to -5.2V
AV_{EE} to DV_{EE}	0mV ± 50mV		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C, V_{EE} = -5.2V, V_{RT} = 0V, V_{RB} = -2V, full temperature range = -40°C to +85°C

Characteristic	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min.	Typ.	Max.		
Power Supply								
Supply current	I_{EE}	25	1	180	270	300	mA	
		Full	4	165		310	mA	
Analog Input								
Input bias current	I_{IN}	25	1	80	150	285	µA	
		Full	4	50		350	µA	
Input bandwidth (3dB)		25	4		120		MHz	
Input capacitance	C_{IN}	25	4		29	32	pF	V_{IN} = 0V
Input resistance	R_{IN}	25	4		75		kΩ	V_{IN} = 0V
Reference Chain								
Ladder resistance	R_R	25	1	90	105	135	Ω	
		Full	4	70		155	Ω	
Ladder offset (top & bottom)	$V_{RT/B}$	25	3		7.5		mV	
Clock Input								I/P voltage swing = 1Vp-p
Logic '1' voltage	V_{IH}	25	4	-3.05		DGND	V	
Logic '0' voltage	V_{IL}	25	4	-3.85		-0.8	V	
Logic '1' current	I_{IH}	25	1			380	µA	V_{IH} = -0.8V
		Full	4	310	360	390	µA	V_{IH} = -0.8V
Logic '0' current	I_{IL}	25	4			280	µA	V_{IL} = -1.8V
		Full	4	220	260	290	µA	V_{IL} = -1.8V
Min. pulse width (high)		25	4		3		ns	
Min. pulse width (low)		25	4		2.3		ns	
Digital Outputs								
Logic '1' voltage	V_{OH}	25	1	-0.90	-0.83		V	R_L = 680Ω to DV_{EE}
		Full	4	-1.00			V	
Logic '0' voltage	V_{OL}	25	4		-1.80	-1.90	V	R_L = 680Ω to DV_{EE}
		Full	4			-1.65	V	
Switching Performance								
Max. conversion rate	f_C	25	4	110			MHz	f_{IN} = 50MHz at FS
Aperture delay	t_{ad}	25	5		1.9		ns	
Aperture uncertainty	t_{au}	25	4		30		ps rms	
Output data delay	t_d	25	4		2.9		ns	R_L = 680Ω to DV_{EE}
Output data rise time	t_r	25	4		2.0		ns	R_L = 680Ω to DV_{EE}
Output data fall time	t_f	25	4		1.6		ns	R_L = 680Ω to DV_{EE}
Output data time skew	t_s	25	4		0.4		ns	R_L = 680Ω to DV_{EE}
Static Performance								f_C = 4MHz, f_{IN} = 1kHz ramp
Differential non-linearity	DNL	25	1	-0.85	±0.5	0.85	LSB	No missing codes
		Full	4	-1.0		1.0	LSB	No missing codes
Integral non-linearity	INL	25	1	-1.4		1.3	LSB	
		Full	4	-1.8		1.6	LSB	
Missing codes		25	1	No missing codes				Guaranteed
Gain error		25	1	-1.5		1.5	%FS	
Offset error		25	1	-15		0	mV	
Dynamic Performance								f_C = 100MHz
Transient response (rise)		25	4		2.4		ns	f_{IN} = 50MHz
Transient response (fall)		25	4		2.1		ns	square wave at FS
Slew rate			4		1.0		V/ns	
Differential non-linearity	DNL	25	1	-0.9		1.4	LSB	f_{IN} = 30MHz
Integral non-linearity	INL	25	1	-3.0		3.0	LSB	sinewave at FS
Signal-to-noise ratio	SNR	25	4		45.8		dB	f_{IN} = 1MHz at FS
		25	1	41	44.5		dB	f_{IN} = 10MHz at FS
		25	4		39.0		dB	f_{IN} = 30MHz at FS
Total harmonic distortion	THD	25	4		53.5		dBc	f_{IN} = 1MHz at FS
		25	1	46	48.5		dBc	f_{IN} = 10MHz at FS
		25	4		40.4		dBc	f_{IN} = 30MHz at FS
Effective number of bits	ENCOB	25	4		7.3		bits	f_{IN} = 1MHz at FS
		25	1	6.5	7.1		bits	f_{IN} = 10MHz at FS
		25	4		6.2		bits	f_{IN} = 30MHz at FS
Bit error rate	BER	25	4		1 in 10^9			f_{IN} = 50MHz at ¼ FS

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis is 3dB down on the DC level.

Aperture Delay

The delay between the rising edge of the CLOCK signal and the instant at which the analog input is sampled.

Aperture Jitter

The sample-to-sample variation in aperture delay.

Bit Error Rate (BER)

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occuring outside the histogram cusp for a $^3/_4$ FS sinewave.

Differential Non-Linearity (DNL)

The deviation of any code width from ideal 1LSB step.

Effective Number of Bits (ENOB)

This is a measure of the device's dynamic performance and may be obtained from the SNR or form a sine wave curve fit test, according to the following expressions:

$$\text{ENOB} = \frac{\text{SNR-1.76}}{6.02} \quad \text{or} \quad \text{ENOB} = \text{N-log}_2 \frac{\text{rms error (actual)}}{\text{rms error (ideal)}}$$

where N is the conversion resolution and the rms error is the deviation of the output from an input sine wave.

Integral Non-Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Output Delay

The delay between the 50% point of the falling edge of the clock signal and the 50% point of any data output change.

Reference Ladder Offset

The voltage error at the ends of the resistor chain caused by the end terminations, the lead frame and the bond wire.

Signal-to-Noise Ratio (SNR)

The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components, including harmonics but excluding DC with a full scale analog input signal.

Total Harmonic Distortion (THD)

The RMS value of all the harmonics compared with the RMS value of the fundamental.

Transient Response

The time required by the outputs to move from 10(90)% to 90(10)% of the full scale range.

Test Levels

- **Level 1** - 100% production tested at 25°C
- **Level 2** - 100% production tested at 25°C and sample tested at specified temperatures
- **Level 3** - Sample tested only
- **Level 4** - Parameter is guaranteed by characterisation or design
- **Level 5** - Parameter is a typical value only

APPLICATION NOTES

Analog Input (Figs.3, 4 and 5)

The maximum amplitude and offset of the input is defined by the reference voltages (V_{RB} to V_{RT}). The optimum input is 2V p-p with a DC offset of -1V. The analog input circuit of the SP97508 consists of 256 buffered comparator inputs, as shown in Fig. 3.

The internal buffering to the device results in the typical input characteristics of Figs. 4 and 5. The dependence of input capacitance on voltage level is typical of flash converters and so requires that the analog input is driven from a low impedance source such as the SL9999.

Failure to drive the input capacitance properly causes increased levels of harmonic distortion, most noticeable in the second harmonic.

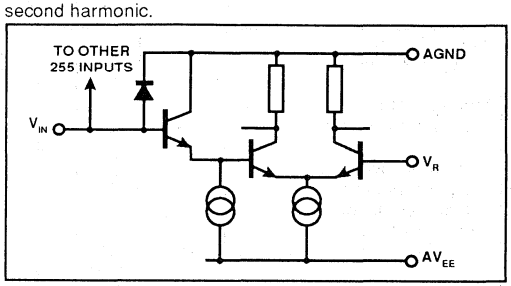


Fig.3 Analog input

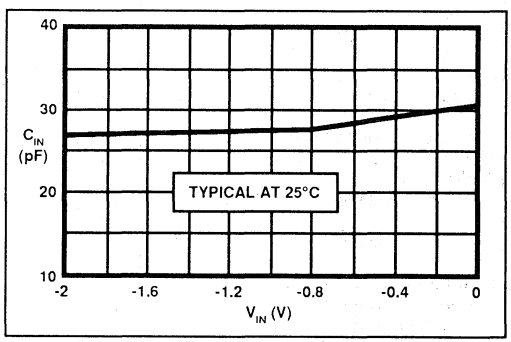


Fig.4 Analog input capacitance

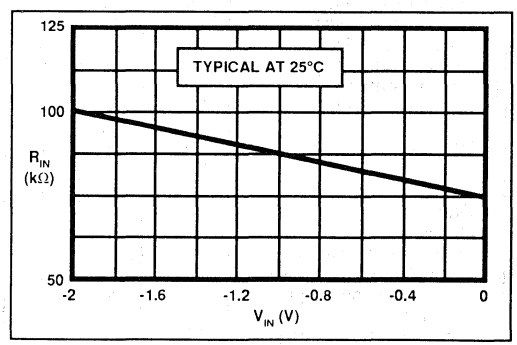


Fig.5 Analog input resistance (AC)

Reference Pins (Fig. 6)

Between V_{RT} and V_{RB} there are 256 series resistors forming the reference chain. The total resistance may be between 90Ω and 120Ω. A mid-reference pin (V_{RM}) is also provided as an option for precision setting of integral linearity. Both V_{RM} and V_{RB} should be adequately decoupled to analog ground. For optimum performance, V_{RT} is connected directly to analog ground and V_{RB} is driven from a -2V DC supply. For precise reference setting, this supply should be adjustable by ±0.2V.

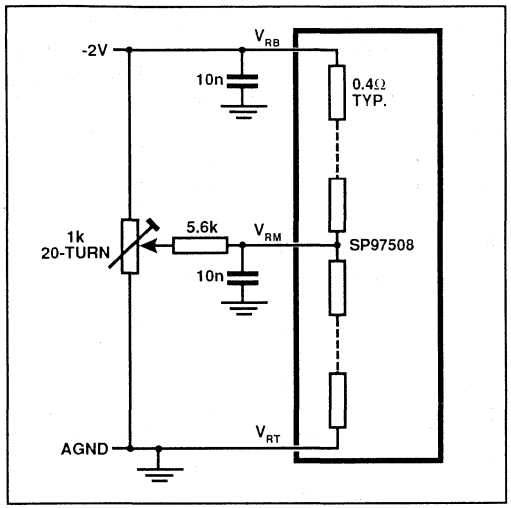


Fig.6 Reference connections

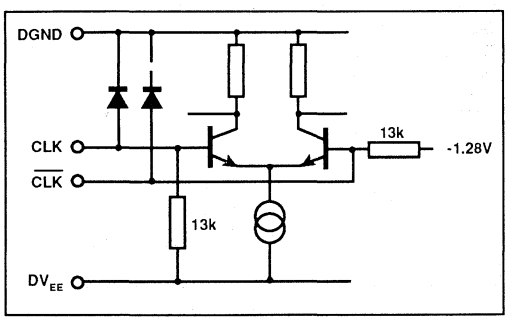


Fig.7 Clock inputs

Clock Inputs CLK and $\overline{CLK}$ (Figs. 7 and 8)

The SP97508 can be driven from either differential or single-ended ECL clocks. In either mode, the clock lines should be terminated with the line's characteristic impedance close to the device clock pins. For full 100MHz operation, a conventional unity mark/space ratio clock can be used.

Single-ended drive can be simply provided by adding a 1nF chip or encapsulated chip capacitor from the $\overline{CLK}$ pin to DGND. The $\overline{CLK}$ pin will then self-bias at -1.28V, which is the mid-threshold for ECL. The device can then be clocked by an ECL signal into the CLK input.

Timing (Fig.8)

The analog input is acquired by the device shortly after the rising edge of the CLK signal. The internal latch causes a one cycle delay, hence the output data is valid one clock cycle after the acquisition of the analog signal.

The output data is further delayed by the clock-to-output delay (t_D = 2.9ns typ.). This gives the advantage that the same timing and phase of the SP97508 CLK signal can be used to acquire the output data.

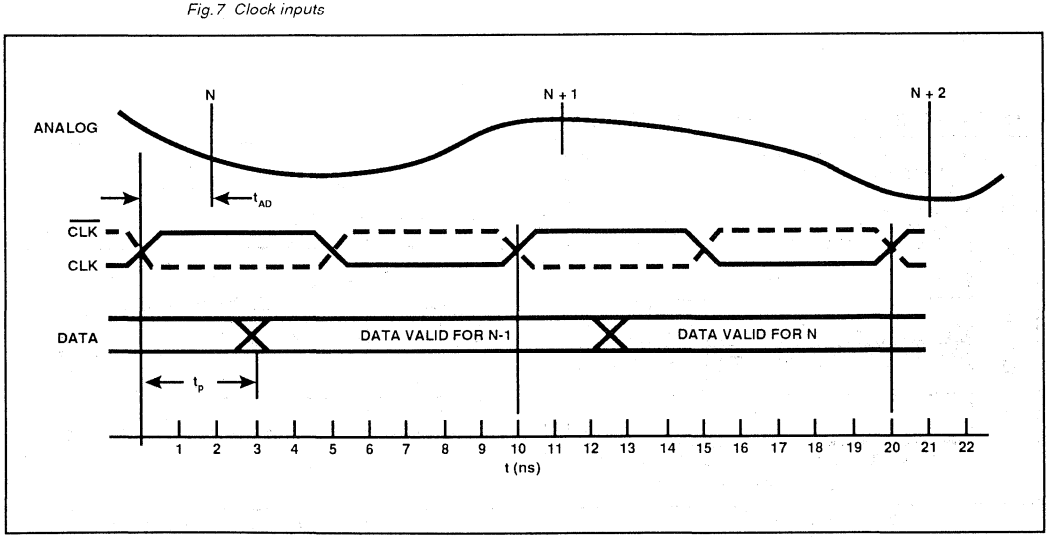


Fig.8 Timing at 100MHz (typ.)

Output Coding (Table 1 and Fig.9)

With MINV and LINV left open circuit, the output will be coded in standard binary with all 1s code corresponding to the most positive input $V_{IN}=V_{RT}=0V$.

An inverse binary output can be provided by connecting both MINV and LINV to ground.

Two's complement coding (inverted MSB) can be provided by connecting only the MINV pin to ground and inverse two's complement coding can be achieved by connecting only the LINV pin to ground.

V_{IN}	Binary MINV = O/C (0) LINV = O/C (0)	Inv 2s' comp. MINV = O/C (0) LINV = GND (1)	2s' comp. MINV = GND (1) LINV = O/C (0)	Inv binary MINV = GND (1) LINV = GND (1)
0V	111 11	100 00	011 11	000 00
	111 10	100 01	011 10	000 01
	-	-	-	-
	-	-	-	-
	-	-	-	-
	100 00	111 11	000 00	011 11
	011 11	000 00	111 11	100 00
	-	-	-	-
	-	-	-	-
	-	-	-	-
	000 01	011 10	100 01	111 10
-2V	000 00	011 11	100 00	111 11

Table 1

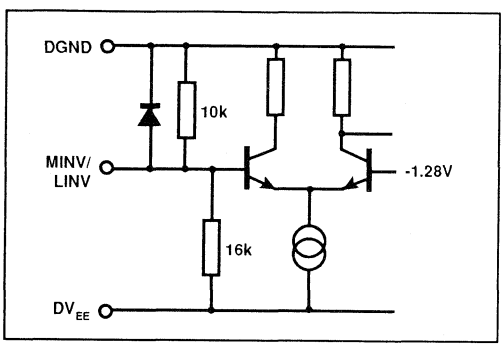


Fig.9 MINV/LINV input

8-Bit ECL Outputs (Fig.10)

The outputs are standard ECL open emitters and therefore require pull-down resistors connected from the outputs to -5.2V or -2V digital supply. Single in-line resistors of value 680Ω to 1kΩ are recommended for termination to DV_{EE}. The outputs are capable of driving 200Ω terminations connected to a -2V supply.

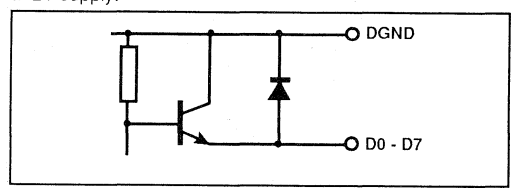


Fig.10 Digital output

TYPICAL PERFORMANCE CHARACTERISTICS

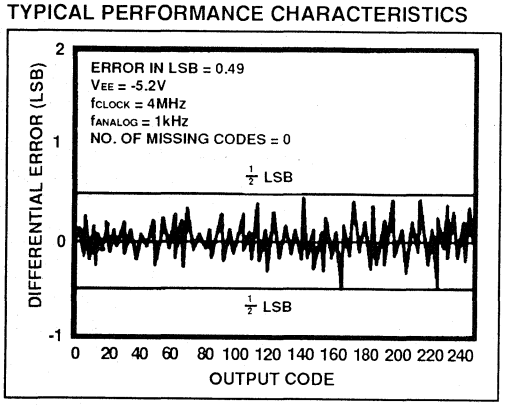


Fig.11 Static differential linearity in LSB: typical production device

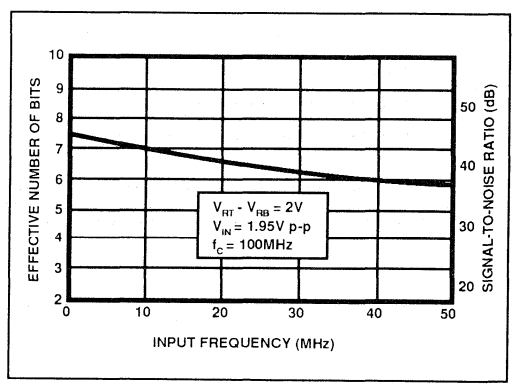


Fig.12 Effective number of bits (ENOB) and signal-to-noise ratio (SNR) v. input frequency

CIRCUIT BOARD CONSTRUCTION

As with most PCB construction for analog-to-digital conversion, the best performance from the SP97508 can be achieved by separating the ground plane into two sections: analog ground (AGND), and digital ground (DGND). This aids the device performance by reducing the degree of noise due to digital switching fed back to the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which, ideally, should be terminated by a 680Ω load to the -5.2V digital supply, DV_{EE}.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. It is wise, therefore, to decouple the SP97508 close to the device supply pins with good quality, high frequency capacitors.

Notes on Construction

1. Use split analog and digital ground planes connected together close to the device. Do not run the analog input next to the clock or data lines.
2. All NC pins must be grounded: connect pins 1 and 18 to DGND, all others to AGND.
3. Connect digital and analog supplies together at a point on the PCB away from the device.
4. Use 10nF capacitors for supply decoupling.
5. Use stripline techniques for siginal paths longer than 5cm (2 inches)
6. Use 4.7µF electrolytic capacitors to decouple the -5.2V V_{EE} supplies

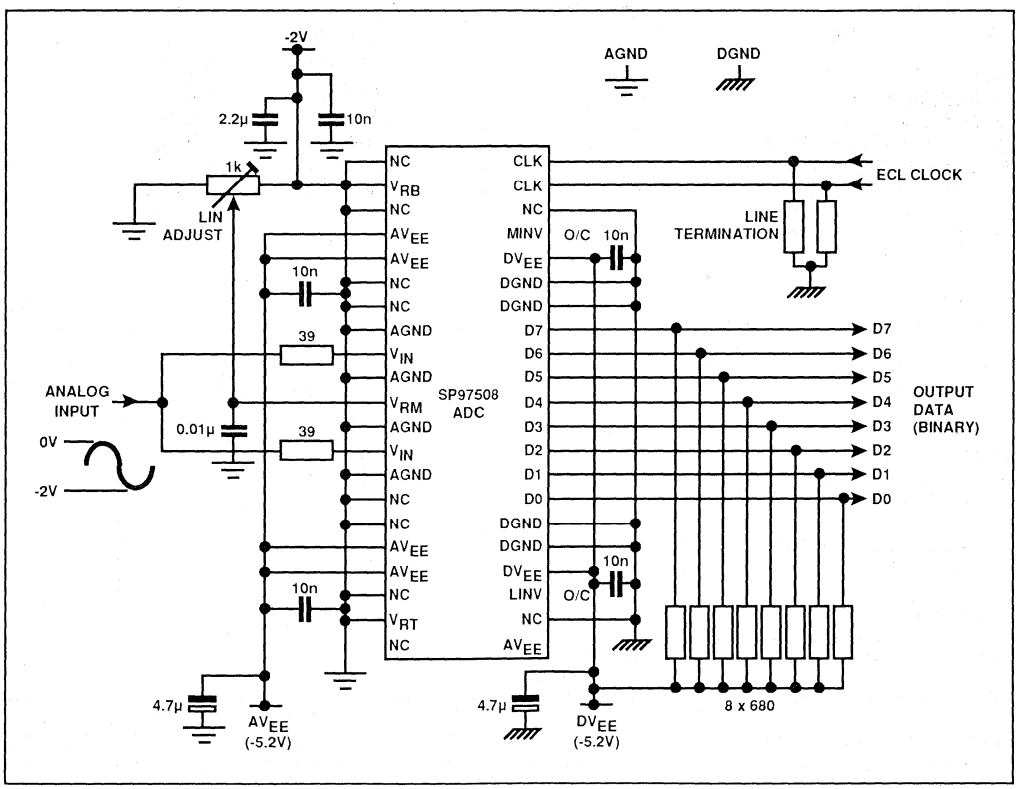


Fig.13 Test and Application circuit

VP1058

8-BIT, 25MHz, VIDEO FLASH ADC (SINGLE + 5V SUPPLY)

The VP1058 is a low power analog-to-digital flash converter which requires no preceding sample and hold stage. Operating from a single +5V supply, it is capable of digitising analog signals with frequencies up to the Nyquist limit.

Output data is available in four possible 8-bit formats, selectable via two digital control inputs, giving either true or inverted code in binary or offset twos' complement.

FEATURES

- 8-Bit Resolution
- 25MHz Conversion Rate
- 60MHz 3dB Analog Input Bandwidth
- Single +5V Supply Operation
- Low Power Consumption (Typically 670mW)
- +3V to +5V Analog Input Range
- Selectable Data Format
- TTL Compatible
- Direct Replacement for TDC 1058 or CXA 1096P
- Low Cost
- No Missing Codes - Guaranteed

APPLICATIONS

- Digital Television
- Computing
- Radar
- Medical Imaging
- Nucleonics
- Low-Cost, High-Speed Data Conversion

OPERATING TEMPERATURE RANGE

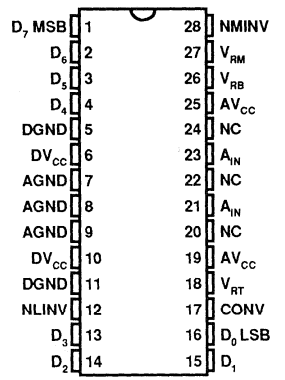
Commercial 0°C to 70°C (Still - Air ambient)

ORDERING INFORMATION

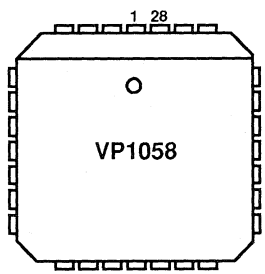
VP1058 F CG DPAS (Commercial - Plastic DIL Package, DP28)
VP1058 F CG HPAS (Commercial - Quad Plastic J Lead Package, HP28)
VP1058 F CG DGAS (Commercial - Ceramic DIL Package, DG28)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+7V
Analog input, A_{IN}	Vcc +0.5
Reference voltage V_{RT}, V_{RB}	Vcc +0.5
Reference voltage V_{RT}, V_{RB}	2.5V
Digital inputs	Vcc
Mid-ref input current	-50mA to +50mA
Digital output current	-20mA to +20mA
Voltage between AGND and DGND	-0.5V to +0.5V
Voltage between AVcc and DVcc	-0.5V to +0.5V



DP28
DG28



HP28

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	D_7 MSB	8	AGND	15	D_1	22	NC
2	D_6	9	AGND	16	D_0 LSB	23	A_{IN}
3	D_5	10	DV_{CC}	17	CONV	24	NC
4	D_4	11	DGND	18	V_{RT}	25	AV_{CC}
5	DGND	12	NLINV	19	AV_{CC}	26	V_{RB}
6	DV_{CC}	13	D_3	20	NC	27	V_{RM}
7	AGND	14	D_2	21	A_{IN}	28	NMINV

Fig.1 Pin Connections (Top View)

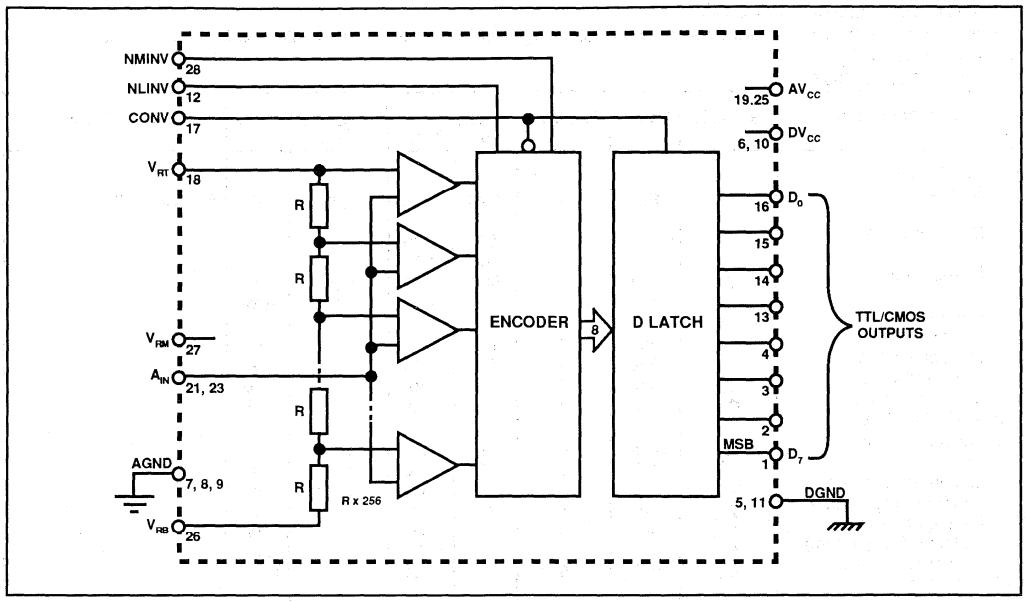


Fig.2 Internal block diagram

PIN DESCRIPTIONS

Pin No.	Function	Description
1	D_7	Most significant bit (output data bit 7)
2 - 4	D_6 - D_4	Output data bits 6 to 4
5, 11	DGND	Digital ground
6, 10	DV_{CC}	Digital supply pin (+5V)
7 - 9	AGND	Analog ground
12	NLINV	Not Least significant bits INvert - inverts data D_0 to D_6 when taken low
13 - 15	D_3 - D_1	Output data bits 3 to 1
16	D_0	Least significant bit (output data bit 0)
17	CONV	Clock input - the rate of input (CONVert) clock signal determines the ADC sampling rate
18	V_{RT}	Top of reference resistor chain
19, 25	AV_{CC}	Analog supply pin
20, 22, 24	NC	Not connected
21, 23	A_{IN}	Analog input pin
26	V_{RB}	Bottom of reference resistor chain
27	V_{RM}	Midpoint of reference resistor - can be used for linearity adjustment
28	NMINV	Not Most significant bit INvert - inverts data bit D_7 when taken low

THERMAL CHARACTERISTICS

Storage Temperature Range			-65°C to +150°C	
Maximum Junction Operating Temperature			+175°C	
Lead Temperature (soldering 60 seconds)			300°C	
	DP	**HP**	**DG**	
Junction to Ambient θjA	55	57	44	°C/W
Junction to Case θjc	14	15	9	°C/W

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5V ± 0.25V
Reference V_{RT}	5V ± 0.1V
Reference V_{RB}	3V ± 0.1V
AV_{CC} to DV_{CC}	0V ± 50mV
Analog Input	4V ± 1V

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions conditions (unless otherwise stated):

V_{CC} = +5V ± 0.25V, T_{amb} = 25°C

DC CHARACTERISTICS

Characteristic	Symbol	Temp	Test level	Value. Min.	Value. Typ.	Value. Max.	Units	Conditions
Power Supply								
Supply voltage	AV_{CC}/DV_{CC}	Full	4	4.75		5.25	V	AGND/DGND = 0V
Supply current	I_{CC}	Full	4	95	125	165	mA	
		25	1	105	125	150	mA	
Power dissipation	P	Full	4	500	670	900	mW	
		25	1	540	670	830	mW	
Analog Input								
Input range	A_{IN}	Full	4	V_{RB}		V_{RT}	V	
Input bias current	I_{IN}	Full	4	60	150	500	µA	
3dB bandwidth	f_{3dB}	25	4		60		MHz	
Input capacitance	C_{IN}	25	4		30		pF	
Reference Ladder								
Ladder resistance	R_D	Full	4	50	90	145	Ω	
		25	1	75	100	125	Ω	
Ladder voltage (top)	V_{RT}	Full	4		5.0	AV_{CC} + 0.1	V	} $V_{RT} > V_{RB}$
Ladder voltage (bottom)	V_{RB}	Full	4	2.5	3.0		V	
Ladder offset (top)	V_{RTO}	25	5		15		mV	
Ladder offset (bottom)	V_{RBO}	25	5		5		mV	
Ladder temp. coeff.	R_{TC}	Full	5		0.33		Ω/°C	
Digital Inputs								
Logic '1' voltage	V_{IH}	Full	4	2.0			V	
Logic '0' voltage	V_{IL}	Full	4			0.8	V	
Logic '1' current	I_{IH}	Full	4			350	µA	$V_I = V_{CC}$ = MAX
Logic '1' current	I_{IH}	Full	4			75	µA	V_I = 2.4V, V_{CC} = MAX
Logic '0' current	I_{IL}	Full	4			-150	µA	V_I = 0.4V, V_{CC} = MAX
Digital Outputs								
Logic '1' voltage	V_{OH}	Full	4	2.4			V	} Into a standard LSTTL load
		25	1	2.4			V	
Logic '0' voltage	V_{OL}	Full	4			0.4	V	
		25	1			0.4	V	
Static performance								
Differential non-linearity	DNL	Full	4		±0.5		LSB	
		25	4		±0.5		LSB	
Integral non-linearity	INL	Full	4		±0.5		LSB	
		25	4		±0.5		LSB	

AC CHARACTERISTICS

Characteristic	Symbol	Temp	Test level	Value. Min.	Value. Typ.	Value. Max.	Units	Conditions
Clock min.high	t_{PW1}	Full	4	15			ns	
Clock min.low	t_{PW0}	Full	4	15			ns	
Max. conversion rate	f_{MAX}	Full	4	25			MHz	A_{IN} at FS & 12.5MHz
Aperture delay	t_{AD}	25	5		3		ns	
Output data delay	t_D	25	4			25	ns	} With standard LSTLL load
		Full	4			30	ns	
Output hold time	t_{HO}	25	4	5			ns	
		Full	4	5			ns	
Aperture Jitter		25	5		50		ps	
Dynamic Performance								f_{CLK} = 25MHz
Differential non-linearity	DNL	25	1	-0.85	±0.5	+1	LSB	} A_{IN} at FS & 1.019MHz
Integral non-linearity	INL	25	1		±1	±2	LSB	
S/N ratio	SNR	25	1		45		dB	A_{IN} = 1.019MHz
		Full	4		44.5		dB	A_{IN} = 1.019MHz
		25	4		44.0		dB	A_{IN} = 2.438MHz
		Full	4		43.5		dB	A_{IN} = 2.438MHz
		25	4		43.5		dB	A_{IN} = 4.388MHz
		Full	4		43.0		dB	A_{IN} = 4.388MHz
Effective No. of bits	ENOB	25	1		7.2		bits	A_{IN} = 1.019MHz
			4		7.1		bits	A_{IN} = 2.438MHz
			4		7.0		bits	A_{IN} = 4.388MHz

ELECTRICAL CHARACTERISTICS DEFINITIONS

Analog Bandwidth
The analog input frequency, at which the spectral power of the fundamental frequency as determined by Fast Fourier Transform analysis, is 3dB down on the DC level.

Aperture Delay
The delay between the falling edge of the CONV signal and the instant at which the analog input is sampled.

Aperture Jitter
The variation between successive samples of the aperture delay.

Conversion Rate
The maximum rate at which the converter will run.

Differential Non-Linearity (DNL)
The deviation of any code width from an ideal LSB step.

Effective Number of Bits (ENOB)
This is a measure of the dynamic performance which is calculated from the following expression.:

$$\text{ENOB} = \frac{\text{SNR-1.76}}{6.02}$$

SNR is the signal-to-noise ratio, in decibels, at the test frequency.

Integral Non-Linearity (INL)
The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

Output Data Delay
The delay between the 50% point of the rising edge of the CONV signal and the 50% point of any data output change.

Reference Ladder Offset
The voltage error at the ends of the resistor chain caused by the lead frame and bond wire.

Signal-to-Noise Ratio (SNR)
The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components including harmonics but excluding DC with a full scale analog input signal.

Test Levels
- **Level 1** - 100% production tested
- **Level 2** - 100% production tested at 25°C and sample tested at specified temperatures
- **Level 3** - Sample tested only
- **Level 4** - Parameter is guaranteed by design and characteristics testing
- **Level 5** - Parameter is a typical value only

CONVERSION TIMING

Operation of the VP1058 requires that an external clock be applied to the CONV (convert) pin. This CONV signal synchronises the sampling, conversion, and output stages of the devices as shown in the timing diagram (Fig.3).

The analog input is sampled when the comparator array is latched after a rising edge on the CONV pin. This rising edge also causes the result of the previous sample to be transferred to the outputs. Data at the outputs is latched at the same time as the 255 to 8 encoding of the current sample. Both these operations are performed on the falling edge of the CONV signal. This results in a 'pipeline' delay which means that the digital result of sample 'N' is available for acquisition by external circuitry whilst sample 'N+2' is being taken.

The time interval between a rising edge on the CONV pin and the comparators latching is the aperture delay time (t_{AD}). This time may be subject to small variations mainly due to temperature and component matching. The short term uncertainty in the aperture delay time is specified by the aperture jitter (or aperture error). Output data becomes valid after t_D (output data delay). Data remains valid for at least t_{HO} (output hold time) after the rising edge of the CONV pin.

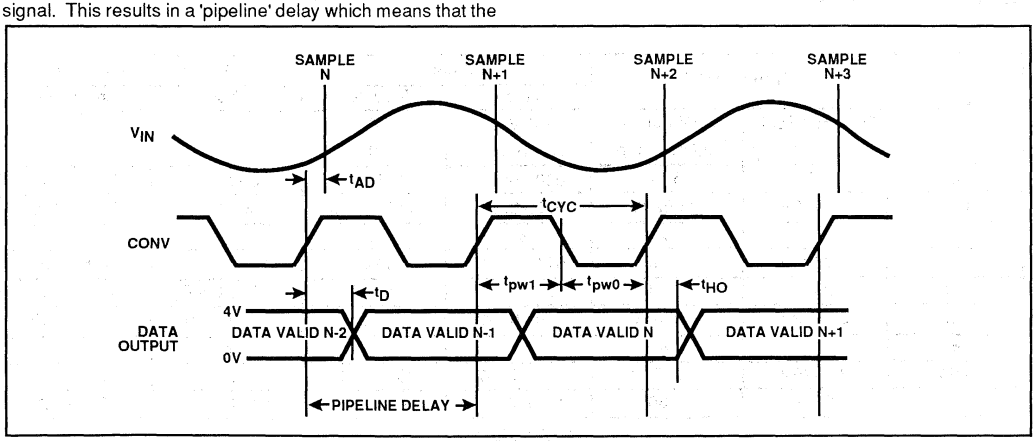


Fig.3 Timing diagram

GENERAL CIRCUIT DESCRIPTION

The VP1058 employs a 'flash' architecture consisting of a reference resistor chain, an array of 256 comparators, encoding logic, and a full 8-bit D-type output latch. The 255 reference levels generated by the resistor chain are compared with the analog input signal by the comparator array. This produces a thermometer code which the encoding logic coverts into an 8-bit word. The D-type latch accepts this data and holds the outputs until the next conversion. The format of the output data is determined by the NLINV and NMINV control lines.

Analog Input

The maximum amplitude and offset of the input is defined by the setting of the two reference voltages V_{RB} and V_{RT}. A signal outside this range will cause the output to be either full-scale positive or full-scale negative, depending on whether the signal is off scale in the positive or negative direction.

For optimum performance, the input signal should be biased at +4.0V with a 2V peak-to-peak amplitude. The necessary gain, offset and low impedance drive required for the input signal can be provided by use of a high slew rate ADC driver.

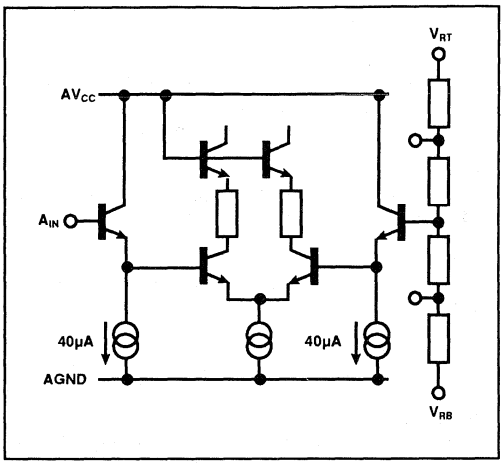


Fig.4 Analog input

Reference Voltage

The reference chain between pins V_{RB} and V_{RT} is formed of 256 series resistors and has a total resistance of approximately 90Ω. A mid-reference pin, V_{RM}, is provided for precise setting of the integral linearity, although adjustment is not necessary to meet the data sheet specification.

The VP1058 will convert analog signals in the range $V_{RB} \leq A_{IN} \leq V_{RT}$, where V_{RB} and V_{RT} are in the range +3V to +5V. (The design of the VP1058 has been optimised for VRB = 3V and VRT = 5V). All reference pins should be adequately decoupled close to the device.

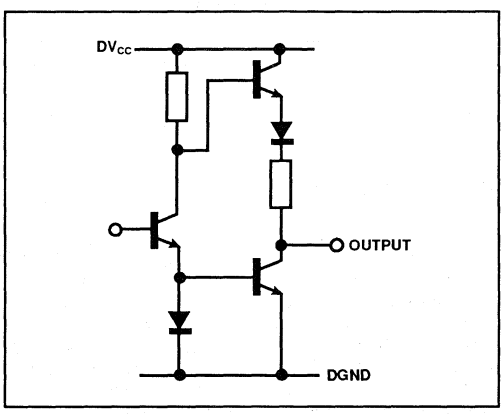


Fig.5 TTL output stage

Output Format

The output data format is controlled by the logic levels at the NLINV and NMINV pins as shown on the output coding table. These inputs are active low and may be tied to DV_{CC} for logic '1' or DGND for logic '0'. Both inputs are considered DC controls and as such should only be altered while the converter is in the steady state.

Code	Input voltage		Binary		Offset 2s' complement	
			True	Inverted	True	Inverted
	20.V Full Scale	2.048V Full Scale	NMINV = 1	0	0	1
	7.8431mV Step	8.0mV Step	NLINV = 1	0	1	0
000	5.0V	5.0V	0000 0000	1111 1111	1000 0000	0111 1111
001	4.9922V	4.9922V	0000 0001	1111 1110	1000 0001	0111 1110
•	•	•	•	•	•	•
127	4.0039V	3.9840V	0111 1111	1000 0000	1111 1111	0000 0000
128	3.9961V	3.9760V	1000 0000	0111 1111	0000 0000	1111 1111
129	3.9882V	3.9680V	1000 0001	0111 1110	0000 0001	1111 1110
•	•	•	•	•	•	•
254	3.0079V	2.9680V	1111 1110	0000 0001	0111 1110	1000 0001
255	3.0V	2.960V	1111 1111	0000 0000	0111 1111	1000 0000

Table 1 Output coding

APPLICATION NOTES

As with all high speed analog-to-digital converters, careful consideration must be given to circuit layout. The best performance from the VP1058 can be achieved by use of separate analog and digital ground planes. Ideally these should be connected at a point close to the device. This will reduce the amount of digital switching noise fed back into the analog section of the converter, so aiding device performance.

Supply line decoupling is important when dealing with mixed analog and digital signals, as they can provide a feedback path from the digital output currents. Therefore, the VP1058 should be decoupled close to the device supply pins with good quality high frequency, low inductance capacitors. Due to the high clock rates, long clock lines to the device should be avoided to reduce noise pick up.

A typical applications circuit is shown below. The analog input amplifier should be a wideband, high slew rate op-amp used to drive the input directly. A stable reference is needed for both input offset and gain control (e.g. REF12Z micropower voltage reference as shown in Fig.6). Both analog input pins should be connected close to the device with the input amplifiers feedback loop closed at the point. The reference inputs should be adequately decoupled to ground so as to limit the effects of system noise on conversion accuracy. A capacitor at the mid-reference point (as shown) may be useful in correcting any inherent reference ladder skew.

The circuit will accept a 1V p-p video signal and level shift and multiply it to provide the recommended 2V p-p signal to drive the VP1058.

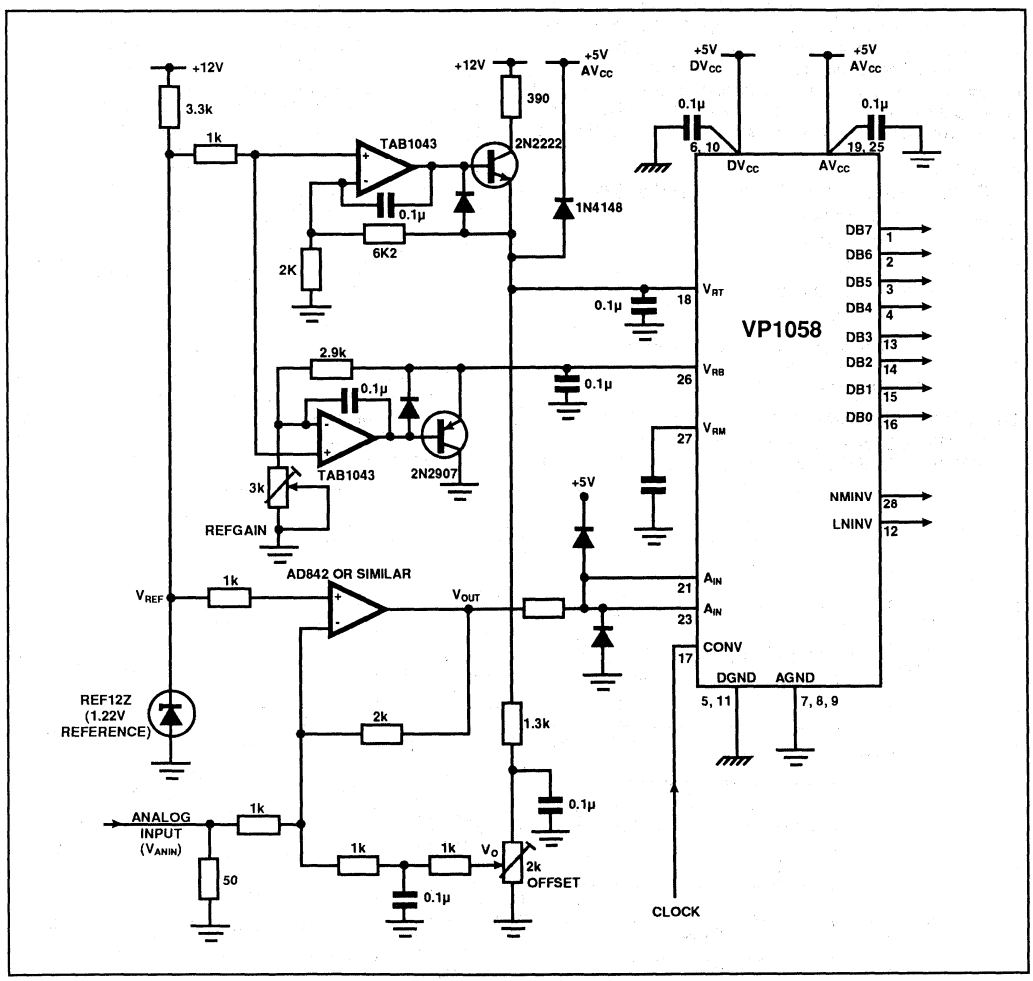


Fig.6 Typical applications circuit

VP8708

30MHz 8–BIT ANALOG VIDEO INPUT INTERFACE

(Supersedes edition in December 1993 Digital Video & Digital Signal Processing Handbook)

The VP8708 is an analog input interface designed for video signal conditioning and digitisation.

Operating from a single +5V supply, the VP8708 includes an input multiplexer, video amplifier with clamp and gain control, an onboard reference and a buffered 8–bit ADC capable of digitising signals upto the Nyquist limit.

Video signals may be supplied to the VP8708 either directly to the ADC, or via one of three multiplexed inputs for signal conditioning. The analog signal (with appropriate gain and clamping) is available as output prior to digitisation. The coded data, updated at the sample rate, is available in either binary or two's complement format via the 3–state TTL output buffers.

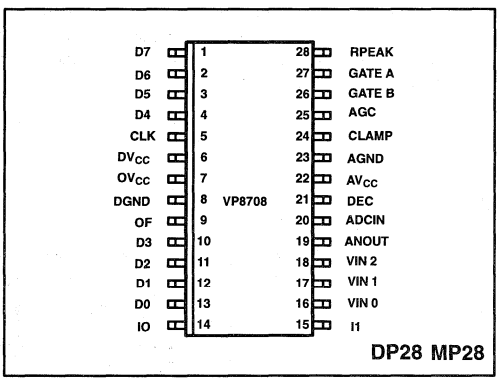


Fig. 1 Pin connections – top view

FEATURES

- Direct replacement for the PhilipsTDA8708†
- 30MHz Sampling rate
- Selectable data format:
- Internal ADC reference
- Clamp and AGC functions
- 3–state TTL outputs

†GEC Plessey also offer direct replacements for Philips TDA8708A (GPS part no VP87A8) TDA8709A (GPS part no VP87A9)

ORDERING INFORMATION

VP8708G CG DPAS (Commercial – Plastic DIL)
VP8708G CG MPES (Commercial – Miniature Plastic DIL)

ABSOLUTE MAXIMUM RATINGS

Supply voltages, AV_{CC}, DV_{CC}, OV_{CC}	+7V
Supply differential	±1V
Ground differential	±1V
Video input voltage	AV_{CC}
Output current	10mA

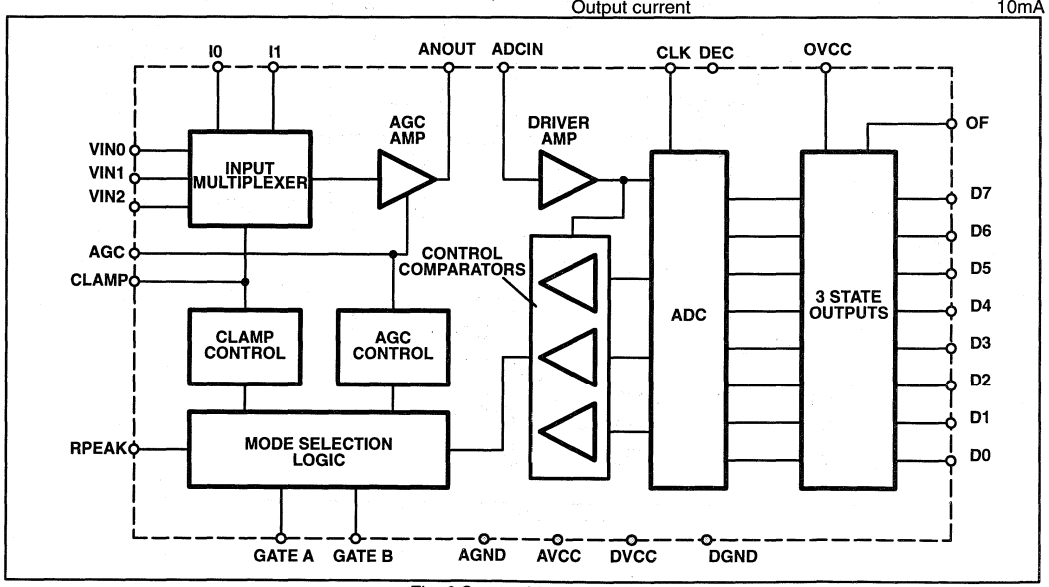


Fig. 2 System block diagram

RECOMMENDED OPERATING CONDITIONS

Supply voltage AV_{CC}, DV_{CC}, OV_{CC}	+5V
Supply differential	0V
Ground differential	0V
Video input voltage	1Vp–p

OPERATING TEMPERATURE RANGE

Commercial 0°C to +70°C (still air ambient)

THERMAL CHARACTERISTICS

Storage temperature range	–65°C to 150°C
Lead temperature (soldering 11 seconds)	+265°C
THERMAL RESISTANCES, DP PACKAGE	
Junction to ambient (θ_{ja})	55°C/W
Junction to case (θ_{jc})	14°C/W
THERMAL RESISTANCES, MP PACKAGE	
Junction to ambient (θ_{ja})	84°C/W
Junction to case (θ_{jc})	32°C/W

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
POWER SUPPLY								
Analog supply voltage	AV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Digital supply voltage	DV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Output supply voltage	OV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Analog supply current	AI_{CC}	25 FULL	1 4		60	 72	mA mA	
Digital supply current	DI_{CC}	25 FULL	1 4		13	 19	mA mA	
Output supply current	OI_{CC}	25 FULL	1 4		12	 18	mA mA	
Power dissipation	P	25 FULL	1 4		425	 600	mW mW	
VIDEO INPUTS								
Input range	V_{IN} (p–p)	FULL	4	0.5	1.0	1.6	V	
Input impedance	$\|Z_{IN}\|$	FULL	4	18	20	22	kΩ	f_{in}=6MHZ
Input capacitance	C_{in}	25	5		2		pF	f_{in}=6MHZ
I1, IO GATE B,TTL INPUTS + GATE A								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input current HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input current LOW	I_{il}	25 FULL	1 4	–150 –200			µA µA	V_i=0.4V V_i=0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			10 20	µA µA	V_i=3.6V V_i=3.6V
RPEAK Input								
Peak capacitor charge/discharge current	I_{PEAK}	FULL	4		80		µA	R_{peak} = 0Ω

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
AGC Control Input								
AGC voltage for minimum gain	V_{agc}	25	4		2.7		V	
AGC voltage for maximum gain	V_{agc}	25	4		3.9		V	
AGC output current	I_{agc}	25	1		*			* See table 4
CLAMP Control Input								
Clamp voltage	V_{clp}	25	4		3.5		V	ADC output = 128
Clamp output current	I_{clp}	25	1		*			* See table 4
VIDEO Amplifier Outputs								
Internal current source	I_{19}	25	4			2	mA	
DC Output voltage for black level	V_{blk}	FULL	4		AV_{CC}– 3.25		V	
AC Output voltage (peak–peak)	V_{19}	FULL	4		1		V	
Output impedance	Z_{19}	25	4		45		Ω	
CLK INPUT								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input current LOW	I_{il}	25 FULL	1 4	–150 –200			µA µA	V_i = 0.4V V_i = 0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			10 20	µA µA	V_i= 3.6V V_i= 3.6V
Input impedance	$\|Z_{IN}\|$	25	4		3.5		kΩ	
Input capacitance	C_{clk}	25	4		5		pF	
Maximum frequency	f_{max}	FULL	4	30			MHz	
OF INPUT (3–state control)								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input voltage 3–STATE	V_z	25	1		1.4		V	
Input current LOW	I_{il}	25 FULL	1 4	–175 –200			µA µA	V_i=0.4V V_i=0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			500 700	µA µA	V_i=3.6V V_i=3.6V

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
ADCIN INPUT								
Input voltage	V_{adc}	FULL	4		AV_{CC}– 1.75		V	For Code 0
Input voltage	V_{adc}	FULL	4		AV_{CC}– 1.25		V	For Code 255
Input voltage amplitude (p–p)	V_{20}	FULL	4		0.5		V	
Input current	I_{adc}	25	1		1		µA	
Input impedance	Z_{adc}	25	1		14		MΩ	
Input capacitance	C_{adc}	25	4		5		pF	
DIGITAL OUTPUTS								
Output voltage LOW	V_{ol}	25 FULL	4 4			0.4 0.4	V V	$I_{ol=}$ 2mA $I_{ol=}$ 2mA
Output voltage HIGH	V_{oh}	25 FULL	1 4	2.4 2.4			V V	$I_{oh=}$–0.4mA $I_{oh=}$–0.4mA
3–STATE Output current	I_{OZ}	25	4		2		µA	
ADC PERFORMANCE								
Static differential non – linearity	DNL	25 FULL	1 4		±0.5 ±0.5		lsb lsb	
Static integral non – linearity	INL	25 FULL	1 4		±1 ±1		lsb lsb	
Dynamic integral non – linearity	INL	25 FULL	1 4		±2 ±2		lsb lsb	
VIDEO AMPLIFIER DYNAMIC PERFORMANCE								
–3dB Bandwidth	f3dB	25	4		20		MHz	
Differential gain	G_d	25	4		2		%	
Differential phase	$\varnothing_d$	25	4		2		degrees	
Gain range	ΔG	25	4	–3		7	dB	
Crosstalk between VIN inputs		25	4		–60		dB	
Signal–to–noise ratio	SNR	25	4		55		dB	
ANALOG SIGNAL* PROCESSING								*f_{clk} = 30MHz
–3dB Bandwidth	f3dB	25	1		15		MHz	
Differential gain	G_d	25	4		2		%	
Differential phase	$\varnothing_d$	25	4		2		degrees	
Total harmonic distortion	THD	25	4		–55		dB	
Supply voltage ripple rejection	SVRR	25	4		5		%/V	

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=T_{full} =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
TIMING*								* f_{clk}=30MHz C_1=15pF I_{ol}=2mA
Sampling delay	t_{ds}	FULL	4		3		ns	
Output hold time	t_{ho}	FULL	4	5			ns	
Output delay time	t_d	FULL	4			20	ns	
3 State delay time for enble	t_{ez}	FULL	4			25	ns	
3 State delay time for disable	t_{dz}	FULL	4			25	ns	

ELECTRICAL CHARACTERISTIC DEFINITIONS

Analog –3dB Bandwidth ADC

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis, is 3dB down on the DC level.

Differential Non–Linearity (DNL)

The deviation of any code width from an ideal 1LSB step size.

Integral Non–Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least–square curve–fit.

Differential Gain (G_d) and Phase ($\varnothing_d$)

The difference in gain/phase at the ADC output when a 17.5 IRE units peak to peak, 3.58MHz input signal is superimposed on a dc level at 1/16 and 15/16 full scale input.

Supply Voltage Rejection Ratio (SVRR)

The variation in the amplitude of the given signal when the supply voltage is changed by 1V.

Signal–to–Noise Ratio

The ratio of the RMS signal amplitude to the RMS value of "noise" which is defined as the sum of all other spectral components including harmonics, but excluding DC with a full–scale analog input signal.

Total Harmonic Distortion (THD)

The RMS addition of all peaks in a Fast Fourier Transform measurement, which occur at integer multiples of the fundamental frequency of the input signal.

Test Levels

Level 1	100% production tested
Level 2	100% production tested at 25°C and sample tested at specified temperatures
Level 3	Sample tested only
Level 4	Parameter is guaranteed by design and characteristics testing
Level 5	Parameter is a typical value only

GENERAL CIRCUIT DESCRIPTION

The VP8708 is an analog video input interface capable of digitising signals at sample rates upto 30MHz.

The multiplexer uses the logic conditions on the selection pins (IO, I1) to select one of upto three signals applied to the video inputs (VIN0, VIN1, VIN2). This signal is then clamped to the required dc level by the action of the clamp control logic. The output of the multiplexer passes through the AGC amplifier, where the gain of the signal is adjusted such that after going through the driver amplifier, the signal fills the desired portion of the ADC range. This input to the ADC also drives three reference comparators which supply the signals necessary to control the clamp and AGC circuitry.

Two modes of operation are available; these being determined by the relative occurrences, during the sync and rear porch periods, of logic pulses at the GATE A and GATE B inputs.

Mode 1 (see Fig. 3) is employed initially to allow the device to reach its optimum operation point. The gain and dc level of the signal are roughly adjusted to set the sync level to ADC code 0 and the peak level to ADC code 255. This allows rapid recovery of the video synchronisation pulses.

If the GATE A and GATE B pulses become distinct (see Fig. 4) then the VP8708 will switch into mode 2. In this configuration a more sophisticated control scheme is used in order to produce a 'fixed'digitised output from the device: Whilst the GATE A pulse (which must be within the sync period) is high, the sync level is adjusted to code 0,.Similarly, the black level is adjusted to code 64 if the GATE B pulse occurs during the rear porch periods. Peak level control is always active such that maximum digital output will tend to lie below code 240. Nominal input signals, 1Vp–p, should have a peak output level equal to code 213.

For the device to operate, two external capacitors must be connected to the AGC and CLAMP pins. An optional external resistor may be attached to the RPEAK input to alter the maximum charge/discharge current into these capacitors. This varies the loop response time.

The format of the output data, updated at the sample rate, is determined by the logic level on the OF pin. The OF pin may also be used to force the outputs to a high impedance state.

The DEC ('decouple') pin is not connected on the VP8708. On similar devices (e.g. TDA8708) an external capacitor may be attached to this pin to stabilise the ADC reference voltage. The VP8708 has an internally stable reference and thus requires one less external component.

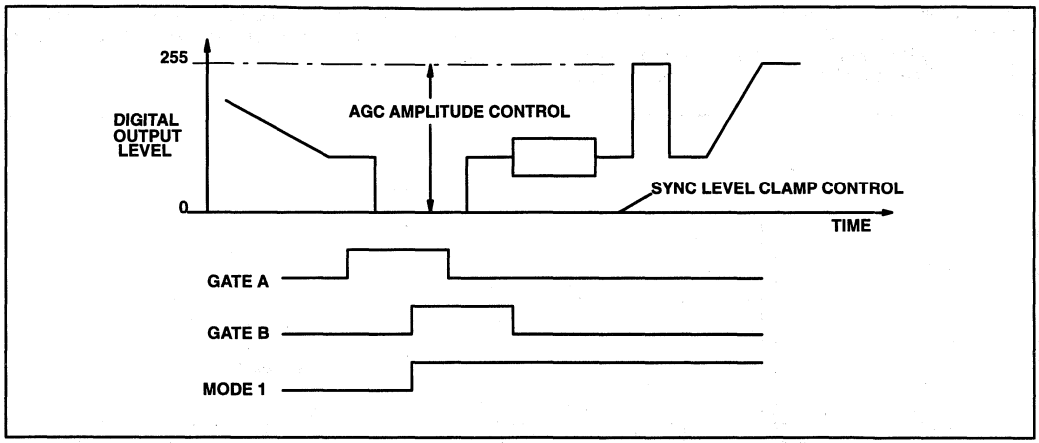


Fig. 3 Control mode 1

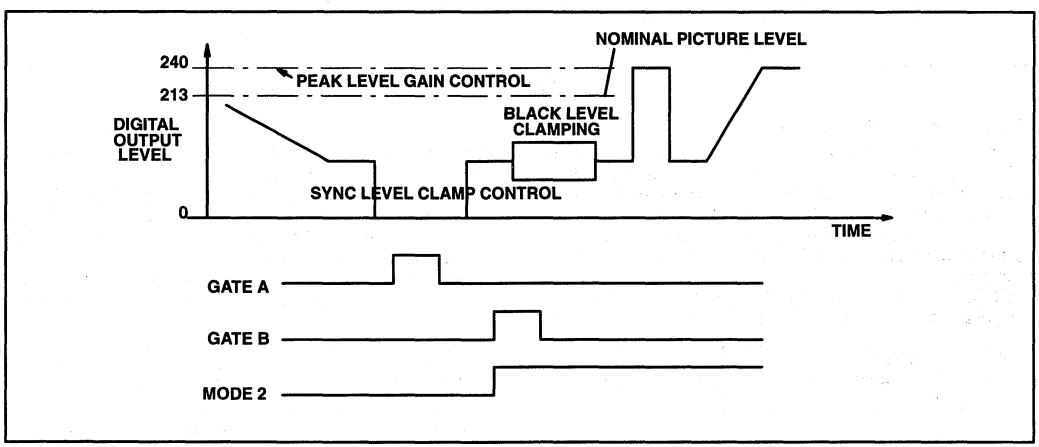


Fig. 4 Control mode 2

VIDEO INPUTS

Each of the three video inputs may be selected with the selection pins I0 and I1. Table 2 shows the action of these pins.

I1	I0	SELECTED INPUTS
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 Video input selection

OUTPUT FORMAT (OF PIN)

The format of the output data is selectable via the OF pin as shown in Table 3. To improve noise immunity, a small (10nF) capacitor may be connected between this pin and ground if binary operation is required.

OF	D0 TO D7
0	Active, two's complement
Open	Active, binary
1	High impedance

Table 3 Output format control

ANOUT AND ADCIN

The analog output (ANOUT) and ADC input (ADCIN) pins should have an external anti-aliasing filter connected betwen them. Care must be taken to ensure that the filter input impedance and filter output levels are in accordance with the specifications.

As an evaluatuion tool, two 1.5kΩ resistors may be used to form a potential divider between ANOUT and AV_{CC}. The centre tap of this divider can then be used to connect the signal to ADCIN. It should be noted however, that dynamic device performance will not be maximum.

TIMING INFORMATION

Fig. 5 depicts the system relationship between sampling edge offset and output data.

The analog input signal is sampled t_{ds} seconds after the rising edge of the clock signal. Old data will remain valid for at least t_{ho} and new data will become valid after at most t_d. Data may be latched on either the falling or rising edges of the clock signal.

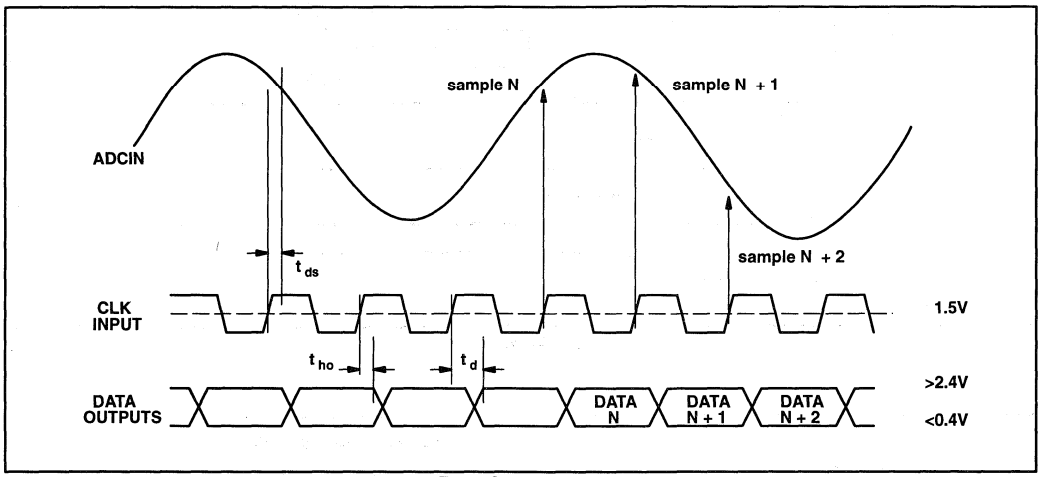


Fig. 5 System timing

AGC AND CLAMP CONTOL

In both mode 1 and 2, AGC and clamp control is achieved by the charging and discharging of two external capacitors attached to the AGC and CLAMP pins. Suggested values for these capacitors are C_{agc}=220nF and C_{clp}=18nF.

For correct device operation, the relative occurrences of the control pulses at the GATE A and GATE B pins must be as given below:

MODE 1 – GATE A and GATE B must overlap, GATE B being delayed with respect to GATE A. This will ensure that the signal fills the complete ADC range and thus allows quick recovery of the video sync pulses.

MODE 2 – GATE A must occur wholly within the sync period GATE B must occur wholly within the rear porch. This will tend to hold the output signal amplitude below code 240, the black level at code 64, and the sync tip at code 0.

Table 4 shows the control action of the device with reference to the logic states of the GATE A and GATE B inputs.

GATE A	GATE B	MODE	DIGITAL OUTPUT CODE	I_{AGC}	I_{CLP}
1	↑	Device will enter mode 1			
		1	Output >255	$-I_{peak}$	+5µA
		1	Output <255	+5µA	–
		1	Output >0	–	+5µA
		1	Output <0	+5µA	$-I_{peak}$
↑ ↓ 0	0 0 ↑	This control sequence will switch the device into mode 2.			
0	1	2	Output >240	$-I_{peak}$	+50µA
0	1	2	Output >64	–	+50µA
0	1	2	Output <64	–	–50µA
0	0	2	Output >240	$-I_{peak}$	–
1	0	2	Output >240	$-I_{peak}$	–
1	0	2	Output >0	–5µA	–
1	0	2	Output <0	+5µA	–

Table 4: Mode 1/Mode 2 control

PIN	NAME	DESCRIPTION
1	D7	Data Output Bit 7 (MSB)
2	D6	Data Output Bit 6
3	D5	Data Output Bit 5
4	D4	Data Output Bit 4
5	CLK	Clock Input
6	DV_{CC}	Digital Supply Voltage
7	OV_{CC}	Output Buffer Supply Voltage
8	DGND	Digital Ground
9	OF	Output Format/Chip Enable
10	D3	Data Output Bit 3
11	D2	Data Output Bit 2
12	D1	Data Output Bit 1
13	D0	Data Output Bit 0 (LSB)
14	I0	Input Selection Bit 0

PIN	NAME	DESCRIPTION
15	I1	Input Selection Bit 1
16	VIN0	Video Input 0
17	VIN1	Video Input 1
18	VIN2	Video Input 2
19	ANOUT	Analog Output
20	ADCIN	ADC Input
21	DEC	Not Connected – VP8708 is internally stable
22	AV_{CC}	Analog Supply Voltage
23	AGND	Analog Ground
24	CLAMP	Clamp Capacitor
25	AGC	AGC Capacitor
26	GATE B	Black Level Control Pulse
27	GATE A	Sync Level Control Pulse
28	RPEAK	Peak Current Resistor

PCB CONSTRUCTION

As with all high speed analog to digital converters, careful consideration must be given to the PCB layout.

In general, the best results will be obtained by tying all grounds to a 'solid' low impedance ground plane. Separate analog and digital ground planes will also help. Device connections to the ground plane should be as short as possible.

Supply decoupling is important when dealing with mixed analog and digital signals, it can provide a feedback path for the digital output currents. The VP8708 should therefore be decoupled as close to the supply pins as possible. Good quality, high frequency, low inductance capacitors. Isolation may be further improved by adding series inductors to the supplies.

Jitter and noise on the clock pin and its reference to ground must be minimised. Long clock lines should be avoided and all lines correctly terminated.

A typical application circuit is shown below.

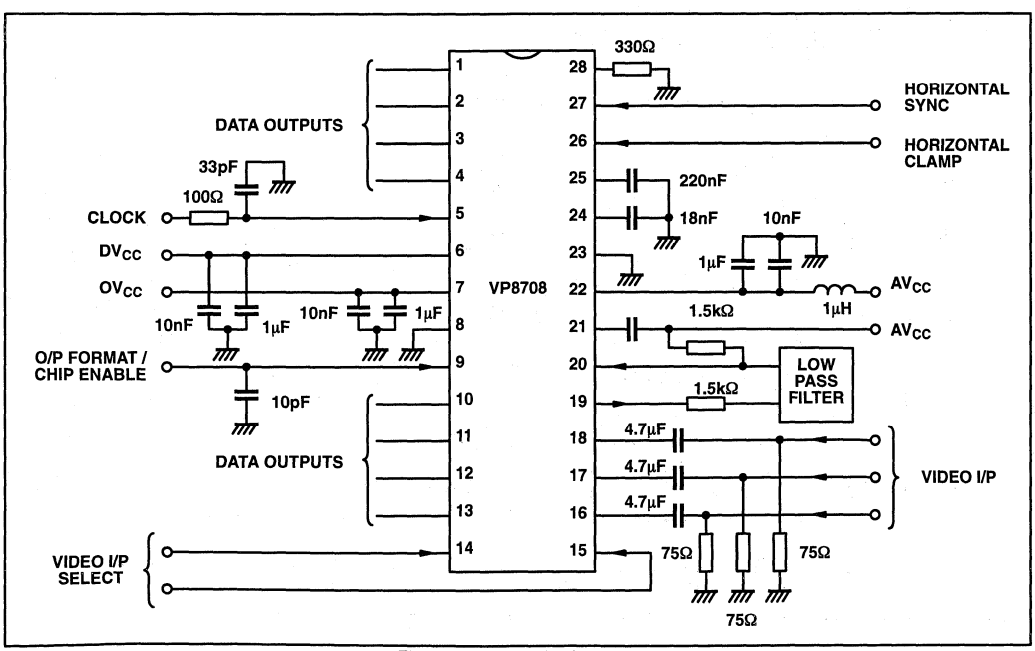


Fig. 6 Typical application circuit

VP87A8

32MHz 8–BIT ANALOG VIDEO INPUT INTERFACE

The VP87A8 is an analog input interface dessigned for video signal conditioning and digitisation.

Operating from a single +5V supply, the VP87A8 includes an input multiplexer, Video amplifier with clamp and gain control, an on board reference and a buffered 8–bit ADC capable of digitising signals upto the Nyquist limit.

Video signals may be supplied to the VP87A8 either directly to the ADC, or via one of three multimplexed inputs for signal conditioning. The conditioned analog signal (with appropriate gain and clamping) is available as output prior to digitisation. The coded data, updated at the sample rate, is available in either binary or two's complement format via the 3–state TTL output buffers.

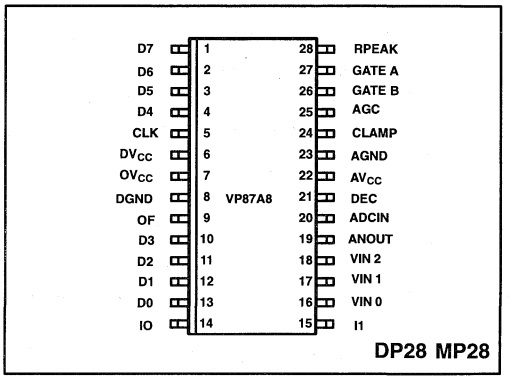


Fig. 1 Pin connections – top view

FEATURES

- Direct replacement for TDA8708A†
- 32MHz sample rate
- Selectable data format
- Internal ADC reference
- Clamp and AGC functions
- 3–state TTL outputs

†GEC Plessey also offer direct replacements for Philips
TDA8708 (GPS part no VP8708)
TDA8709A (GPS part no VP87A9)

ORDERING INFORMATION

VP87A8B CG DPAS (Commercial – Plastic DIL)
VP87A8B CG MPES (Commercial – Miniature Plastic)

ABSOLUTE MAXIMUM RATINGS

Supply voltages; (AV_{CC}, DV_{CC}, OV_{CC})	+7V
Supply differential	±1V
Ground differential	±1V
Video input voltage	AV_{CC}
Output current	10mA

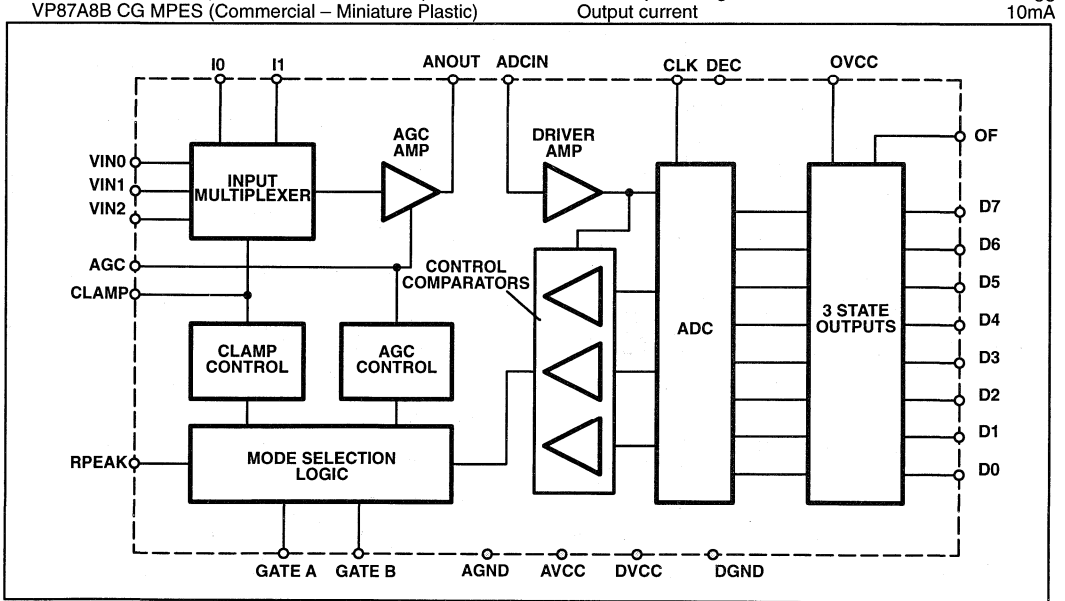


Fig. 2 System block diagram

RECOMMENED OPERATING CONDITIONS

Supply voltages; AVCC, DVCC, OVCC	+5V
Supply differential	0V
Ground differential	0V
Video input voltage	1Vp–p

OPERATING TEMPERATURE RANGE

Commercial	0°C to +70°C (still–air ambient)

THERMAL CHARACTERISTICS

Storage temperature range	–65°C to +150°C
Lead temperature (soldering 11 seconds)	+265°C
THERMAL RESISTANCE, MP PACKAGE	
Junction to ambient (Θ_{ja})	84°C/W
Junction to case (Θ_{jc})	32°C/W
THERMAL RESISTANCE ,DP PACKAGE	
Junction to ambient (Θ_{ja})	55°C/W
Junction to case (Θ_{jc})	14°C/W

ELECTRICAL CHARACTERISTICS:

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
POWER SUPPLY								
Analog supply voltage	AV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Digital supply voltage	DV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Output supply voltage	OV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Analog supply current	AI_{CC}	25 FULL	1 4		60	 70	mA mA	AV_{CC}=5.0V AV_{CC}=5.5V
Digital supply current	DI_{CC}	25 FULL	1 4		13	 17	mA mA	DV_{CC}=5.0V DV_{CC}5.5V
Output supply current	OI_{CC}	25 FULL	1 4		12	 16	mA mA	$OV_{CC=5.0V}$ OV_{CC}=5.5V
Power dissipation	P	1 4			425	 570	mW mW	V_{CC}=5.0V V_{CC}=5.5V
VIDEO INPUTS								
Input range	V_{IN} (p–p)	FULL	4	0.5	1.0	1.6	V	
Input impedance	$\|Z_{IN}\|$	25	1	18	20	22	kΩ	f_{in}=6MHZ
Input capacitance	C_{in}	25	5		2		pF	f_{in}=6MHZ
I1, IO GATE A, GATE B TTL INPUTS								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input current HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input current LOW	I_{il}	25 FULL	1 4	–150 –200			µA µA	V_i=0.4V V_i=0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			10 20	µA µA	V_i=3.6V V_i=3.6V
RPEAK INPUT								
Peak capacitor charge/discharge current	I_{PEAK}	FULL	4		80	150	µA	R_{peak} = 0Ω

ELECTRICAL CHARACTERISTICS: (cont.)

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
AGC CONTROL INPUT								
AGC voltage for minimum gain	V_{agc}	25	4		2.7		V	
AGC voltage for maximum gain	V_{agc}	25	4		3.9		V	
AGC output current	I_{agc}	25	1		*			* See table 4
CLAMP CONTROL INPUT								
Clamp voltage	V_{clp}	25	1		3.5		V	ADC output = 128
Clamp output current	I_{clp}	25	1		*			* See table 4
VIDEO AMPLIFIER OUTPUTS								
Internal current source	I_{19}	25	4	2			mA	
DC Output voltage for black level	V_{blk}	FULL	4		AV_{CC}– 2.24		V	
AC Output voltage (peak–peak)	V_{19}	FULL	4		1.33		V	
Output impedance	Z_{19}	25	4		45		Ω	
CLK INPUT								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input current LOW	I_{il}	25 FULL	1 4	–150 –200			µA µA	V_i = 0.4V V_i = 0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			10 20	µA µA	V_i= 3.6V V_i= 3.6V
Input impedance	$\|Z_{IN}\|$	25	4		3.5		kΩ	
Input capacitance	C_{clk}	25			5		pF	
Maximum frequency	f_{max}	FULL	4	30	32		MHz	
OF INPUT (3–STATE control)								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input voltage 3–STATE	V_z	25	1		1.4		V	
Input current LOW	I_{il}	25 FULL	1 4	–175 –200			µA µA	V_i=0.4V V_i=0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			500 700	µA µA	V_i=3.6V V_i=3.6V

ELECTRICAL CHARACTERISTICS: (cont.)

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
ADCIN INPUT								
Input voltage	V_{adc}	FULL	4		AV_{CC}– 2.41		V	For Code 0
Input voltage	V_{adc}	FULL	4		AV_{CC}– 1,41		V	For Code 255
Input voltage amplitude (p–p)	V_{20}	FULL	4		1.0		V	
Input current	I_{adc}	25	1		1		µA	
Input impedance	Z_{adc}	25	1		14		MΩ	
Input capacitance	C_{adc}	25	4		5		pF	
DIGITAL OUTPUTS								
Output voltage LOW	V_{ol}	25 FULL	1 4			0.4 0.4	V V	I_{oi}=2mA I_{oi}=2mA
Output voltage HIGH	V_{oh}	25 FULL	1 4	2.4 2.4			V V	$I_{oh=}$–0.4mA I_{oh}=–0.4mA
3–STATE Output current	I_{OZ}	25	1		2		µA	
ADC PERFORMANCE								
Static differential non – linearity	DNL	25 FULL	1 4		±0.5 ±0.5		lsb lsb	
Static integral non – linearity	INL	25 FULL	1 4		±1 ±1		lsb lsb	
Dynamic integral non – linearity	INL	25 FULL	1 4		±2 ±2		lsb lsb	
VIDEO AMPLIFIER DYNAMIC PERFORMANCE								
–3dB Bandwidth	f3dB	25	4		20		MHz	
Differential gain	G_d	25	4		2		%	
Differential phase	$\varnothing_d$	25	4		2		degrees	
Gain range	ΔG	25	4	–3		7	dB	
Crosstalk between VIN inputs		25	4		–60		dB	
Signal–to–noise ratio	SNR	25	4		55		dB	
Supply voltage ripple rejection	SVRR	25	4		0.5		%/V	
ANALOG SIGNAL PROCESSING								*f_{clk} = 30MHz
–3dB Bandwidth	f3dB	25	4		15		MHz	
Differential gain	G_d	25	4		2		%	
Differential phase	$\varnothing_d$	25	4		2		degrees	
Total harmonic distortion	THD	25	4		–55		dB	
Supply voltage ripple rejection	SVRR	25	4		5		%/V	

ELECTRICAL CHARACTERISTICS: (cont.)

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
TIMING (note 2)								
Sampling delay	t_{ds}	FULL	4		3		ns	
Output hold time	t_{ho}	FULL	4	5			ns	
Output delay time	t_d	FULL	4			20	ns	
3 State delay time for enble	t_{ez}	FULL	4			25	ns	
3 State delay time for disable	t_{dz}	FULL	4			25	ns	

ELECTRICAL CHARACTERISTIC DEFINITIONS

Analog –3dB Bandwidth ADC

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis, is 3dB down on the DC level.

Differential Non–Linearity (DNL)

The deviation of any code width from an ideal 1LSB step size.

Integral Non–Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least–square curve–fit.

Differential Gain (G_d) and Phase ($\varnothing_d$)

The difference in gain/phase at the ADC output when a 17.5 IRE units peak to peak, 3.58MHz input signal is superimposed on a dc level at 1/16 and 15/16 full scale input.

Supply Voltage Rejection Ratio (SVRR)

The variation in the amplitude of the given signal when the supply voltage is changed by 1V.

Signal–to–Noise Ratio

The ratio of the RMS signal amplitude to the RMS value of "noise" which is defined as the sum of all other spectral components including harmonics, but excluding dc with a full–scale analog input signal.

Total Harmonic Distortion (THD)

The RMS addition of all peaks in a Fast Fourier Transform measurement, which occur at integer multiples of the fundamental frequency of the input signal.

Test Levels

Level 1	100% production tested
Level 2	100% production tested at 25°C and sample tested at specified temperatures
Level 3	Sample tested only
Level 4	Parameter is guaranteed by design and characteristics testing
Level 5	Parameter is a typical value only

GENERAL CIRCUIT DESCRIPTION

The VP87A8 is an analog video input interface capable of digitising signals at sample rates upto 32MHz.

The multiplexer uses the logic conditions on the selection pins (IO, I1) to select one of upto three signals applied to the video inputs (VIN0, VIN1, VIN2). The output of the multiplexer passes through the AGC amplifier, where the gain of the sigal is adjusted and the signal clamped to the required DC level such that after going through the driver amplifier, the signal fills the desired portion of the ADC range. This input to the ADC also drives three reference comparators which supply the signals necessary to control the clamp and AGC circuitry.

Two modes of operation are available; these being determined by the relative occurrences, during the sync and rear porch periods, of logic pulses at the GATE A and GATE B inputs.

Mode 1 (see Fig. 3) is employed initially to allow the device to reach its optimum operation point. The gain and DC level of the signal are roughly adjusted to set the sync level to ADC code 0 and the peak level to ADC code 255. This allows rapid recovery of the video synchronisation pulses.

If the GATE A and GATE B pulses become distinct (see Fig. 4) then the VP87A8 will switch into mode 2. In this configuration a more sophisticated control scheme is used in order to produce a 'fixed' digitised output from the device: Whilst the GATE A pulse (which must be within the sync period) is high, the sync level is adjusted to code 0.Similarly, the black level is adjusted to code 64 if the GATE B pulse occurs during the rear porch periods. Peak level control is always active such that maximum digital output will tend to lie below code 248. Nominal input signals, 1Vp–p, should have a peak output level equal to code 213.

For the device to operate, two external capacitors must be connected to the AGC and CLAMP pins. An optional external resistor may be attached to the RPEAK input to alter the maximum charge/discharge current into these capacitors. This varies the loop response time.

The format of the output data, updated at the sample rate, is determined by the logic level on the OF pin. The OF pin may also be used to force the outputs to a high impedance state.

The DEC ('decouple') pin is not connected on the VP87A8. On similar devices (e.g. TDA8708A) an external capacitor may be attached to this pin to stabilise the ADC reference voltage. The VP87A8 has an internally stable reference and thus requires one less external component.

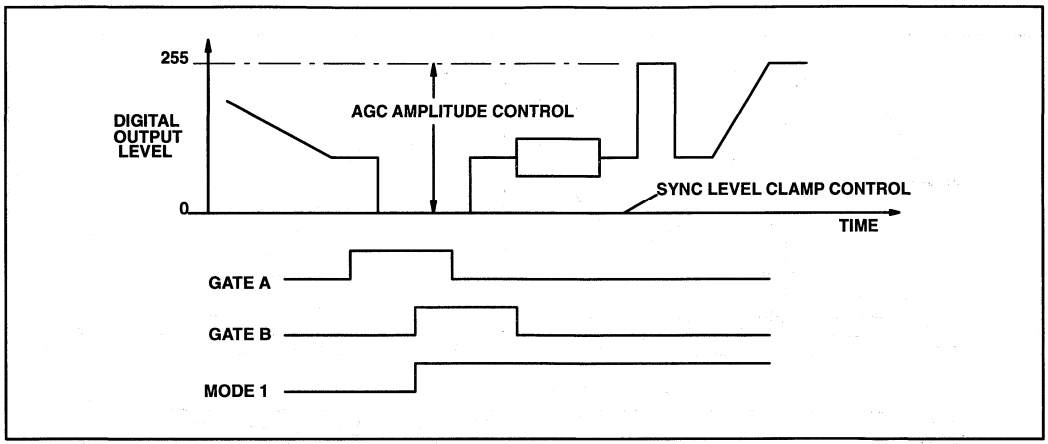


Fig. 3 Control mode 1

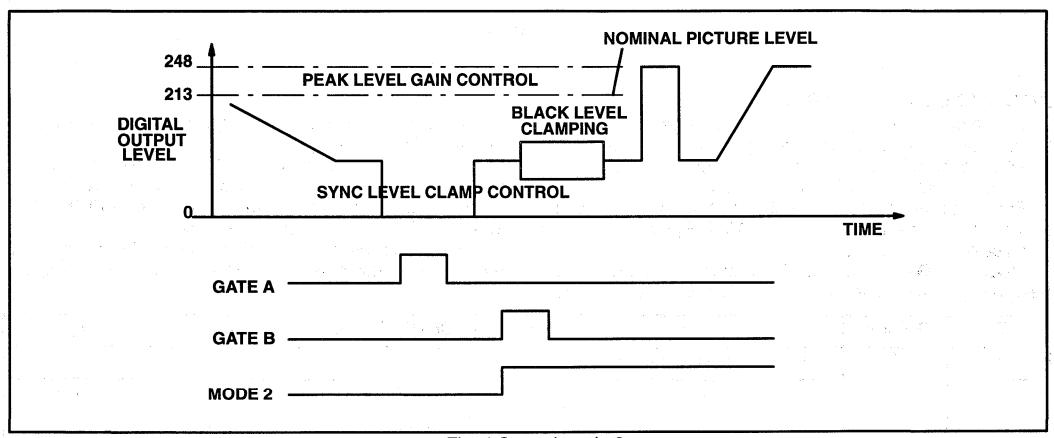


Fig. 4 Control mode 2

VIDEO INPUTS

Each of the three video inputs may be selected with the selection pins I0 and I1. Table 2 shows the action of these pins.

I1	I0	SELECTED INPUTS
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 2 Video input selection

OUTPUT FORMAT (OF PIN)

The format of the output data is selectable via the OF pin as shown in Table 3. To improve noise immunity, a small (10nF) capacitor may be connected between this pin and ground if binary operation is required.

OF	D0 TO D7
0	Active, two's complement
Open	Active, binary
1	High impedance

Table 3 Output format control

ANOUT AND ADCIN

The analog output (ANOUT) and ADC input (ADCIN) pins should have an external anti–aliasing filter connected betwen them. Care must be taken to ensure that the filter input impedance and filter output levels are in accordance with the specifications.

As an evaluatuion tool, two resistors (680Ω and 2200Ω) may be used to form a potential divider between ANOUT and AV_{CC}. The centre tap of this divider can then be used to connect the signal to ADCIN. It should be noted however, that dynamic device performance will not be maximum.

TIMING INFORMATION

Fig. 5 depicts the system relationship between sampling edge offset and output data.

The analog input signal is sampled t_{ds} seconds after the rising edge of the clock signal. Old data will remain valid for at least t_{ho} and new data will become valid after at most t_d. Data may be latched on either the falling or rising edges of the clock signal.

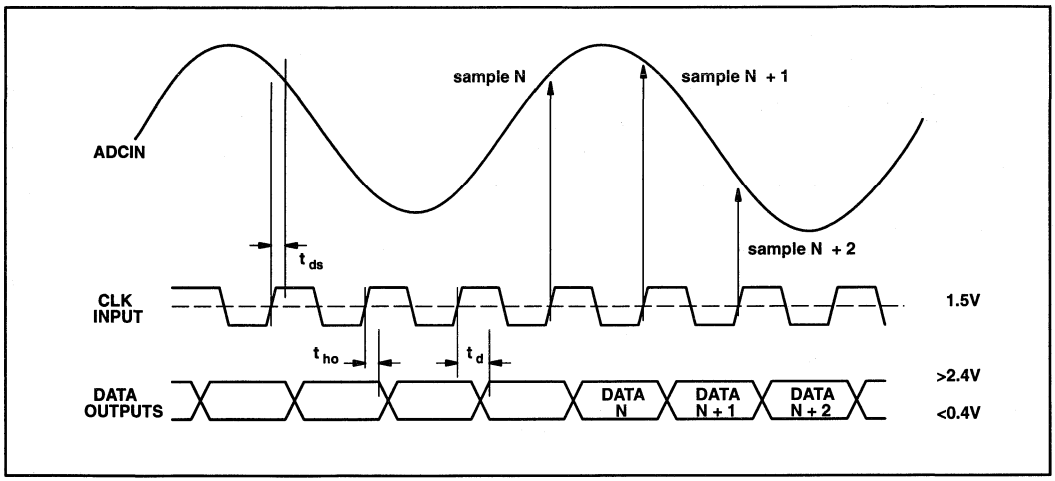


Fig. 5 System timing

AGC AND CLAMP CONTOL

In both mode 1 and 2, AGC and clamp control is acheived by the charging and discharging of two external capacitors attached to the AGC and CLAMP pins. Suggested values for these capacitors are C_{agc}=220nF and C_{clp}=18nF.

For correct device operation, the relative occurrences of the control pulses at the GATE A and GATE B pins must be as given below:

MODE 1 – GATE A and GATE B must overlap, GATE B being delayed with respect to GATE A. This will ensure that the signal fills the complete ADC range and thus allows quick recovery of the video sync pulses.

MODE 2 – GATE A must occur wholly within the sync period GATE B must occur wholly within the rear porch. This will tend to hold the output signal amplitude below code 248, the black level at code 64, and the sync tip at code 0.

Table 4 shows the control action of the device with reference to the logic states of the GATE A and GATE B inputs.

GATE A	GATE B	MODE	DIGITAL OUTPUT CODE	I_{AGC}	I_{CLP}
1	↑	Device will enter mode 1			
		1	Output >255	$-I_{peak}$	+5µA
		1	Output <255	+5µA	–
		1	Output >0	–	+5µA
		1	Output <0	+5µA	$-I_{peak}$
↑ ↓ 0	0 0 ↑	This control sequence will switch the device into mode 2.			
0	1	2	Output >248	$-I_{peak}$	+50µA
0	1	2	Output >64	–	+50µA
0	1	2	Output <64	–	–50µA
0	0	2	Output >248	$-I_{peak}$	–
1	0	2	Output >248	$-I_{peak}$	–
1	0	2	Output >0	–5µA	–
1	0	2	Output <0	+5µA	–

Table 4: Mode 1/Mode 2 control

PIN	NAME	DESCRIPTION
1	D7	Data Output Bit 7 (MSB)
2	D6	Data Output Bit 6
3	D5	Data Output Bit 5
4	D4	Data Output Bit 4
5	CLK	Clock Input
6	DV_{CC}	Digital Supply Voltage
7	OV_{CC}	Output Buffer Supply Voltage
8	DGND	Digital Ground
9	OF	Output Format/Chip Enable
10	D3	Data Output Bit 3
11	D2	Data Output Bit 2
12	D1	Data Output Bit 1
13	D0	Data Output Bit 0 (LSB)
14	I0	Input Selection Bit 0

PIN	NAME	DESCRIPTION
15	I1	Input Selection Bit 1
16	VIN0	Video Input 0
17	VIN1	Video Input 1
18	VIN2	Video Input 2
19	ANOUT	Analog Output
20	AD_CIN	ADC Input
21	DEC	Not Connected – VP87A8 is internally stable
22	AV_{CC}	Analog Supply Voltage
23	AGND	Analog Ground
24	CLAMP	Clamp Capacitor
25	AGC	AGC Capacitor
26	GATE B	Black Level Control Pulse
27	GATE A	Sync Level Control Pulse
28	RPEAK	Peak Current Resistor

Table 4 Pin descriptions

PCB CONSTRUCTION

As with all high speed analog to digital converters, careful consideration must be given to the PCB layout.

In general, the best results will be obtained by tying all grounds to a 'solid' low impedance ground plane. Separate analog and digital ground planes will also help. Device connections to the ground plane should be as short as possible.

Supply decoupling is important when dealing with mixed analog and digital signals, it can provide a feedback path for the digital output currents. The VP87A8 should therefore be decoupled as close to the supply pins as possible. Good quality, high frequency, low inductance capacitors. Isolation may be further improved by adding series inductors to the supplies.

Jitter and noise on the clock pin and its reference to ground must be minimised. Long clock lines should be avoided and all lines correctly terminated.

A typical application circuit is shown below.

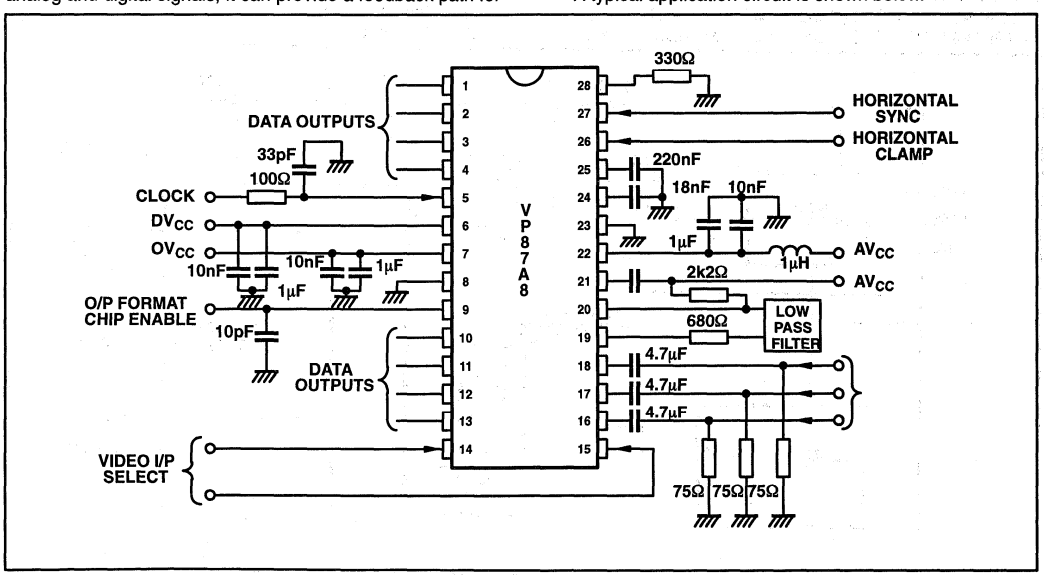


Fig. 6 Typical application circuit

VP87A9

30MHz 8–BIT ANALOG VIDEO INPUT INTERFACE

The VP87A9 is an analog input interface designed for video signal conditions and digitisation.

Operating from a single +5V supply, the VP87A9 includes an input multiplexer, video amplifier with internal clamp and variable gain, an on–board reference and a buffered 8–bit ADC capable of digitising signals up to the Nyquist limit.

Video signals may be supplied to the VP87A9 either directly to the ADC, or via one of three multiplexed inputs for signal conditioning. The conditioned analog signal (with appropriate gain and clamping) is available as output prior to digitisation. The coded data, updated at the sample rate, is available in either binary or two's complement format via the 3–state TTL output buffers.

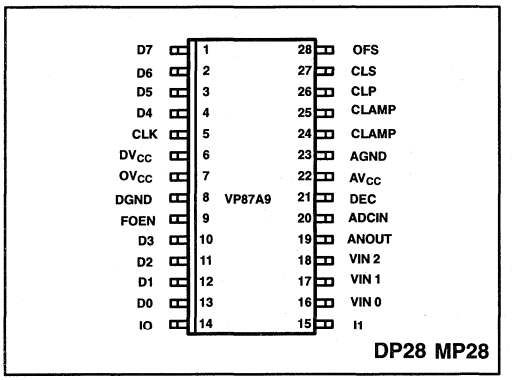


Fig. 1 Pin connections – top view

FEATURES

- Direct replacement for TDA8709A†
- 30MHz sampling rate
- Internal clamp to code 16 or 128
- Varaible signal gain
- Selectable data format
- Internal ADC reference
- 3–state TTL outputs

†GEC Plessey also offer direct replacements for Philips
TDA8708 (GPS part no VP8708)
TDA8708A (GPS part no VP87A8)

ORDERING INFORMATION

VP87A9A CG DPAS (Commercial – Plastic DIL)
VP87A9A CG MPES (Commercial – Miniature Plastic)

ABSOLUTE MAXIMUM RATINGS

Supply voltages; AV_{CC}, DV_{CC}, OV_{CC}	+5V
Supply differential	±1V
Ground differential	±1V
Video input voltage	AVCC
Output current	10mA

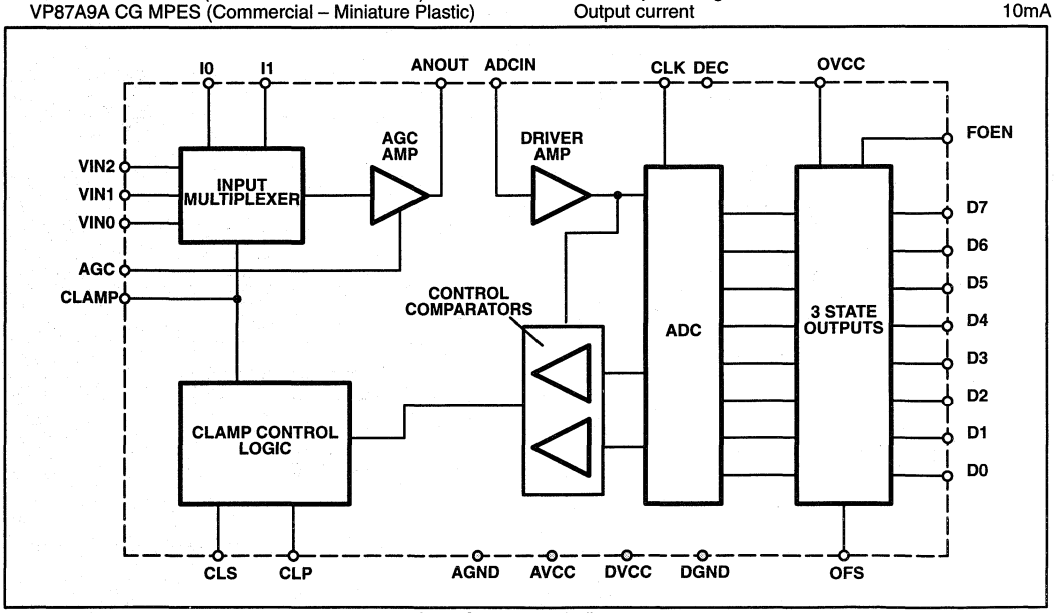


Fig. 2 System block diagram

RECOMMENDED OPERATING CONDITIONS

Supply voltages; AV_{CC}, DV_{CC}, OV_{CC}	+5V
Supply differential	/V
Ground differential	0V
Video input voltage	1Vp–p

OPERATING TEMPERATURE RANGE

Commercial	0°C to +70°C (still–air ambient)

THERMAL CHARACTERISTICS

Storage temperature range	–65°C to +150°C
Lead temperature (soldering 11 seconds)	+265°C
THERMAL RESISTANCE DP PACKAGE	
Junction to ambient (Θ_{ja})	55°C/W
Junction to case (Θ_{jc})	14°C/W
THERMAL RESISTANCE, MP PACKAGE	
Junction to ambient (Θ_{ja})	84°C/W
Junction to case (Θ_{jc})	32°C/W

ELECTRICAL CHARACTERISTICS: DC CHARACTERISTICS

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
POWER SUPPLY								
Analog supply voltage	AV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Digital supply voltage	DV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Output supply voltage	OV_{CC}	25 FULL	1 4	4.5 4.5	5.0 5.0	5.5 5.5	V V	
Analog supply current	AI_{CC}	25 FULL	1 4		55 55	65 75	mA mA	
Digital supply current	DI_{CC}	25 FULL	1 4		10 10	15 20	mA mA	
Output supply current	OI_{CC}	25 FULL	1 4		10 10	15 20	mA mA	
Power dissipation	P	25 FULL	1 4		375 375	525 635	mW mW	
VIDEO INPUTS								
Input range	V_{IN} (p–p)	FULL	4	0.5	1.0	1.5	V	
Input impedance	$\|Z_{IN}\|$	FULL	4	18	20	22	kΩ	f_{in}=6MHZ
Input capacitance	C_{in}	25	5		2		pF	f_{in}=6MHZ
I0, I1, CLS CLP TTL INPUTS								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input current LOW	I_{il}	25 FULL	1 4	–150 –200			µA µA	V_i=0.4V V_i=0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			10 20	µA µA	V_i=3.6V V_i=3.6V

ELECTRICAL CHARACTERISTICS: DC CHARACTERISTICS (cont.)

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=T_{full} =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
GAIN CONTROL INPUT								
Voltage for minimum gain	V_{gc}	25	4		1.8		V	See Fig. 5
Voltage for maximum gain	V_{gc}	25	4		3.8		V	See Fig.5
Input current	I_{gc}	25	1		1		µA	
Gain/Temperature stability	G_T	*	4		5		%	See Fig.5
CLAMP CONTROL INPUT								
Clamp voltage	V_{clp}	25	4		*			* See Fig. 4
Clamp output current	I_{clp}	25	1		*			* See Table 4
VIDEO AMPLIFIER OUTPUTS								
Internal current source	I_{19}	25	4	2			mA	
DC Output voltage for black level	V_{blk}	FULL	4		AV_{CC} 2.00		V	CLS=1
					AV_{CC} 2.60		V	CLS=0
AC Output voltage (peak–peak)	V_{19}	FULL	4		1.35		V	
Output impedance	Z_{19}	25			40		Ω	
CLK INPUT								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input current LOW	I_{il}	25 FULL	1 4	–150 –200			µA µA	V_i = 0.4V V_i = 0.4V
Input current HIGH	I_{ih}	25 FULL	1 4			10 20	µA µA	V_i= 3.6V V_i= 3.6V
Input impedance	$\|Z_{IN}\|$	25	4		3.5		kΩ	
Input capacitance	C_{clk}	25			5		pF	
Maximum frequency	f_{max}	FULL	4	30			MHz	
FOEN INPUT (3–state control)								
Input voltage LOW	V_{il}	25 FULL	1 4			0.8 0.8	V V	
Input voltage HIGH	V_{ih}	25 FULL	1 4	2.0 2.0			V V	
Input voltage 3–STATE	V_z	25	1		1.4		V	
Input current LOW	I_{il}	25 FULL	1 4	–175 –200			µA µA	V_i=0.4V V_i=0.4V
Input current HIGH	I_{ih}	25 FULL	1			50 70	µA µA	V_i=3.6V V_i=3.6V

ELECTRICAL CHARACTERISTICS: DC CHARACTERISTICS (cont.)

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
ADCIN INPUT								
Input voltage	V_{adc}	FULL	4		AV_{CC}– 2.50		V	For Code 0
Input voltage	V_{adc}	FULL	4		AV_{CC}– 1.50		V	For Code 255
Input voltage amplitude (p–p)	V_{20}	FULL	4		1.0		V	
Input current	I_{adc}	25	1		1		µA	
Input impedance	Z_{adc}	25	1		14		MΩ	
Input capacitance	C_{adc}	25	4		5		pF	
DIGITAL OUTPUTS								
Output voltage LOW	V_{ol}	25 FULL	1 4			0.4 0.4	V V	I_{ol}=2mA I_{ol}=2mA
Output voltage HIGH	V_{oh}	25 FULL	1 4	2.4 2.4			V V	I_{oh}=–0.4mA I_{oh}=–0.4mA
3–STATE Output current	I_{OZ}	25	1		2		µA	
ADC PERFORMANCE								
Static differential non – linearity	DNL	25 FULL	1 4		±0.5 ±0.5		lsb lsb	
Static integral non – linearity	INL	25 FULL	1 4		±1 ±1		lsb lsb	
Dynamic integral non – linearity	INL	25 FULL	1 4		±2 ±2		lsb lsb	
VIDEO AMPLIFIER DYNAMIC PERFORMANCE								
–3dB Bandwidth	f3dB	25	4		20		MHz	
Differential gain	G_d	25	4			2	%	
Differential phase	$\varnothing_d$	25	4			2	degrees	
Gain range	ΔG	25	4	–4.5		10	dB	
Crosstalk between VIN inputs		25	4		–60		dB	
Signal–to–noise ratio	SNR	25	4		55		dB	
Gain supply Rejection Ratio	GSSR	25	4		–30		dB	V_{gc} = 2.8V
ANALOG SIGNAL PROCESSING								*f_{clk} = 30MHz
Differential phase	$\varnothing_d$	25	4		2		degrees	
Total harmonic distortion	THD	25	4		–55		dB	
Supply voltage ripple rejection	SVRR	25	4		0.5		%/V	
–3dB Bandwidth	f3dB	25	4		15		MHz	
Differential gain	G_d	25	4		2		%	

ELECTRICAL CHARACTERISTICS: DC CHARACTERISTICS (cont.)

Test conditions (unless otherwise stated): AV_{CC}, DV_{CC}, OV_{CC}=5V±0.5V, AGND/DGND shorted together, Temp=$T_{full.}$ =0 to + 70°C.

Parameter	Symbol	Temp (°C)	Test level	Value			Units	Conditions
				Min	Typ	Max		
TIMING*								* f_{clk}=30MHz C_L=15pF I_{0l}=2mA
Sampling delay	t_{ds}	FULL	4		3		ns	
Output hold time	t_{ho}	FULL	4	5			ns	
Output delay time	t_d	FULL	4			20	ns	
3 State delay time for enable	t_{ez}	FULL	4			25	ns	
3 State delay time for disable	t_{dz}	FULL	4			25	ns	

ELECTRICAL CHARACTERISTIC DEFINITIONS

Analog –3dB Bandwidth of the ADC

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis, is 3dB down on the DC level.

Differential Non–Linearity (DNL)

The deviation of any code width from an ideal LSB step size.

Integral Non–Linearity (INL)

The deviation of the centre of each code from a reference line which has been determined by a least–square curve–fit.

Differential Gain (G_d) and Phase ($\varnothing_d$)

The difference in gain/phase at the ADC output when a 17.5 IRE units peak to peak, 3.58MHz input signal is superimposed on a DC level at 1/16 and 15/16 full scale input.

Supply Voltage Rejection Ratio (SVRR)

The variation in the the given signal when the supply voltage is changed by 1V.

Signal–to–Noise Ratio

The ratio of the RMS signal amplitude to the RMS value of "noise" which is defined as the sum of all other spectral components including harmonics, but excluding dc with a full–scale analog input signal.

Total Harmonic Distortion (THD)

The RMS addition of all peaks in a Fast Fourier Transform measurement, which occur at integer multiples of the fundamental frequency of the input signal.

Test Levels

Level 1	100% production tested
Level 2	100% production tested at 25°C and sample tested at specified temperatures
Level 3	Sample tested only
Level 4	Parameter is guaranteed by design and characteristics testing
Level 5	Parameter is a typical value only

GENERAL CIRCUIT DESCRIPTION

The VP 87A9 is an analog video input interface capable of digitising signals at sample rates upto 30MHz.

The multiplexer uses the logic conditions on the selection pins (IO, I1) to select one of upto three signals applied to the video inputs (VIN0, VIN1, VIN2). This signal is then clamped to the required level by the action of the clamp control logic. The output of the multiplexer passes through the video amplifier, where the gain of the signal is adjusted as determined by the voltage on the 'GAIN' pin, such that after going through the driver amplifier, the signal fills the desired portion of the ADC range (see Fig. 3). This input to the ADC also drives two reference comparators which supply the signals necessary to control the clamp circuitry.

The control circuitry may switched, via the state of the 'CLS' pin, such that the input signal is clamped to either ADC code 16 (for luminance or R,G,B signals) or to ADC code 128 (for chrominance or colour difference signals). For the device to operate, an external capacitor must be connected to the CLAMP pin. This capacitor is then charged/discharged as appropriate during the clamping period (when 'CLP' is taken high).

The format of the output data, updated at the sample rate, is determined by the logic level on the OFS pin. The FOEN pin may also be used to force the outputs to a high impedance state.

The DEC (decouple') pin is not connected on the VP87A9. On similar devices (e.g. TDA8709A) an external capacitor may be attached to this pin to stabilise the ADC reference voltage. The VP87A9 has an internally stable reference and thus requires one less external component.

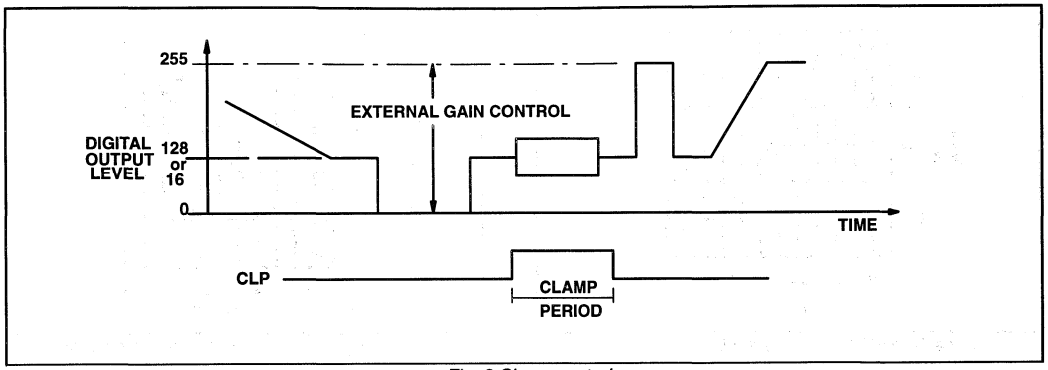


Fig. 3 Clamp control

VIDEO INPUTS

Each of the three video inputs may be selected with the selection pins I0 and I1. Table 3 shows the action of these pins.

I1	I0	SELECTED INPUTS
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

Table 3 Video input selection

OUTPUT FORMAT & ENABLE (OFS FOEN PINS)

The format of the output data is selectable via the OFS pin as shown in Table 4. When the FOEN pin is taken high, the TTL outputs will enter a high impedance state regardless of other signals.

FOEN	OFS	OUTPUT STATES
0	0	Active, Binary
0	1	Active, Two's Complement
1	X	High Impedance

Table 4 Output format control

ANOUT AND ADCIN

The analog output (ANOUT) and ADC input (ADCIN) pins should have an external anti–aliasing filter connected betwen them. Care must be taken to ensure that the filter input impedance and filter output levels are in accordance with the specifications.

As an evaluatuion tool, two resistors (680Ω and 22kΩ) may be used to form a potential divider between ANOUT and AV_{CC}. The centre tap of this divider can then be used to connect the signal to ADCIN. It should be noted however, that dynamic device performance will not be maximum.

TIMING INFORMATION

Fig. 6 depicts the system relationship between sampling edge offset and output data.

The analog input signal is sampled t_{ds} seconds after the rising edge of the clock signal. Old data will remain valid for at least t_{ho} and new data will become valid after at most t_d. Data may be latched on either the falling or rising edges of the clock signal.

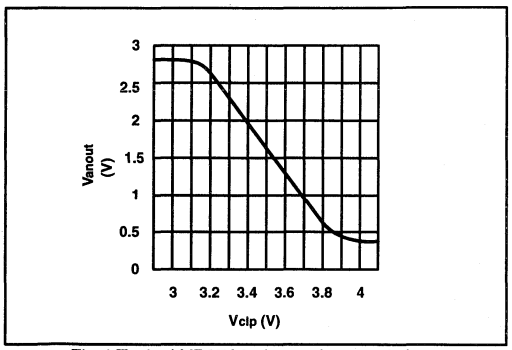


Fig.4 Typical VP87A9 clamp characteristic

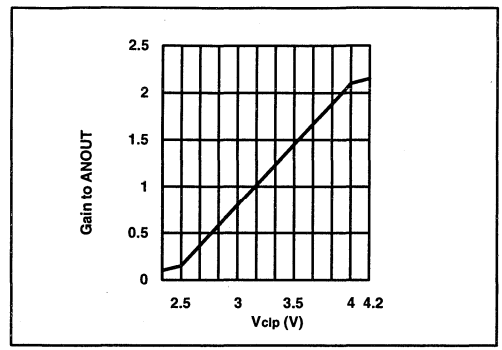


Fig.5 Typical VP87A9 clamp characteristic

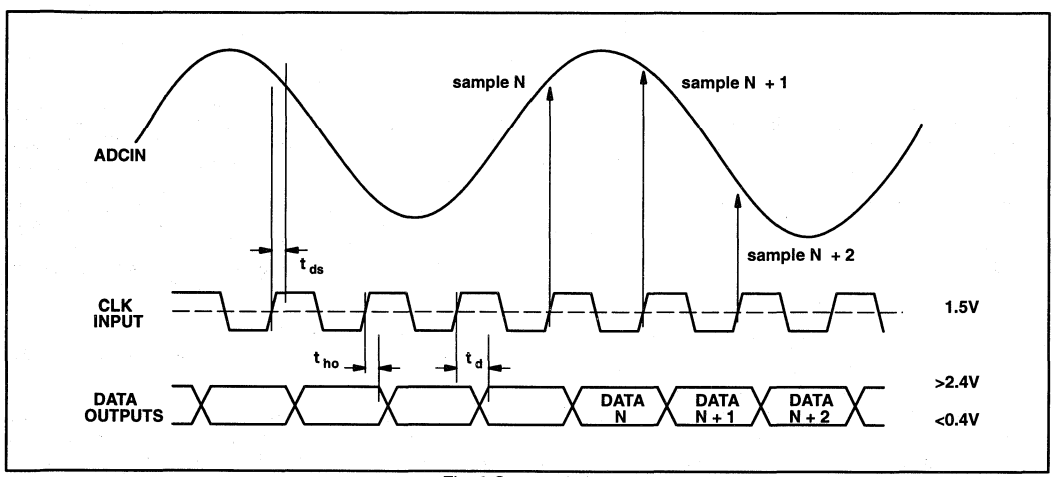


Fig. 6 System timing

CLAMP AND GAIN CONTROL

The typical clamp control characteristic is depicted in Fig. 4 and the control action shown in Table 4.

The clamping circuitry operates whilst 'CLP' is at a logic–high state. It is therefore important to ensure that 'CLP' is only taken high during the breeseway, colour–burst and rear porch. The speed at which the clamp circuitry gains alignment is dependant on both the length of the 'CLP' pulse and also the value of capacitor attached to the 'CLAMP' pin (smaller values of capacitor and /or longer 'CLP' pulse will increase the clamp response).

If necessary the clamping operation may be forced externally by applying a voltage source to the 'CLAMP' pin. In this case the response time is limited by the system bandwidth.

CLS	CLP	ADC OUTPUT CODE	I_{clp}
1	1	Output < 128 Output > 128	+50µA –50µA
X	0	X	0
0	1	Output < 16 Output >16	+50µA –50µA

Table 4: Clamp output current

PIN	NAME	DESCRIPTION
1	D7	Data Output Bit 7 (MSB)
2	D6	Data Output Bit 6
3	D5	Data Output Bit 5
4	D4	Data Output Bit 4
5	CLK	Clock Input
6	DV_{CC}	Digital Supply Voltage
7	OV_{CC}	Output Buffer Supply Voltage
8	DGND	Digital Ground
9	FOEN	Fast output enable
10	D3	Data Output Bit 3
11	D2	Data Output Bit 2
12	D1	Data Output Bit 1
13	D0	Data Output Bit 0 (LSB)
14	I0	Input Selection Bit 0

PIN	NAME	DESCRIPTION
15	I1	Input Selection Bit 1
16	VIN0	Video Input 0
17	VIN1	Video Input 1
18	VIN2	Video Input 2
19	ANOUT	Analog Output
20	ADCIN	ADC Input
21	DEC	Not Connected – VP87A9 is internally stable
22	AV_{CC}	Analog Supply Voltage
23	AGND	Analog Ground
24	CLAMP	Clamp Capacitor
25	GAIN	Gain control input
26	CLP	Clamp Pulse
27	CLS	Clamp level select
28	OFS	Output format select

PCB CONSTRUCTION

As with all high speed analog to digital converters, careful consideration must be given to the PCB layout.

In general, the best results will be obtained by tying all grounds to a 'solid' low impedance ground plane. Separate analog and digital ground planes will also help. Device connections to the ground plane should be as short as possible.

Supply decoupling is important when dealing with mixed analog and digital signals, it can provide a feedback path for the digital output currents. The VP87A9 should therefore be decoupled as close to the supply pins as possible. Good quality, high frequency, low inductance capacitors. Isolation may be further improved by adding series inductors to the supplies.

Jitter and noise on the clock pin and its reference to ground must be minimised. Long clock lines should be avoided and all lines correctly terminated.

A typical application circuit is shown in Fig. 7.

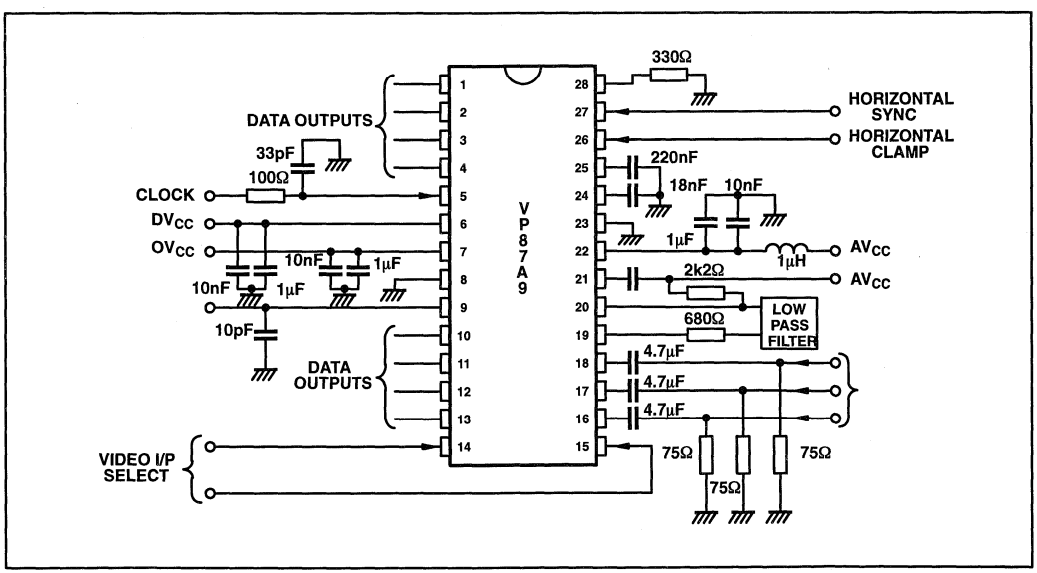


Fig. 7 Typical application circuit

Section 5

Micropower Fixed Voltage References

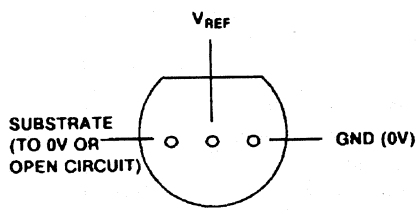
GEC PLESSEY
SEMICONDUCTORS

REF12Z/REF12D

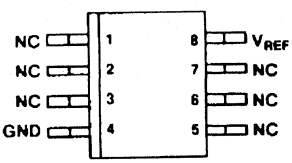
1.26V MICROPOWER PRECISION REFERENCE

The REF12Z and REF12D are integrated circuits using the bandgap principle to provide a precise stable reference voltage of 1.26V. There are two package options available: REF12Z in a plastic 3-pin TO-92 and REF12D in a miniature surface mount package (MP8).

These references feature a recommended operating current of 90μA to 2.5mA which make them ideal for all low power and battery applications.



REF12Z (TO-92) - BOTTOM VIEW



REF12D (MP8) - TOP VIEW

Fig.1 Pin connection

FEATURES

- Low Knee Current - typically 80 microamps
- Ideal for Battery Operation - 113 microwatts
- REF12Z - 3 lead TO-92 Plastic Package
- REF12D - Miniature Plastic Surface Mount Package (MP8)
- Tight Initial V_{REF} Tolerance ±1%
- Low Temperature Coefficient
- Low Slope Resistance
- Low Cost
- Operation over Industrial Temperature Range

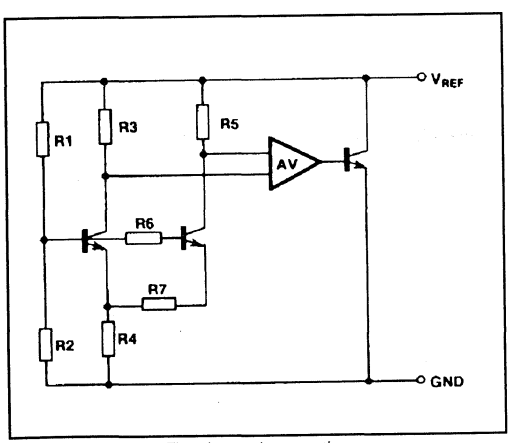


Fig.2 Internal connections

ORDERING INFORMATION

Device Type	Operating Temperature	Package
REF12Z	-40°C to +85°C	TO-92
REF12D	-40°C to +85°C	MP8

ABSOLUTE MAXIMUM RATINGS

Reference current	2.5mA
Operating temperature range:	
REF12Z	-40 to +85°C
REF12D	-40 to +85°C
Storage temperature	-55 to +125°C
Storage temperature for a max. time of 10ns:	
within 1.59mm of the seating plane	300°C
within 0.80mm of the seating plane	265°C

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

T_{amb} = 25°C, C_S = 470nF (see Fig.3)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	1.247	1.26	1.273	V	
Slope resistance (Note 1)	R_{REF}		2.5	4.0	Ω	I_{REF} = 150μA to 2.5mA Note 1
Turn-on (knee) current	I_{ON}		80	90	μA	
Recommended operating current range	I_{REF}	0.09		2.5	mA	
Temperature coefficient (Note 2)	TC V_{REF}		40	80	ppm/°C	REF12Z } Note 2
			30	80	ppm/°C	REF12D }
RMS noise voltage	E_N		1.0		μV/√Hz	0.1Hz to 25kHz
Turn-on time	T_{ON}		0.4		ms	} I_{REF} = 1.5mA
Turn-off time	T_{OFF}		15		ms	
Turn-on time	T_{ON}		5		ms	} I_{REF} = 1.5mA
Turn-off time	T_{OFF}		110		ms	

NOTES

1. Slope resistance (R_{REF})

   Slope resistance is defined as

   $$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

2. Reference voltage temperature coefficient (TC V_{REF})

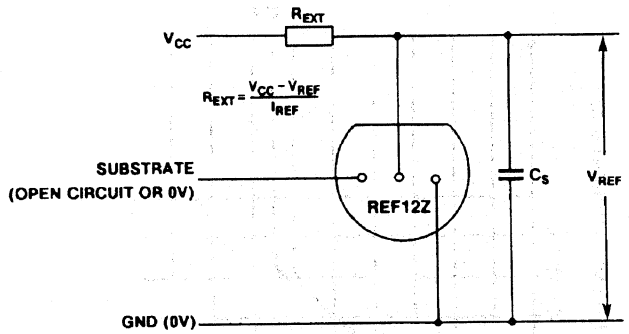
   This is the normalised reference voltage change over temperature, divided by the change in temperature.

   It is expressed in ppm/°C

   $$TC\ V_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

   ΔT = temperature change in °C

   ΔV_{REF} = change in reference voltage over temperature change ΔT



NOTE: In order to achieve optimum operation, a stabilising capacitor ($C_S \geq 470nF$) should be connected between V_{REF} and 0V as shown.

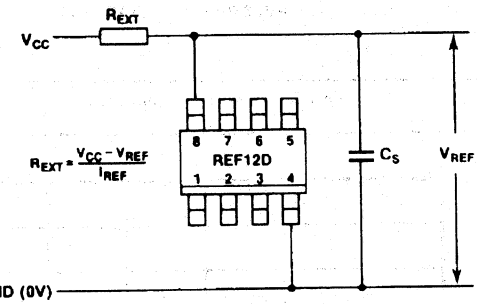


Fig.3 Connection diagram

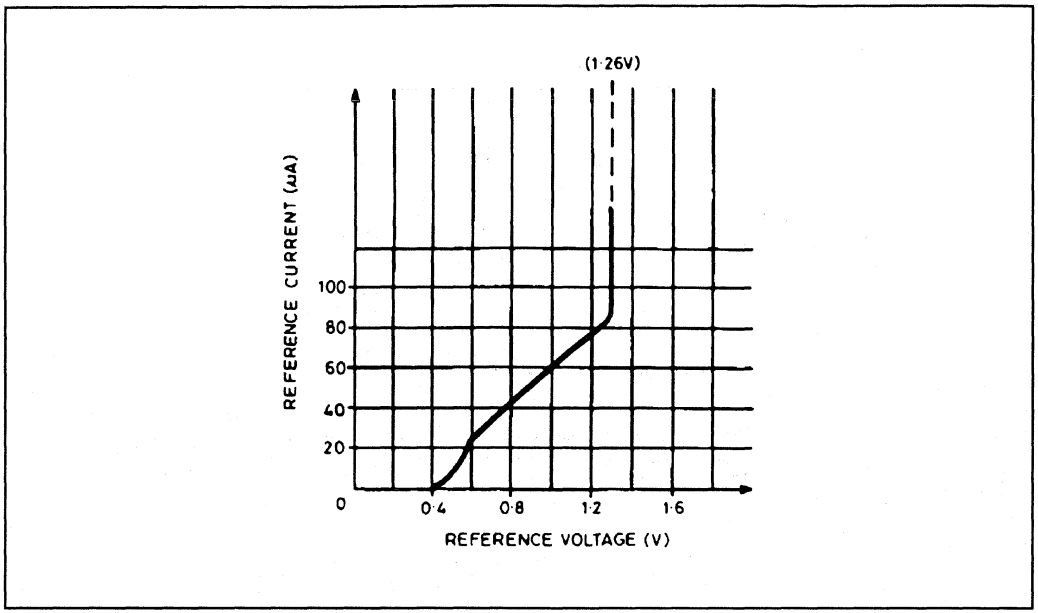


Fig.4 Typical reference characterics

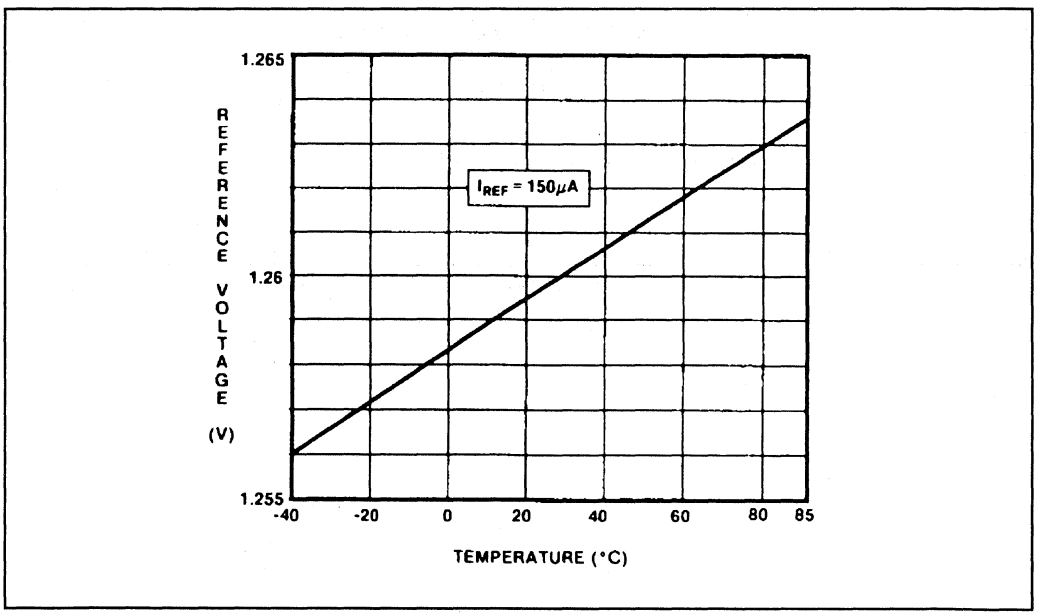


Fig.5 Typical temperature characteristic

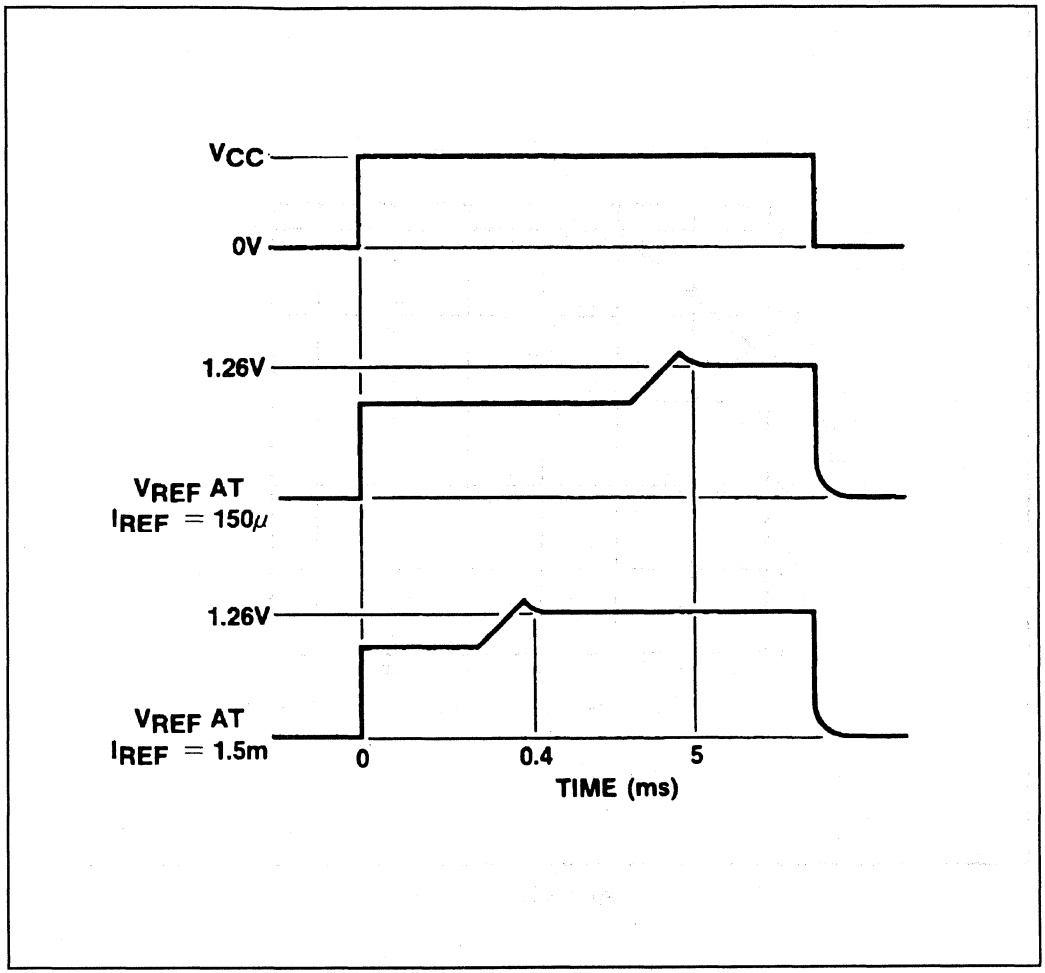


Fig.6 Typical response time

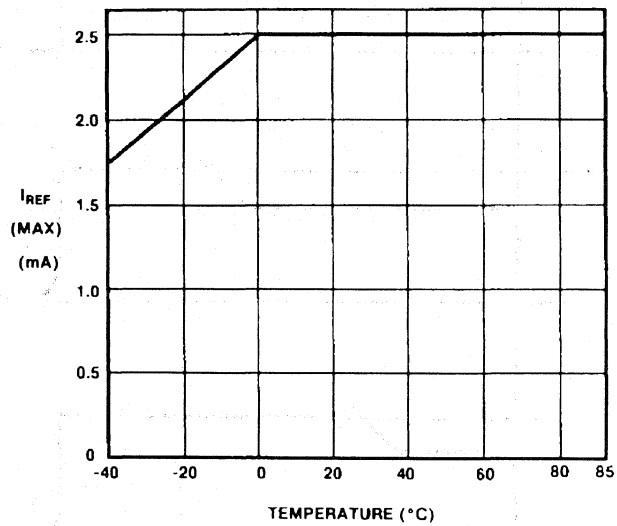


Fig. 7 Typical derating curve

REF25Z/REF25D

2.5V MICROPOWER PRECISION REFERENCE

The REF25Z and REF25D are integrated circuits using the bandgap principle to provide a precise stable reference voltage of 2.5V without the need for an external shaping capacitor. There are two package options available: REF25Z in a plastic 3-pin TO-92 and REF25D in a miniature surface mount package (MP8).

These references feature a recommended operating current of 60μA to 5mA which make them ideal for all low power and battery applications.

FEATURES

- Low Knee Current - typically 40 microamps
- Ideal for Battery Operation - 150 microwatts
- Internally Shaped
- REF25Z - 3 lead TO-92 Plastic Package
- REF25D - Miniature Plastic Surface Mount Package (MP8)
- Tight Initial V_{REF} Tolerance ±1%
- Low Temperature Coefficient
- Low Slope Resistance
- Low Cost
- Operation over Industrial Temperature Range

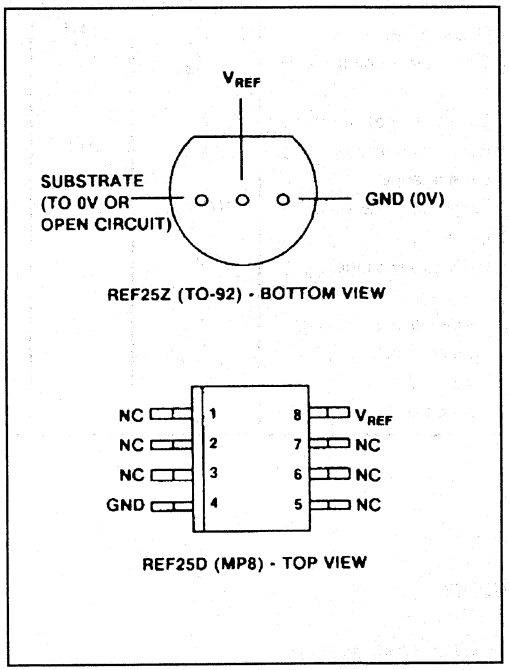


Fig.1 Pin connection

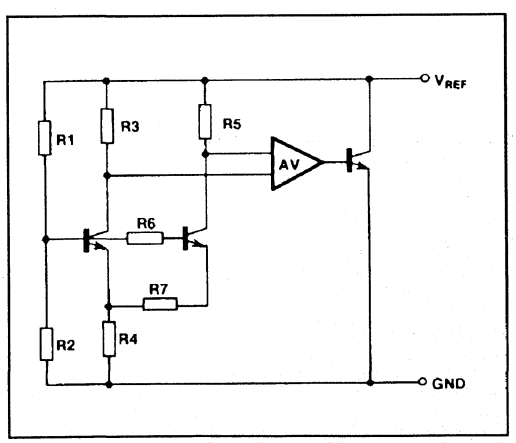


Fig.2 Internal connections

ORDERING INFORMATION

Device Type	Operating Temperature	Package
REF25Z	-40°C to +85°C	TO-92
REF25D	-40°C to +85°C	MP8

ABSOLUTE MAXIMUM RATINGS

Reference current	5mA
Operating temperature range:	
REF25Z	-40 to +85°C
REF25D	-40 to +85°C
Storage temperature	-55 to +125°C
Storage temperature for a max. time of 10ns:	
within 1.59mm of the seating plane	300°C
within 0.80mm of the seating plane	265°C

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

T_{amb} = 25°C, I_{REF} = 150µA

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	2.475	2.500	2.525	V	
Slope resistance (Note 1)	R_{REF}		1.2	2.0	Ω	REF25Z } I_{REF} = 150µA
			1.2	2.0	Ω	REF25D } to 5mA
Turn-on (knee) current	I_{ON}		40		µA	
Recommended operating current range	I_{REF}	0.06		5.0	mA	
Temperature coefficient	TC V_{REF}		35	110	ppm/°C	REF25Z } Note 2
(Note 2)			35	80	ppm/°C	REF25D }
RMS noise voltage	E_N		13		µV	1kHz to 10kHz
Turn-on time	T_{ON}		80		µs	
Turn-off time	T_{OFF}		7		µs	
Turn-on time	T_{ON}		65		µs	} I_{REF} = 500µA
Turn-off time	T_{OFF}		2		µs	

NOTES

1. Slope resistance (R_{REF})

   Slope resistance is defined as

   $$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

2. Reference voltage temperature coefficient (TC V_{REF})

   This is the normalised reference voltage change over temperature, divided by the change in temperature.
   It is expressed in ppm/°C

   $$TC\ V_{REF} = \frac{\Delta V_{REF} \times 10^6\ \text{ppm/°C}}{V_{REF} \times \Delta T}$$

   ΔT = temperature change in °C

   ΔV_{REF} = change in reference voltage over temperature change ΔT

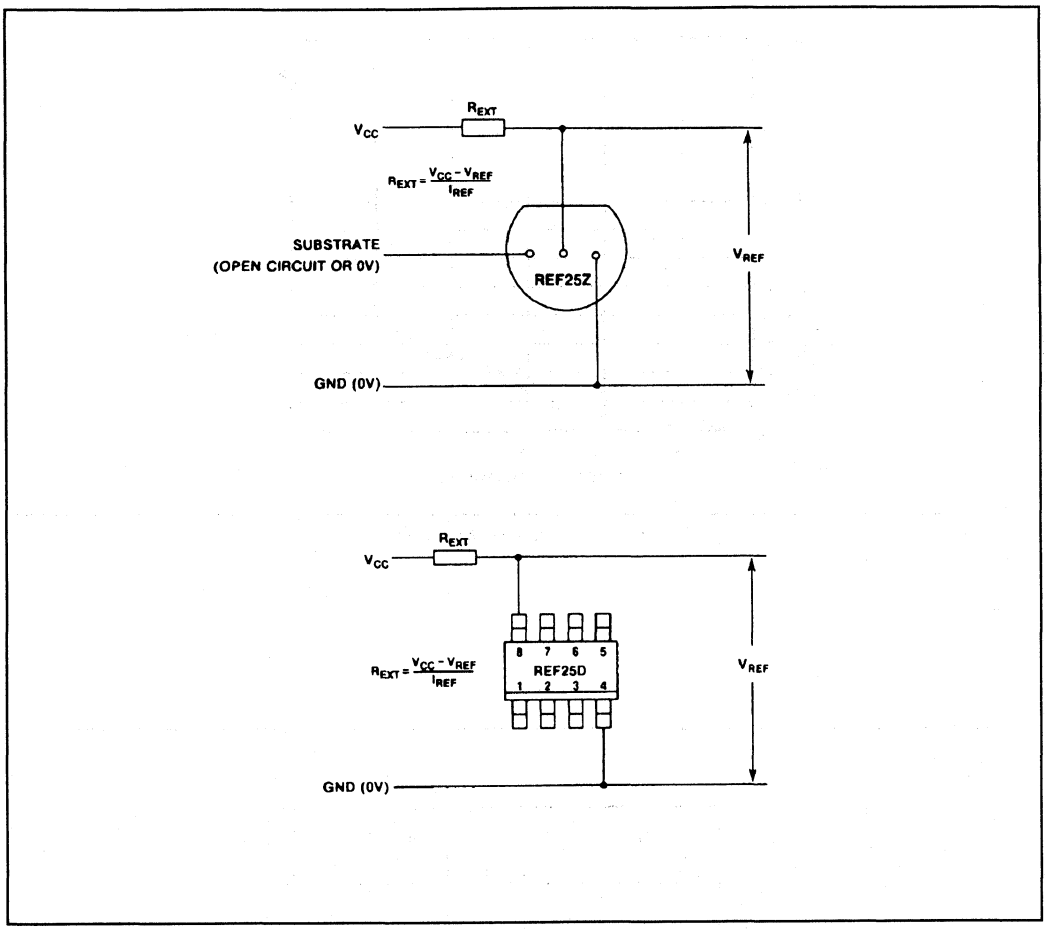


Fig.3 Connection diagram

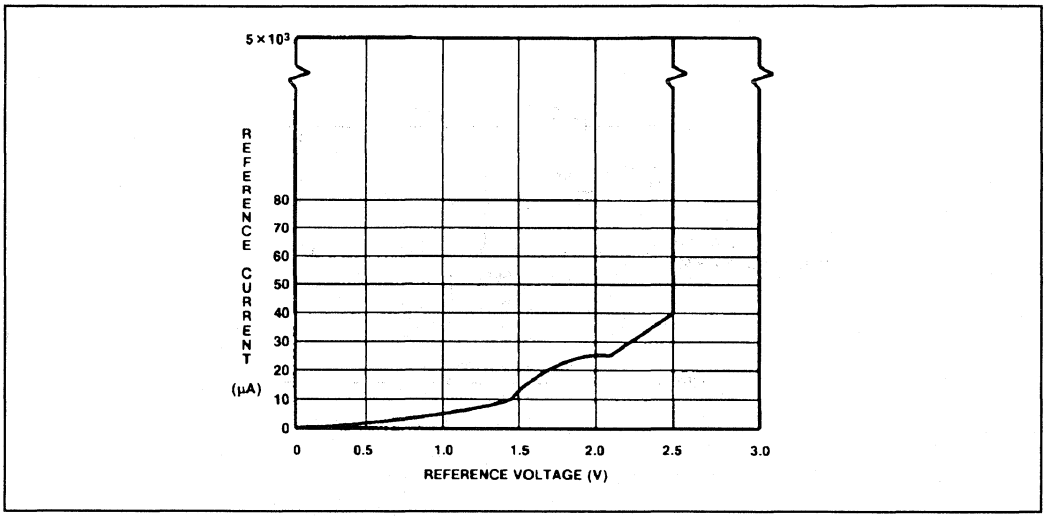


Fig.4 Typical reference characteristic

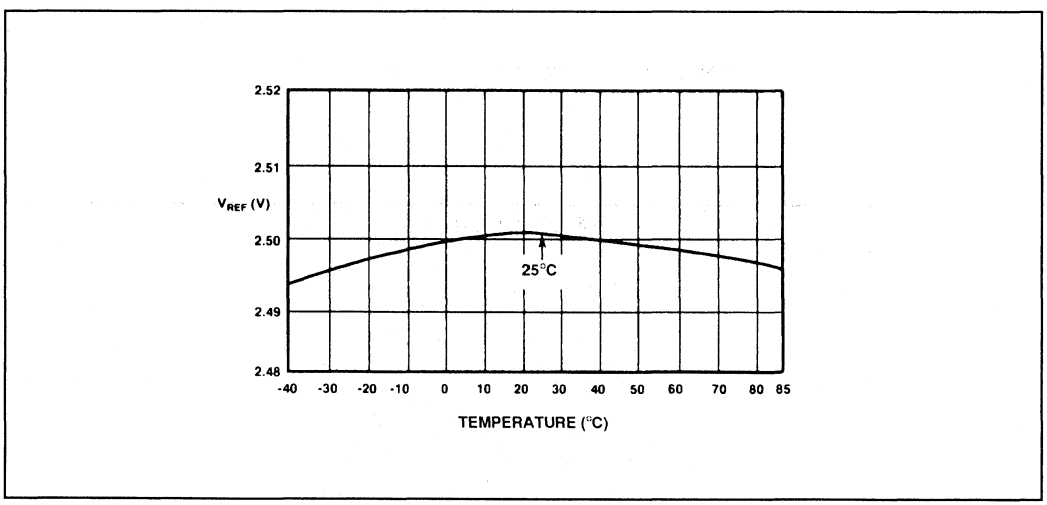


Fig.5 Typical temperature characteristics at I_{REF} = 150μA

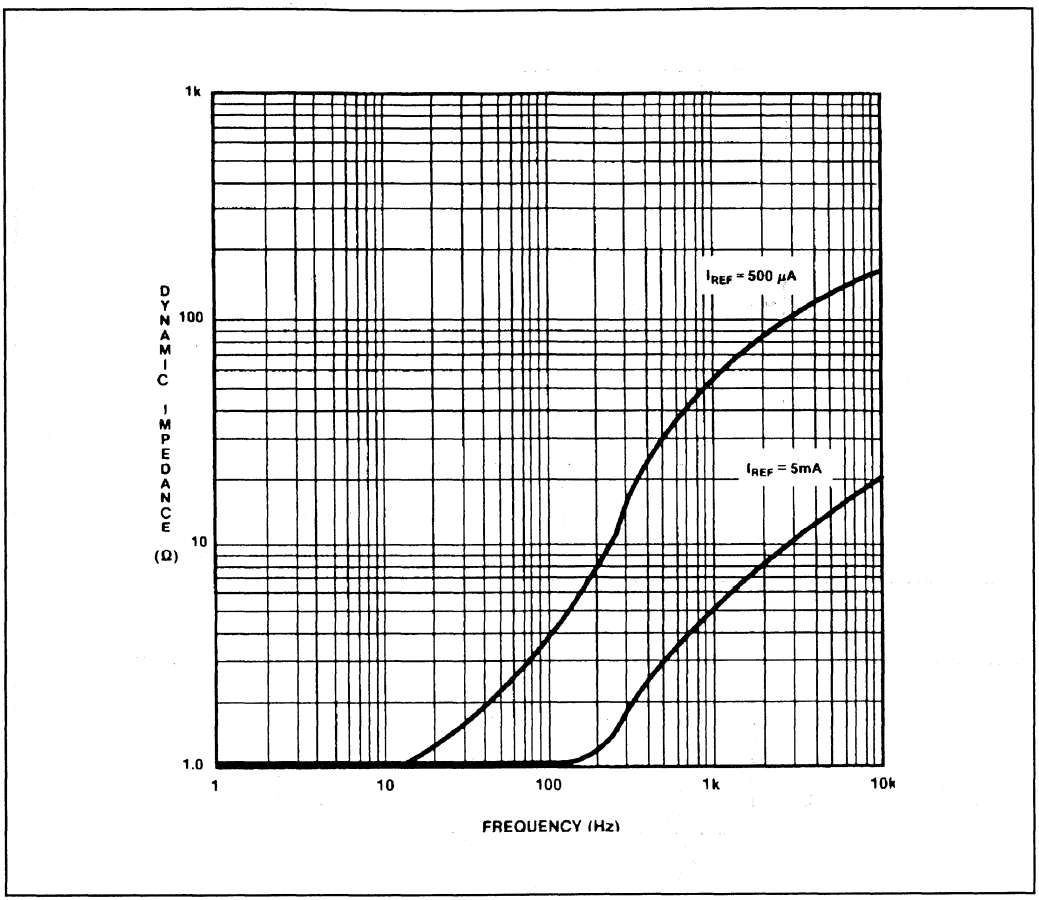


Fig.6 Typical dynamic impedance

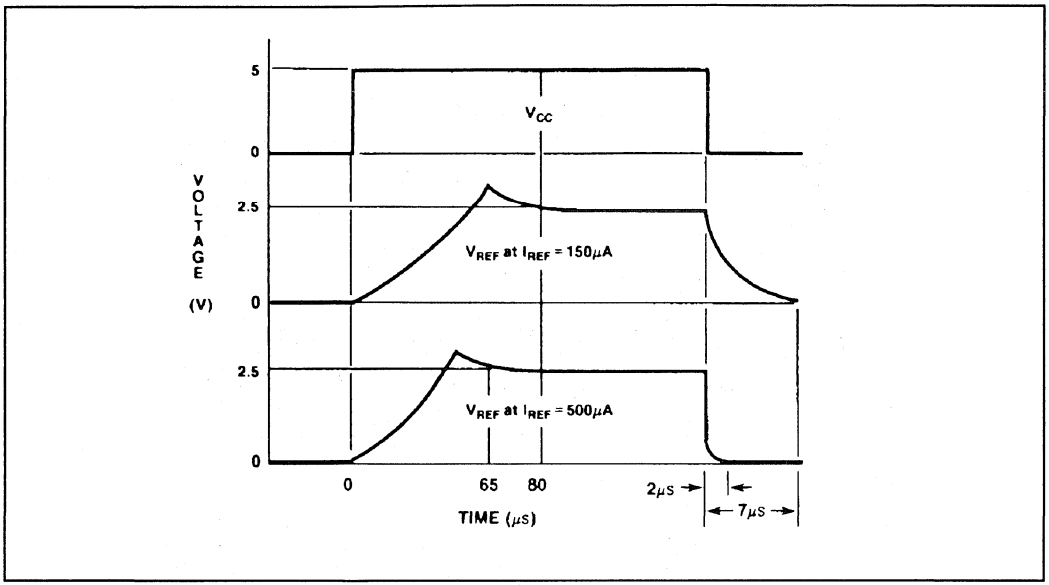


Fig.7 Typical response time

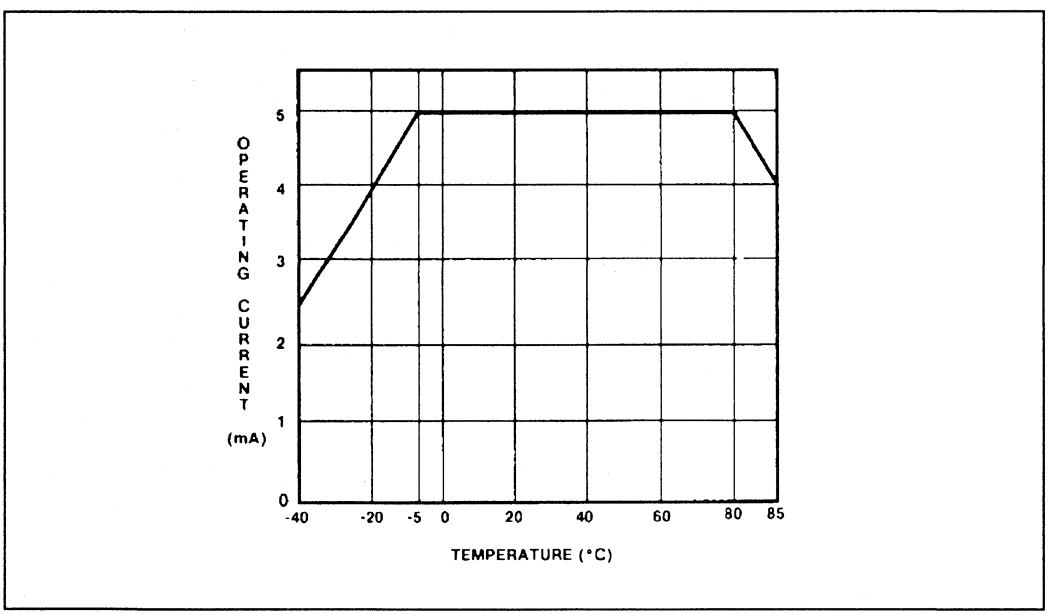


Fig.8 Derating curve REF25Z/25D

REF50Z/REF50D

5V MICROPOWER PRECISION REFERENCE

The REF50Z and REF50D are integrated circuits using the bandgap principle to provide a precise stable reference voltage of 5V. There are two package options available: REF50Z in a plastic 3-pin TO-92 and REF50D in a miniature surface mount package (MP8).

These references feature a recommended operating current of 60µA to 5mA which make them ideal for all low power and battery applications.

FEATURES

- Low Knee Current - typically 40 microamps
- Ideal for Battery Operation - 300 microwatts
- Internally Shaped
- REF50Z - 3 lead TO-92 Plastic Package
- REF50D - Miniature Plastic Surface Mount Package (MP8)
- Tight Initial V_{REF} Tolerance ±1.5%
- Low Temperature Coefficient
- Low Slope Resistance
- Operation over Industrial Temperature Range

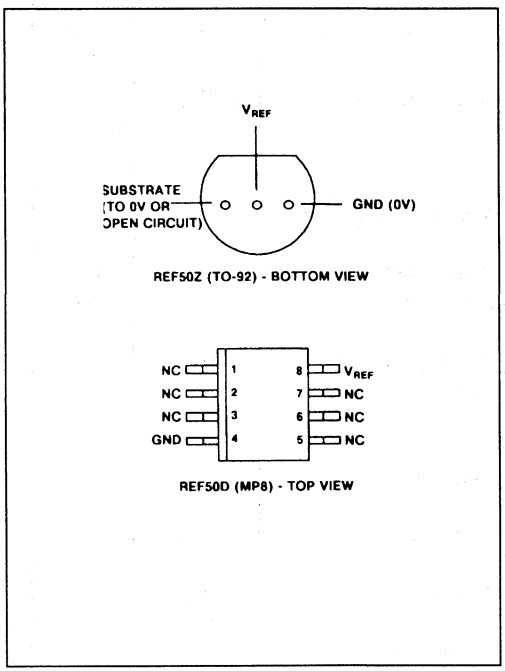


Fig.1 Pin connection

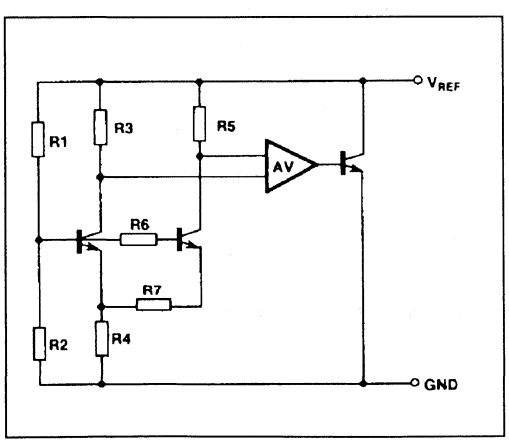


Fig.2 Internal connections

ORDERING INFORMATION

Device Type	Operating Temperature	Package
REF50Z	-40°C to +85°C	TO-92
REF50D	-40°C to +85°C	MP8

ABSOLUTE MAXIMUM RATINGS

Reference current	5mA
Operating temperature range:	
REF50Z	-40 to +85°C
REF50D	-40 to +85°C
Storage temperature	-55 to +125°C
Storage temperature for a max. time of 10ns:	
within 1.59mm of seating plane	300°C
within 0.80mm of seating plane	265°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 25°C, I_{REF} = 150µA

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	4.925	5.00	5.075	V	
Slope resistance (Note 1)	R_{REF}		3.0	3.5	Ω	REF 50Z, I_{REF} = 150µA to 5mA
			3.0	3.5	Ω	REF50D, I_{REF} = 150µA to 5mA
Turn-on (knee) current	I_{ON}		40		µA	
Recommended operating current range	I_{REF}	0.06		5.0	µA	
Temperature coefficient (Note 2)	TC V_{REF}		35	110	ppm/°C	REF25Z, Note 2
			35	80	ppm/°C	REF25D, Note 2
RMS noise voltage	E_N		13		µV	1kHz tp 10kHz
Turn-on time	T_{ON}		80		µs	
Turn-off time	T_{OFF}		7		µs	
Turn-on time	T_{ON}		65		µs	I_{REF} = 500µA
Turn-off time	T_{OFF}		2		µs	I_{REF} = 500µA

NOTES

1. Slope resistance (R_{REF})

   Slope resistance is defined as

   $$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

2. Reference voltage temperature coefficient (TC VREF)

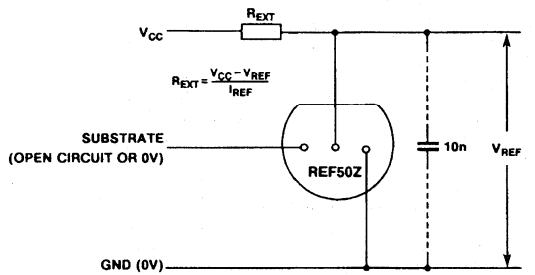
   This is the normalised reference voltage change over temperature, divided by the change in temperature.

   It is expressed in ppm/°C

   $$TC\ V_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

   ΔT = temperature change in °C

   ΔV_{REF} = change in reference voltage over temperature change ΔT



NOTE: In some instances, in order to achieve optimum operation, a 10nF capacitor should be connected between V_{REF} and 0V as shown.

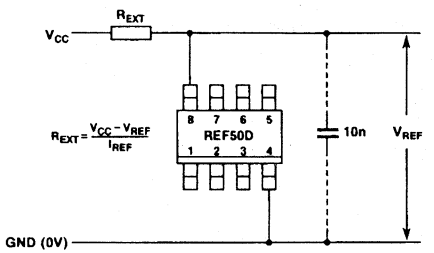


Fig.3 Connections diagram

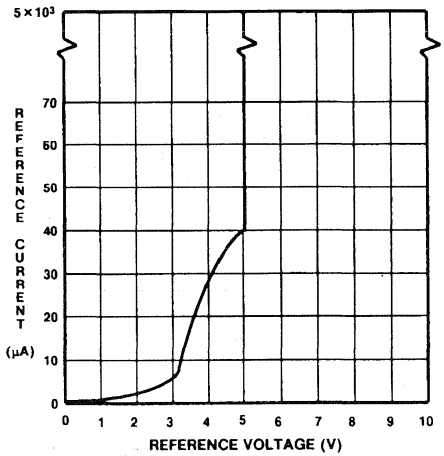


Fig.4 Typical reference characterics

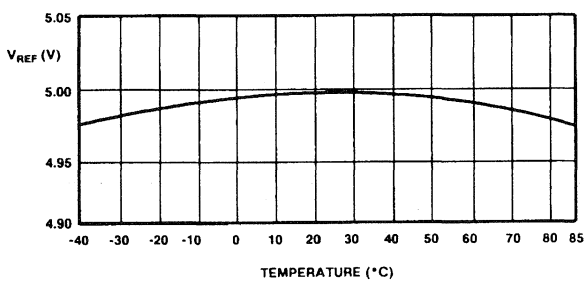


Fig.5 Typical temperature at I_{REF} = 150μA

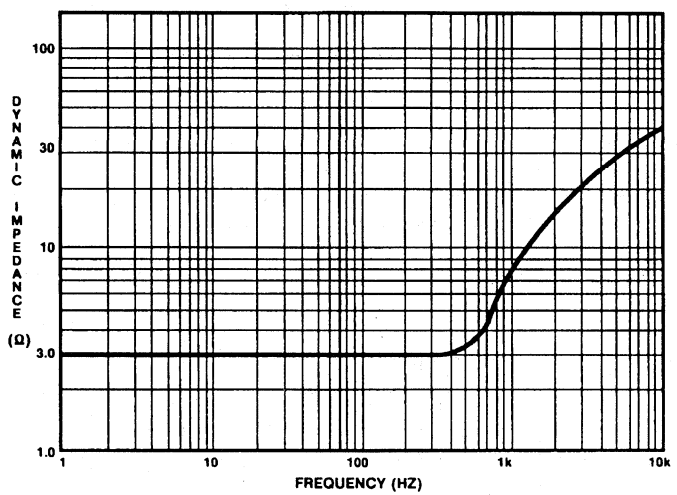


Fig.6 Typical dynamic impedance at I_{REF} = 5mA

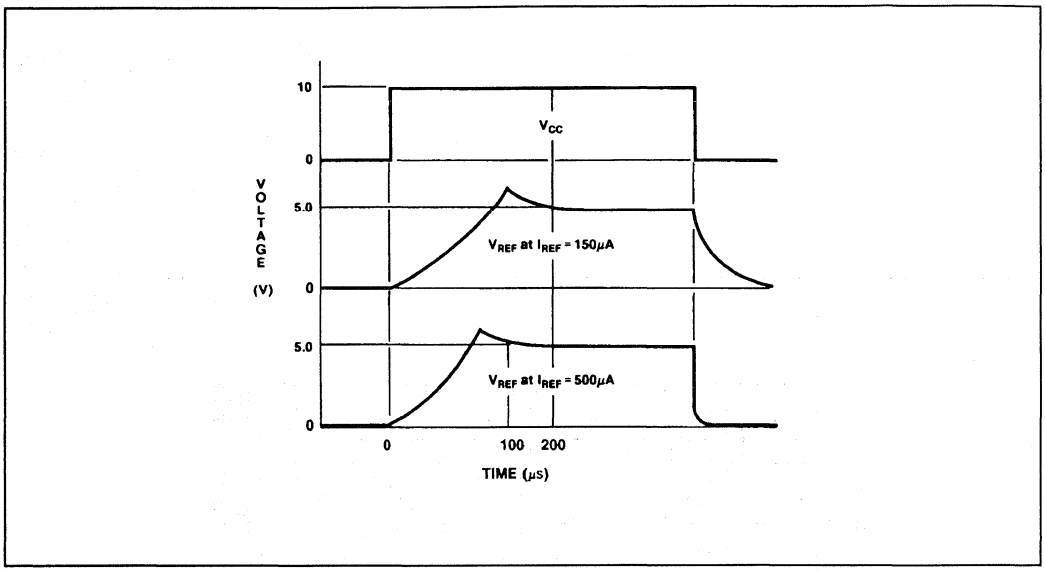


Fig.7 Typical response time (not to scale)

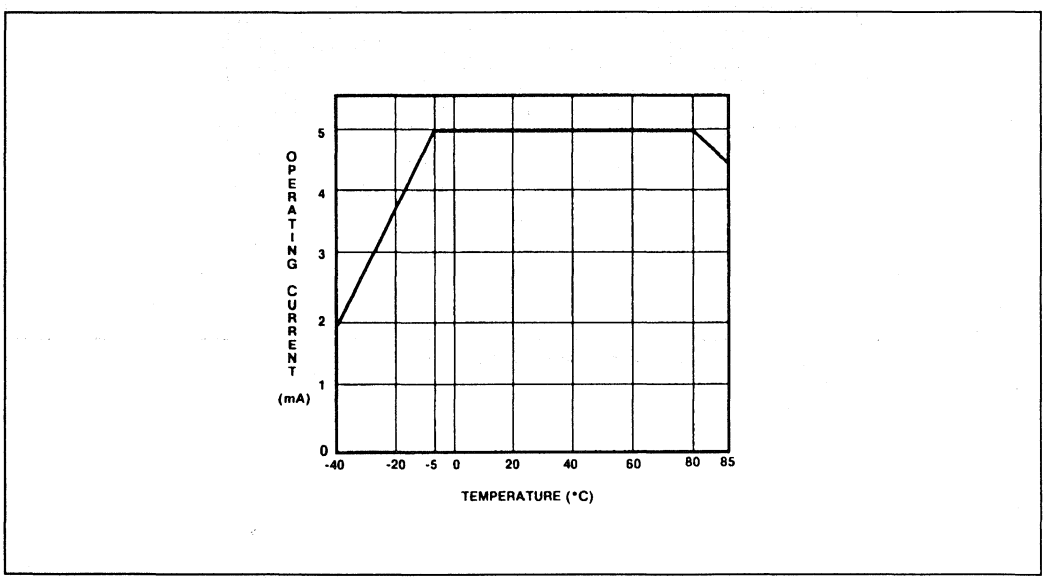


Fig.7 Typical response time (not to scale)

Section 6

Micropower Bandgap Voltage References

GEC PLESSEY
SEMICONDUCTORS

SR12D

1.2V PRECISION VOLTAGE REFERENCE

The SR12D is a monolithic integrated circuit using the bandgap principle to provide a precise reference voltage of 1.23V.

This reference device is packaged in a standard SOT-23 small outline package, making it ideal for all surface mount applications.

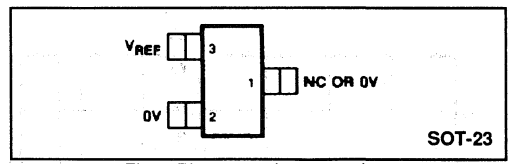


Fig. 1 Pin connections (top view)

FEATURES

- Standard SOT-23 Surface Mount Package
- Low Knee Current - Typically 80 µA
- Low temperature Coefficient

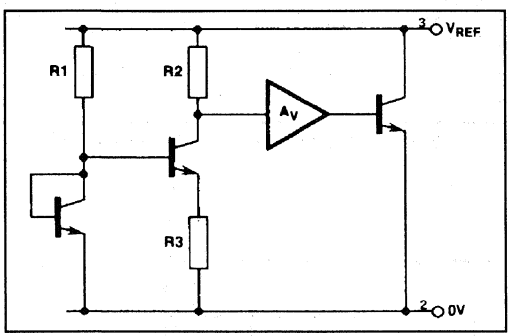


Fig.2 SR12D circuit diagram

ABSOLUTE MAXIMUM RATINGS

Reference current	2.5mA
Operating temperature range	-40°C to + 85°C
Storage temperature range	-55°C to +125°C

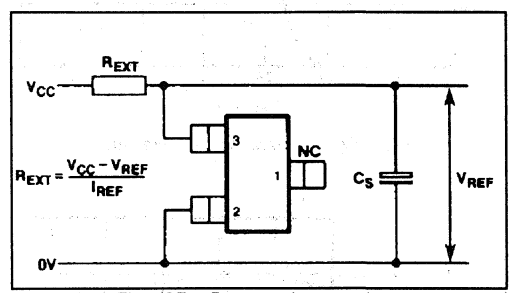


Fig.3 SR12D external connections.

NOTE: In order to achieve optimum operation, an electrolytic stabilising capacitor ($C_S \geq 1\mu F$) should be connected between V_{REF} and 0V as shown in Fig. 3.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{amb} = +25°C, I_{REF} = 150µA, C_S = 1µF

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	1.193	1.230	1.267	V	
Slope resistance (see note 1)	R_{REF}		1.5	2.5	Ω	I_{REF} = 150µA to 2.5mA
Turn-on (knee) current	I_{ON}		80	90	µA	
Recommended operating current range	I_{REF}	0.09		2.5	mA	
Temperature coefficient (see note 2)	TCV_{REF}		40	125	ppm/°C	0°C to +70°C
			40	120	ppm/°C	-40°C to + 85°C
RMS noise voltage	E_N		10		µV	1Hz to 25kHz
Turn on time	t_{ON}		7		ms	
Turn off time	t_{OFF}		24		ms	
Turn on time	t_{ON}		0.4		ms	I_{REF} = 5mA
Turn off time	t_{OFF}		1.8		ms	I_{REF} = 5mA

NOTES

1. Slope Resistance (R_{REF})

The slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over specified current range}}{\text{The change in reference current}}$$

2. Reference Voltage Temperature Coefficient (TCV_{REF})

This is the normalised reference voltage change over temperature , divided by the change in temperature. It is expressed in ppm/°C as follows:

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

ΔT = temperature change in °C

ΔV_{REF} = change in reference voltage over temperature change ΔT.

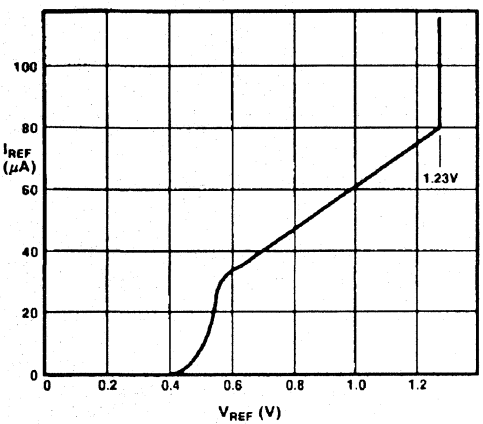


Fig.4 Typical reference characteristic

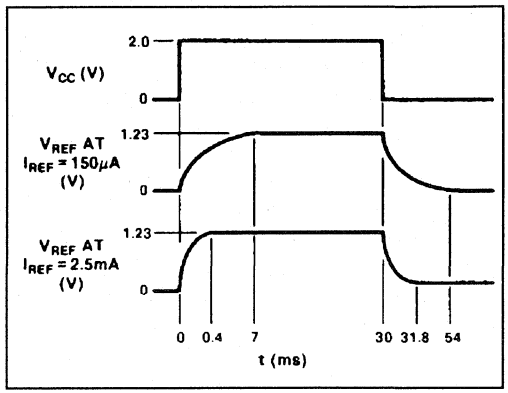


Fig.5 SR12D typical response time (not to scale)

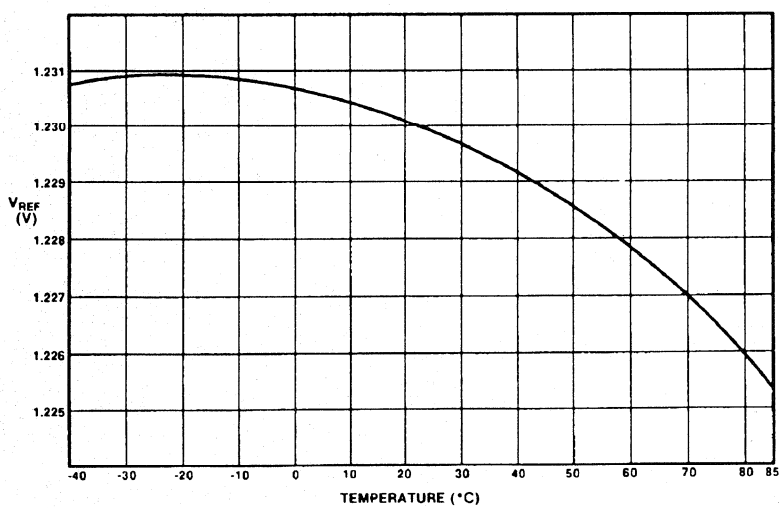


Fig.6 Typical temperature characteristic of SR12D at I_{REF} = 150μA

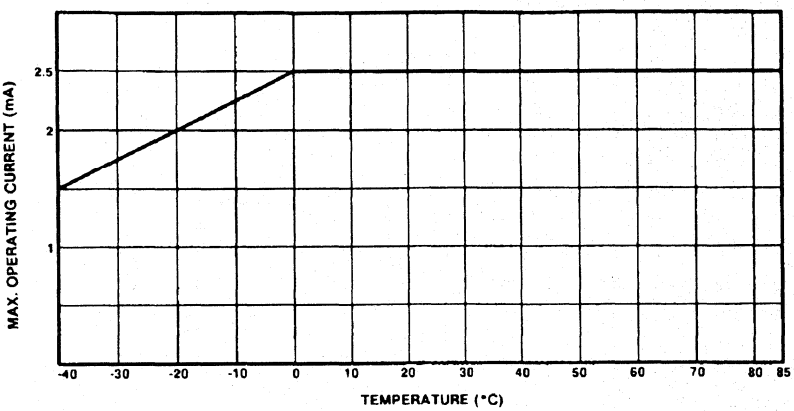


Fig.7 Derating curve

SR25D

2.5V PRECISION VOLTAGE REFERENCE

The SR25D is a monolithic integrated circuit using the bandgap principle to provide a precise reference voltage of 2.5V.

This reference device is packaged in a standard SOT-23 small outline package, making it ideal for all surface mount applications.

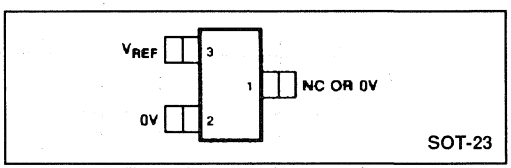


Fig. 1 Pin connections (top view)

FEATURES

- Standard SOT-23 Surface Mount Package
- Low Knee Current - Typically 60 µA
- Low temperature Coefficient

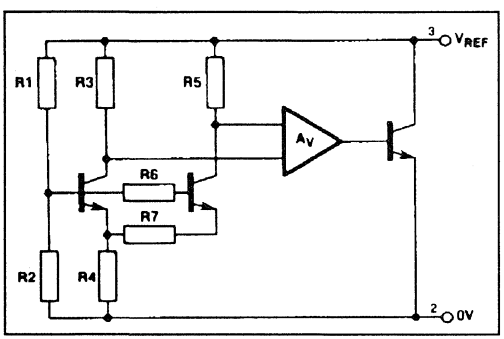


Fig.2 SR25D circuit diagram

ABSOLUTE MAXIMUM RATINGS

Reference current	5mA
Operating temperature range	-40°C to + 85°C
Storage temperature range	-55°C to +125°C

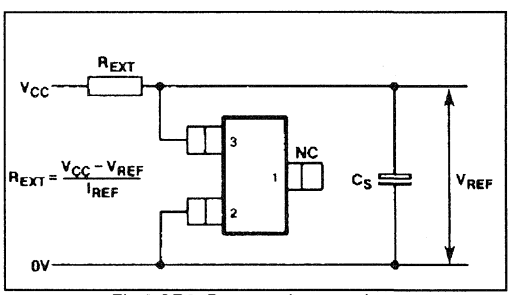


Fig.3 SR25D external connections.

NOTE: In order to achieve optimum operation, an electrolytic stabilising capacitor, C_S, (see Fig. 9) should be connected between V_{REF} and 0V as shown in Fig. 3.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

T_{amb} = +25°C, I_{REF} = 150µA, C_S = 1µF

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Output voltage	V_{REF}	2.425	2.50	2.575	V		
Slope resistance	R_{REF}		1.2	2.0	Ω	I_{REF} = 150µA to 5mA	1
Turn-on (knee) current	I_{ON}		60	80	µA		3
Recommended operating current range	I_{REF}	0.08		5	mA		3
Temperature coefficient	TCV_{REF}		40	150	ppm/°C	-40°C to + 85°C	2&3
RMS noise voltage	E_N		18		µV		3
Turn on time	t_{ON}		12.5		ms		3
Turn off time	t_{OFF}		45		ms		3
Turn on time	t_{ON}		0.4		ms	I_{REF} = 5mA	3
Turn off time	t_{OFF}		1.5		ms		3

NOTES

1. Slope Resistance (R_{REF})

The slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over specified current range}}{\text{The change in reference current}}$$

2. Reference Voltage Temperature Coefficient (TCV_{REF})

This is the normalised reference voltage change over temperature , divided by the change in temperature. It is expressed in ppm/°C as follows:

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

ΔT = temperature change in °C

ΔV_{REF} = change in reference voltage over temperature change ΔT.

3. Guaranteed but not tested

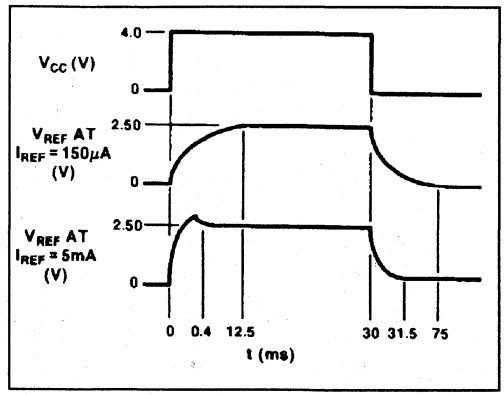


Fig.5 SR25D typical response time (not to scale)

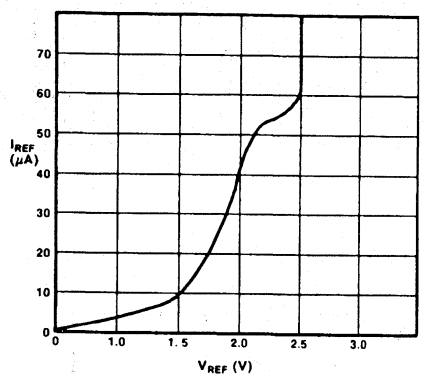


Fig.4 Typical reference characteristic

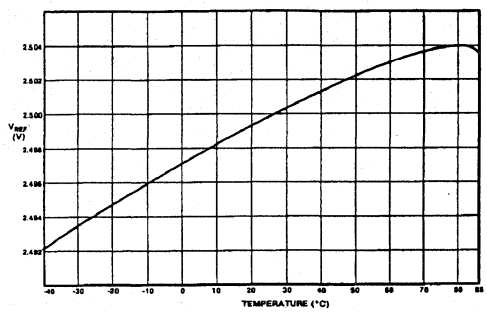


Fig.6 Typical temperature characteristic of SR25D at I_{REF} = 150μA

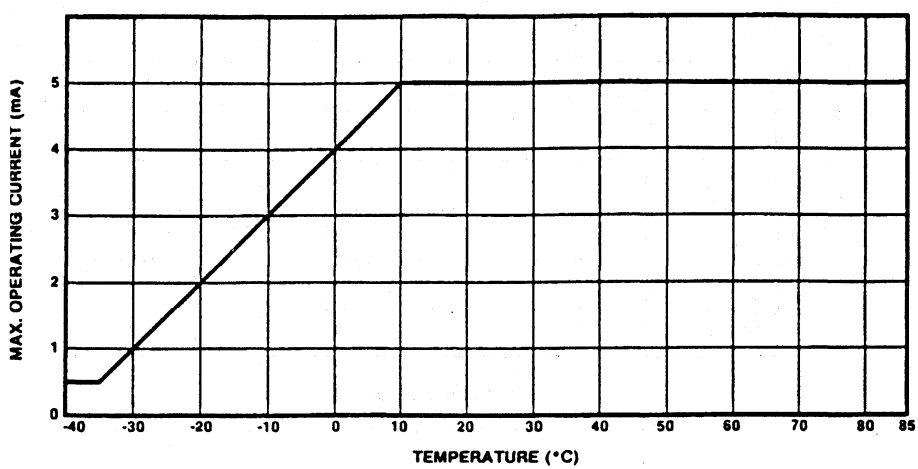


Fig.7 Derating curve

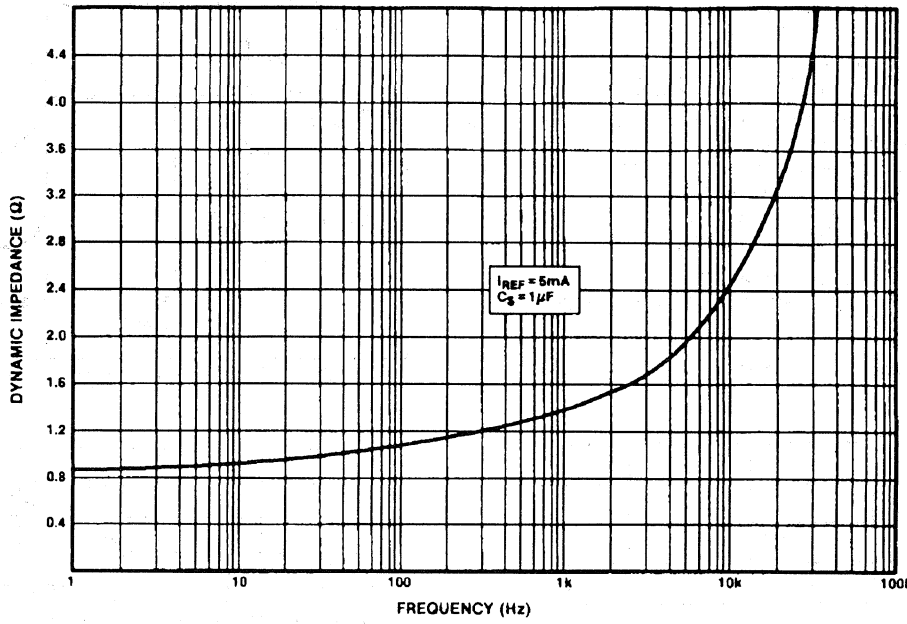


Fig.8 Typical dynamic impedance of SR25D

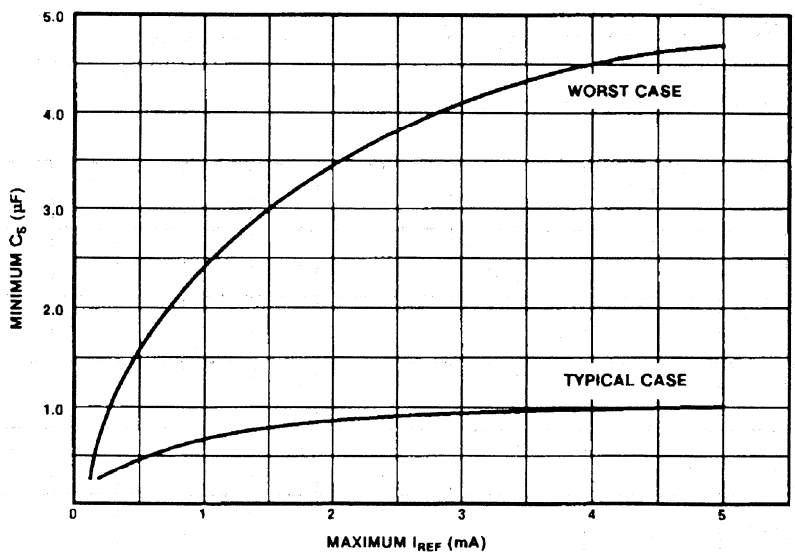


Fig.9 Stabilising capacitor required for optimum operation

VR25

2.5V PRECISION MICROPOWER BANDGAP VOLTAGE REFERENCE

The VR25 is a monolithic integrated circuit using the bandgap principle to provide a precise reference voltage of 2.5V.

The VR25 does not require any external capacitance for stability.

This reference device is supplied in the standard SOT–23 small outline package, making it ideal for all surface mount applications.

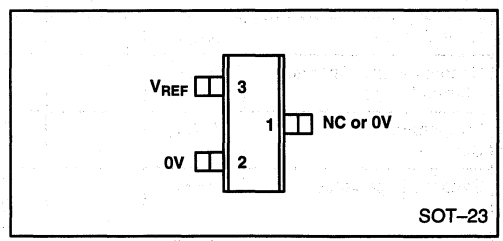


Fig. 1 Pin Connections – top view

FEATURES

- Standard SOT–23 package
- Tight initial V_{REF} tolerance of ± 1%
- Wide operating current range up to 10mA
- Low temperature coefficient
- Low slope resistance
- No external capacitor required for stability
- Tolerates capacitive loading
- Operation over the industrial temperature range

APPLICATIONS

- Instrumentation
- Data acquisition
- Automotive systems

ABSOLUTE MAXIMUM RATINGS

Reference Current	10mA
Power dissipation (T_{amb} = 25°C)	25mW
Operating temperature range	–40°C to +85°C
Storage temperature range	–55°C to +150°C

ORDERING INFORMATION

VR25/IG/MPCY – Industrial (loose SOT–23)
VR25/IG/MPCA – Industrial (tape and reel SOT–23)

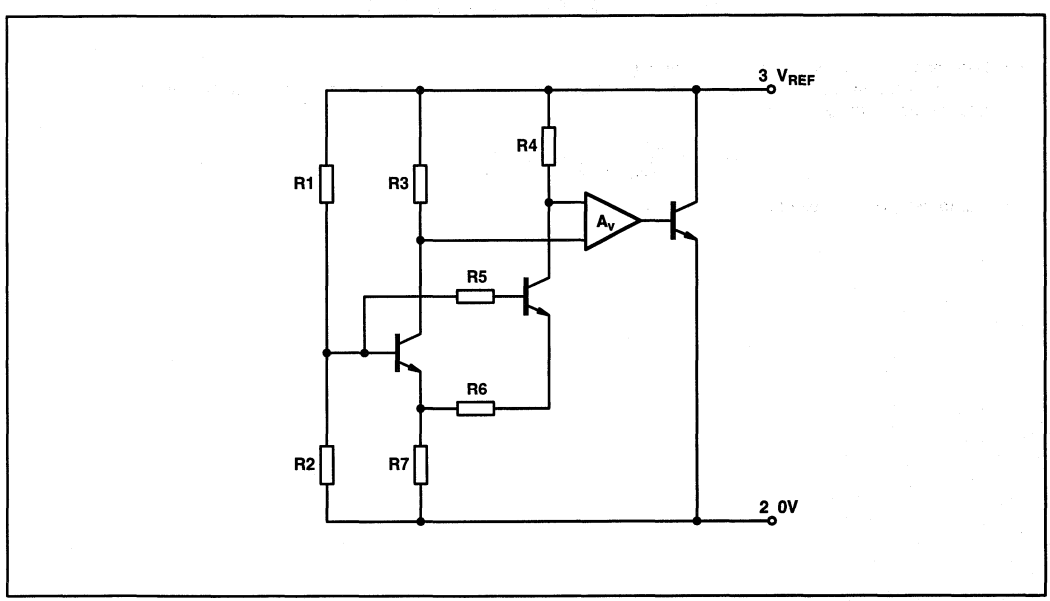


Fig.2 Functional block diagram

VR25

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated) : T_{amb} = 25°C, I_{ref} = 150µA

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Output Voltage	V_{REF}	2.4750	2.5000	2.5250	V	
Slope Resistance	R_{REF}	–0.1 –0.3	0.2 0	0.5 0.3	Ω Ω	I_{ref} = 150µA to 5mA (see note 1) I_{ref} = 150µA to 10mA (see note 1)
Knee Current	I_{KNEE}		65	80	µA	(see note 3)
Recommended Operating Current Range	I_{REF}	0.08		10	mA	(see note 3)
Temperature Coefficient	TCV_{REF}		75	150	ppm/°C	–40 to 85°C (see note 2&3)
Dynamic Impedance	Z_{REF}		10 0.4 0.1		Ω Ω Ω	I_{REF} = 150µA (see note 3) I_{REF} = 5mA (see note3) I_{REF} = 10mA (see note 3) $I_{AC} = 0.1I_{REF}$ f = 100Hz
RMS Noise Voltage	E_N		65		μV_{RMS}	10Hz ≤ f ≤ 10kHz (see note 3)
Turn–on Time	t_{ON}		20 15 15		µs µs µs	I_{REF} = 150µA (see note 3) I_{REF} = 5mA (see note 3) I_{REF} = 10mA (see note 3)
Turn–Off Time	t_{OFF}		25 3 5		µs µs µs	I_{REF} = 150µA (see note 3) I_{REF} = 5mA (see note 3) I_{REF} = 10mA (see note 3)

NOTES

1. Slope resistance (R_{REF})
   The slope resistance is defined as:

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over specified current range}}{\text{The change in reference current}}$$

2. Reference voltage temperature coefficient (TCV_{REF})
   This is the normalised reference voltage change over temperature , divided by the change in temperature.
   It is expressed in ppm/°C as follows:

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

3. Guaranteed but not tested.

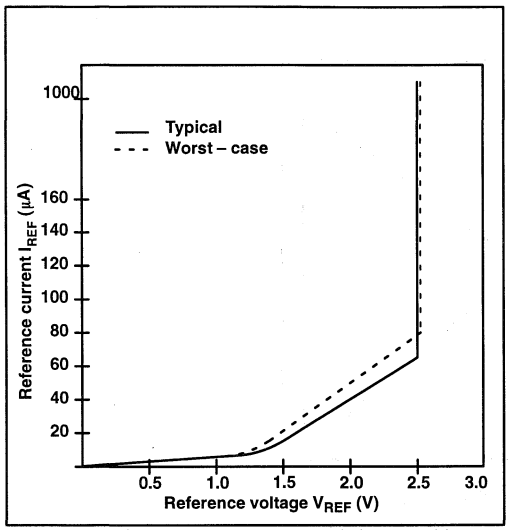


Fig. 3 Reference turn–on characteristics at ambient temperature of 25°C

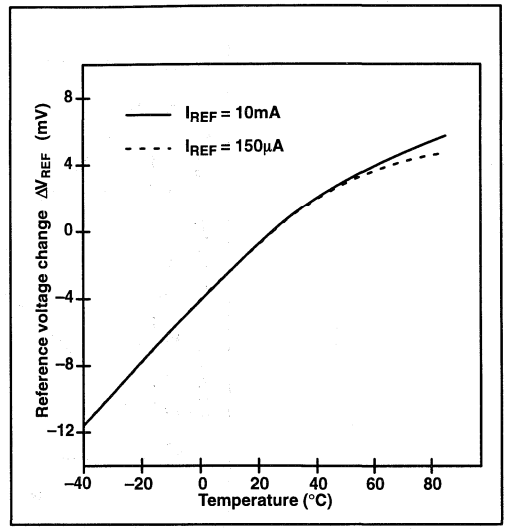


Fig. 5 Typical temperature characteristics

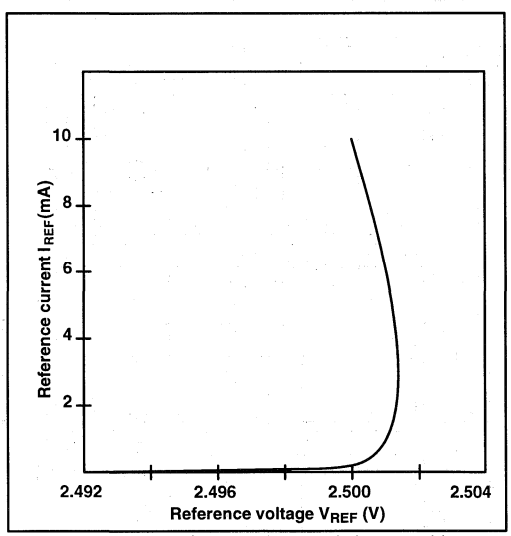


Fig. 4 Typical reference characteristics at ambient temperature of 25°C

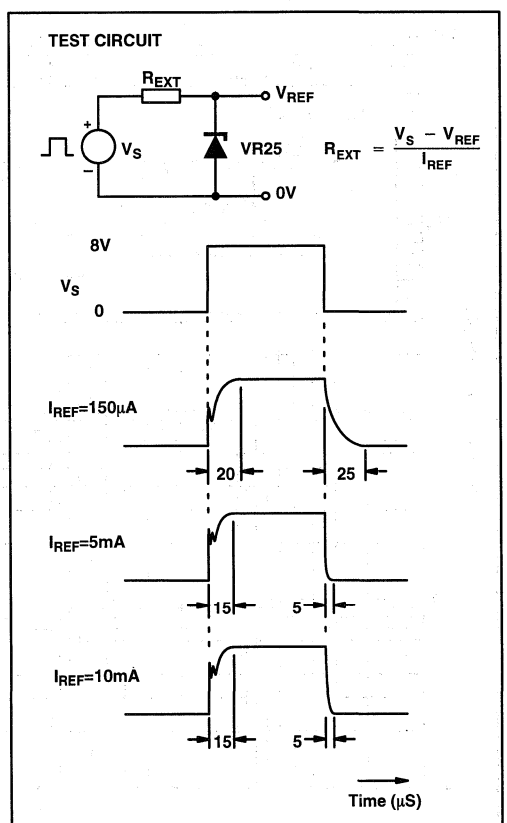


Fig. 6 Typical response times (not to scale)

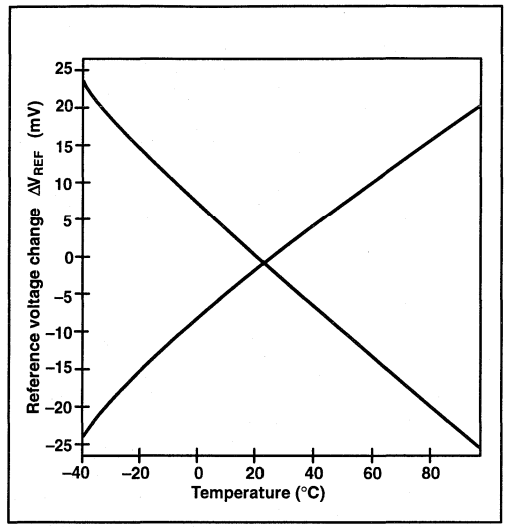


Fig. 7 Worst–case temperature characteristic at I_{REF}=150μA

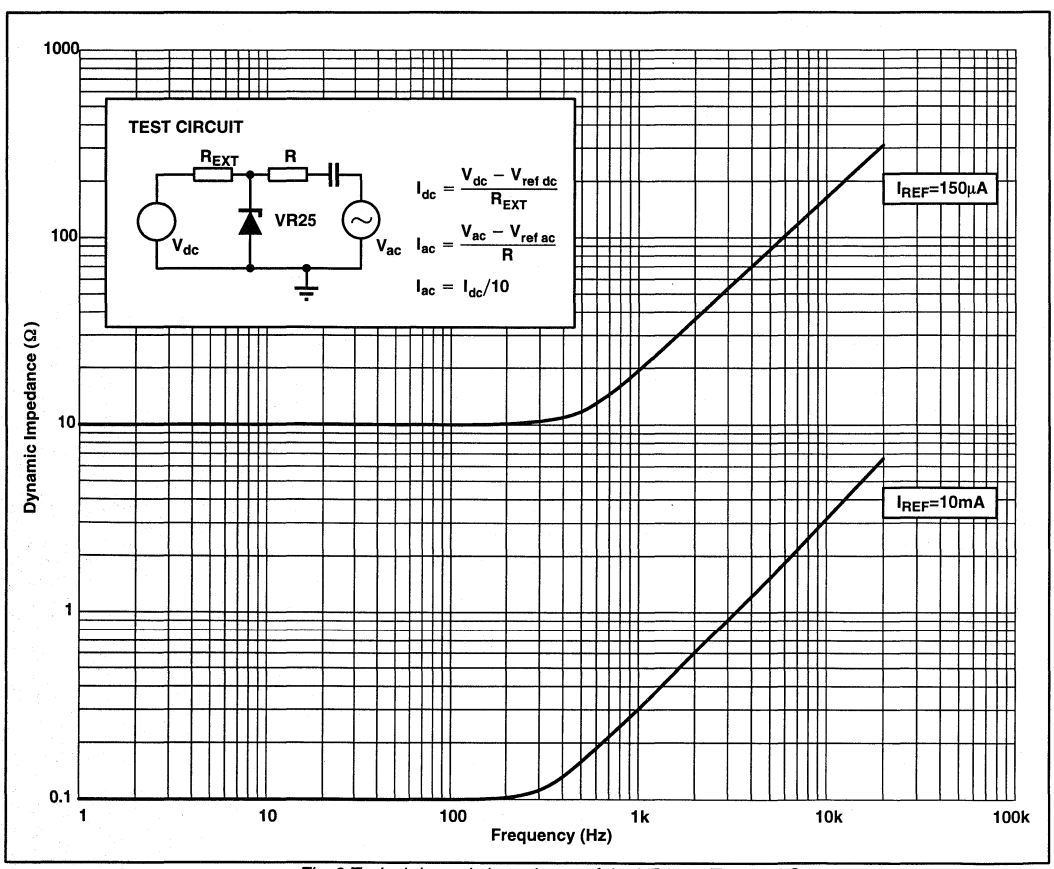


Fig. 8 Typical dynamic impedance of the VR25 at T_{amb}=25°C

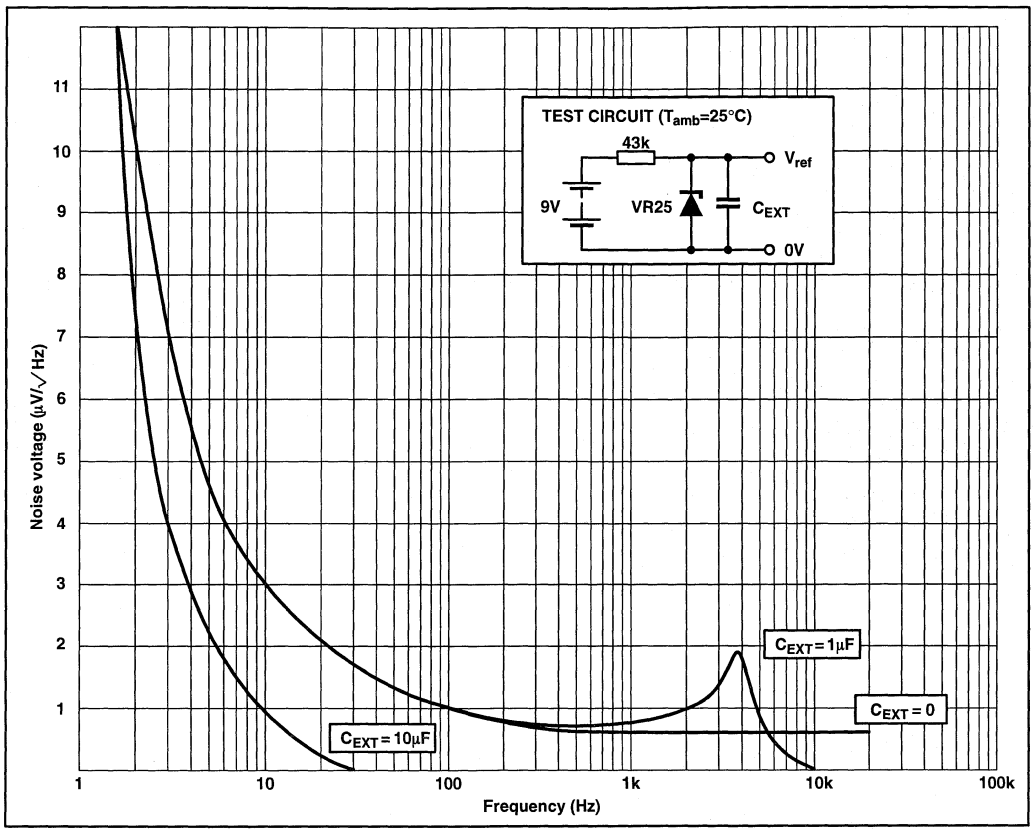


Fig. 9 Noise voltage of VR25

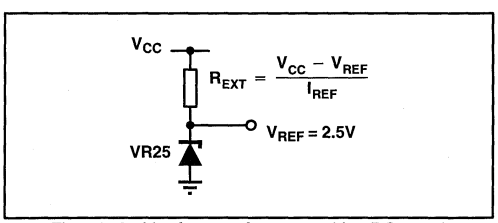


Fig. 10 2.5V reference from a positive DC supply

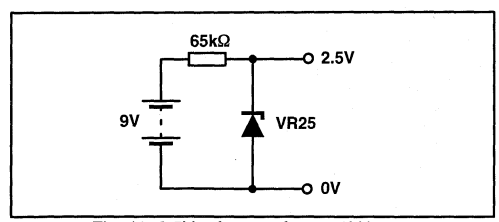


Fig. 11 2.5V reference from a 9V battery (power dissipation = 250μW)

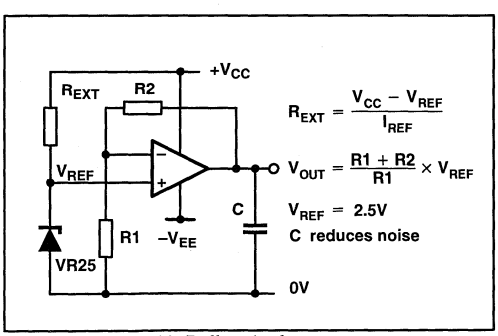


Fig. 12 Buffered reference source

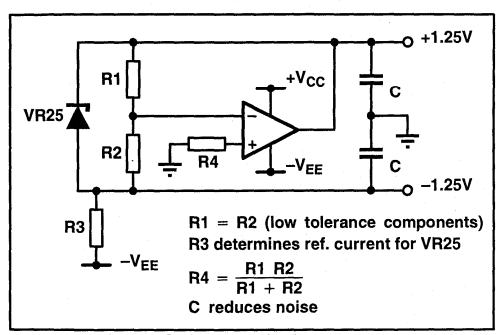


Fig. 13 Split ± 1.25V reference source

Section 7

Fixed Voltage References

ZN404 / ZN404D

2.45V PRECISION REFERENCE REGULATOR

The ZN404 is a monolithic integrated circuit providing a precise stable reference source of 2.45V without the need for an external shaping capacitor.

FEATURES

- Low Temperature Coefficient
- Low Slope Resistance
- Very Good Long Term Stability
- Low Noise
- Internally Shaped
- Tight Tolerance
- ZN404 - 2-Lead TO-18 Metal Can Package
- ZN404D - 8-Lead Miniature Plastic Surface Mount Package

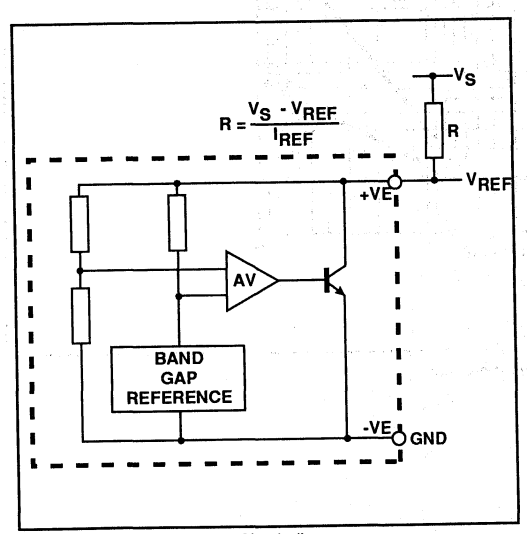


Fig.2 Circuit diagram

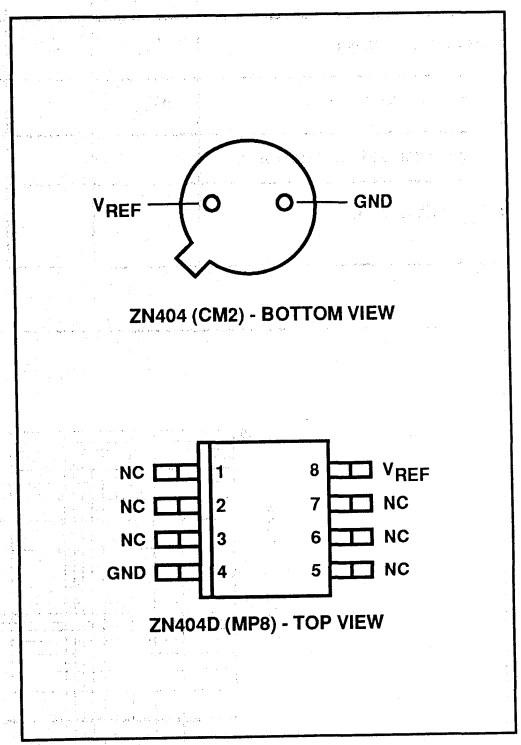


Fig.1 Pin connections

ORDERING INFORMATION

Device	Operating Temperature	Package
ZN404	-20°C to +70°C	CM2
ZN404D	-20°C to +70°C	MP8

ABSOLUTE MAXIMUM RATINGS

Dissipation	300mW
Operating temperature range	
ZN404	-20°C to +70°C
ZN404D	-20°C to +70°C
Storage temperature range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
Output voltage	V_{REF}	2.38	2.45	2.52	V	Measured at 2mA
Slope resistance	R_{REF}	-	0.1	0.2	Ω	
Reference current	I_{REF}	2.0	-	120	mA	
Maximum change in V_{REF}	ΔV_{REF}	-	6	33	mV	-20 to +70°C
RMS noise voltage 1Hz-10kHz			10	-	μV	1kHz - 10kHz
V_{REF} drift at 70°C			±10	-	ppm/1000 hours	CM2 Package

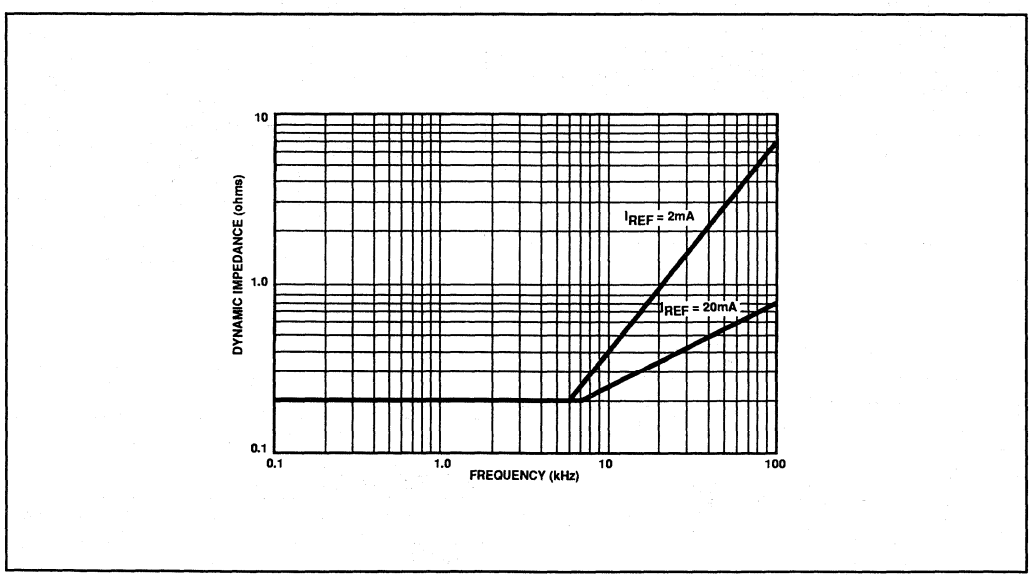


Fig.3 Dynamic impedance

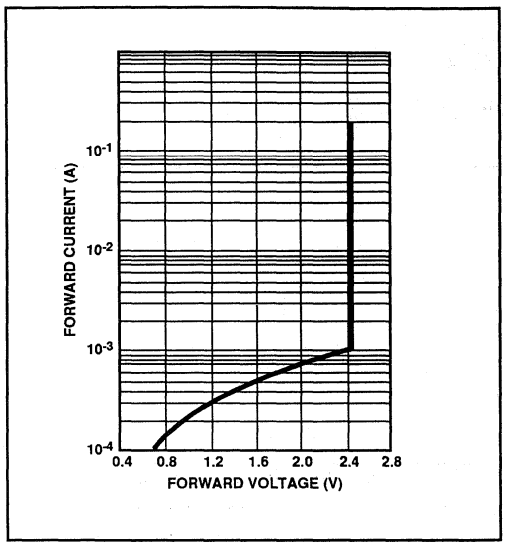


Fig.4 Forward characteristic (typical)

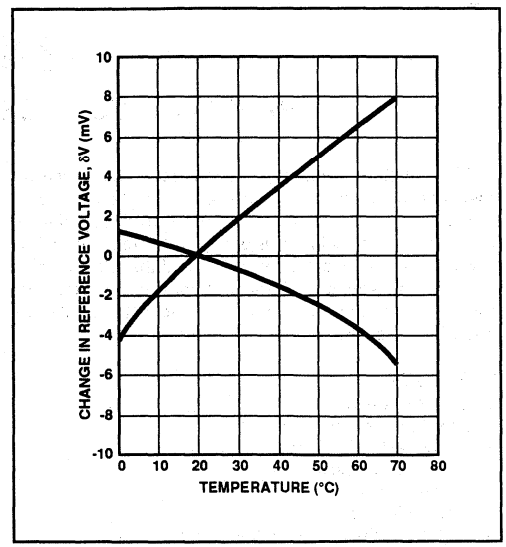


Fig.5 Temperature characteristic (typical)

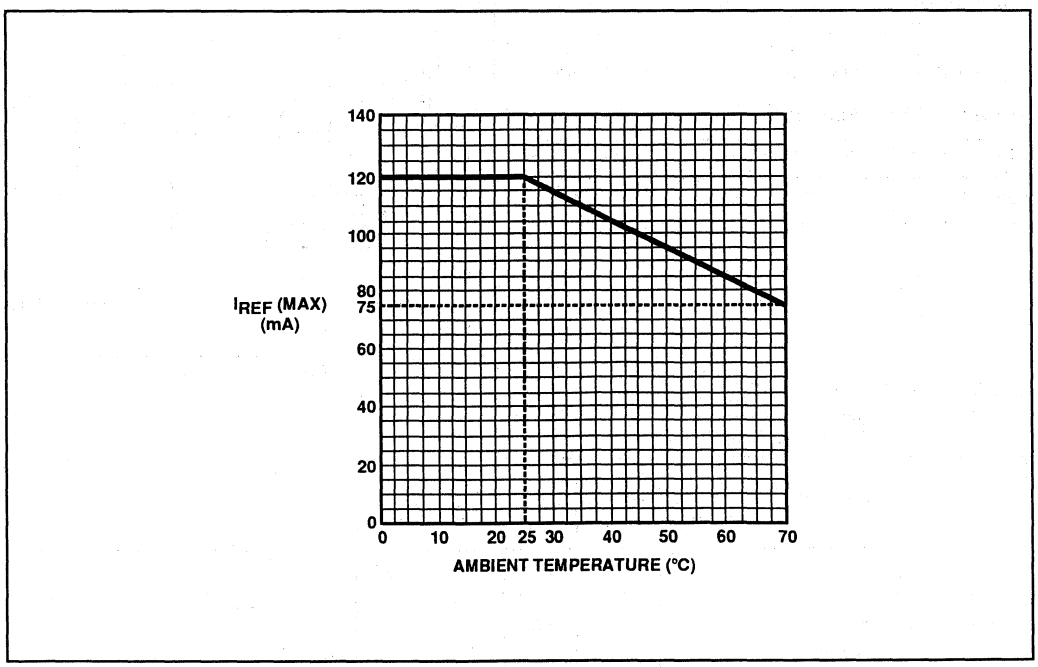


Fig.6 Derating curve

ZN423

PRECISION VOLTAGE REFERENCE SOURCE

The ZN423 is a monolithic integrated circuit using the energy bandgap voltage of a base-emitter junction to produce a precise, stable, reference source of 1.26V. This is derived via an external dropping resistor for supply voltages of 1.5V upwards. The temperature coefficient of the ZN423, unlike conventional Zener diodes, remains constant with reference current. the noise figure associated with breakdown mechanisms is also considerably reduced.

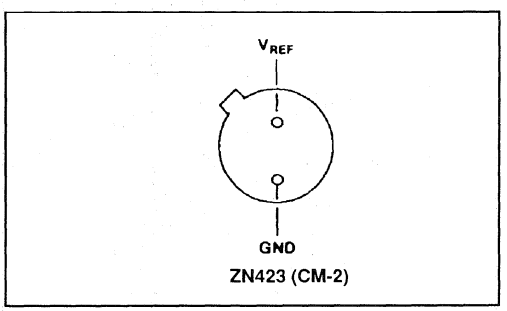


Fig.1 Pin connections (bottom view)

FEATURES

- Low Voltage
- Low Temperature Coefficient
- Very Good Long Term Stability
- Low Slope Resistance
- Low RMS Noise
- Tight Tolerance
- High Power Supply Rejection Ratio
- 2-Lead TO-18 Metal Can Package

ABSOLUTE MAXIMUM RATINGS

Reference current, I_{REF}	20mA
Operating temperature range:	-55°C to +125°C
Storage temperature range:	-65°C to +165°C

ORDERING INFORMATION

Device Type	Operating Temperature	Package
ZN423	-55°C to +125°C	CM2

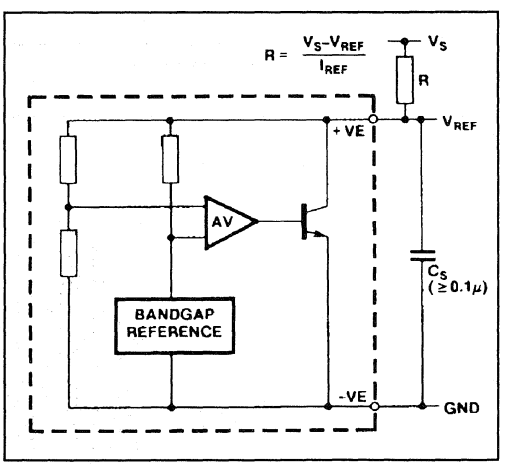


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C, Shaping capacitor, C_S = 0.1μF

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output voltage	V_{REF}	1.2	1.26	1.32	V	
Slope resistance	R_{REF}		0.5	1.5	Ω	I_{REF} = 5mA
Reference current	I_{REF}	1.5		12	mA	
Temperature coefficient			30		ppm/°C	
External resistor	R_{EXT}	100			Ω	$R_{EXT} = (V_{CC}-V_{REF})/I_{REF}$
RMS noise voltage			6		μV	1Hz to 10kHz
Power supply ratio	P_{SRR}		60		dB	$P_{SRR} = R_{EXT}/R_{REF}$, V_{REF} = 1.26V, I_{REF} = 2.5mA, V_{CC} = 5.0V

Reference current I_{REF} (max.) v operating temperature.

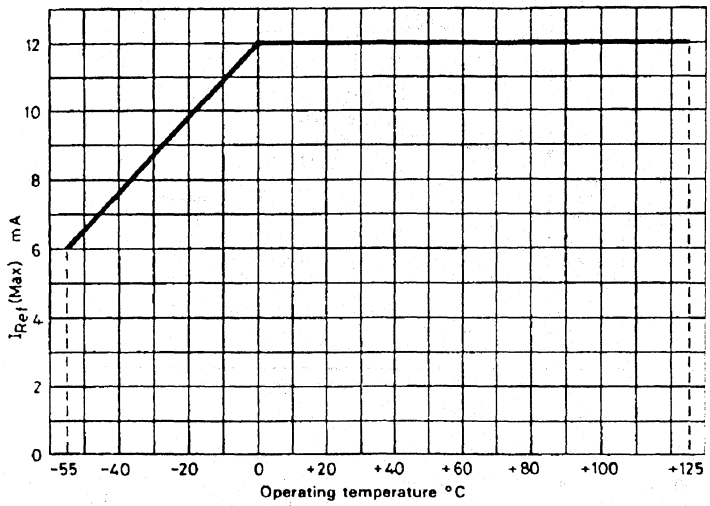


Fig.3 Derating curve

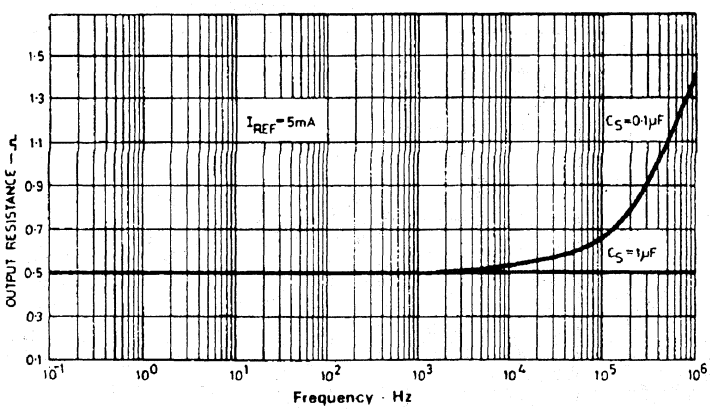


Fig.4 Slope resistance v frequency (I_{REF} = 5mA)

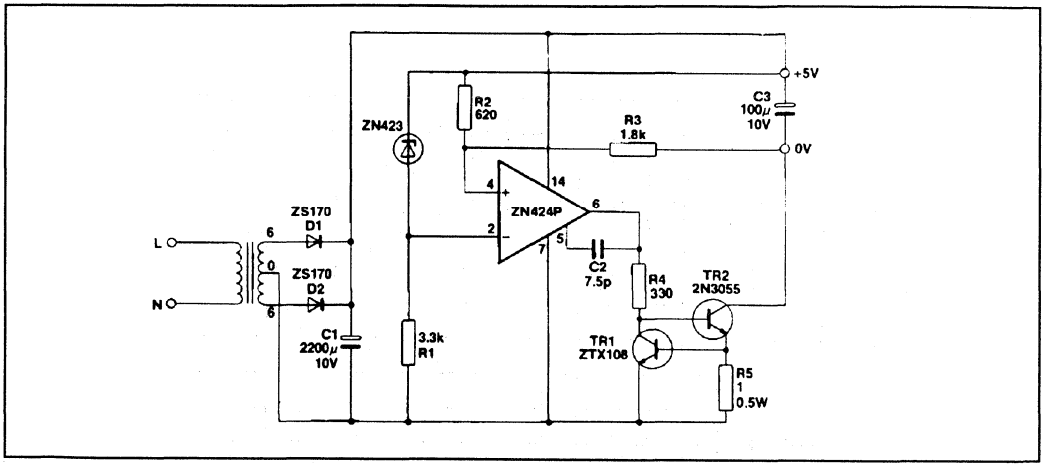


Fig.5 5V, 0.5A power supply

APPLICATIONS

5V, 0.5A Power Supply

The circuit shown in Fig.5 is essentially a constant current source modified by the feedback components R2 and R3 to give a constant voltage output.

The output of the ZN424P need only be 2V above the negative rail, by placing the load in the collector of the output transistor TR2. Current control is achieved by TR1 and R5. The simple circuit has the following performance characteristics:

Output noise and ripple (full load) = 1mV rms
Load regulation (0 to 0.5A) = 0.1%
Temperature coefficient = ±100ppm/°C
Current limit = 0.65A

5V, 1.0A Power Supply

The circuit detailed in Fig.6 provides improved performance over that in Fig.5. This is achieved by feeding the ZN423 reference and the ZN424P error amplifier from a more stable source, derived from the emitter-follower stage (TR1). The supply rejection ratio is improved by the factor R1/R5, where R5 is the slope resistance of the ZN423.

The output voltage is given by:

$$\frac{(R3 + R4)}{R3} \quad V_{REF}$$

and may be adjusted by replacing R3 with a 220 and a 500Ω preset potentiometer.

The output is protected against short circuits by TR2 setting a current limit of 1.6A.

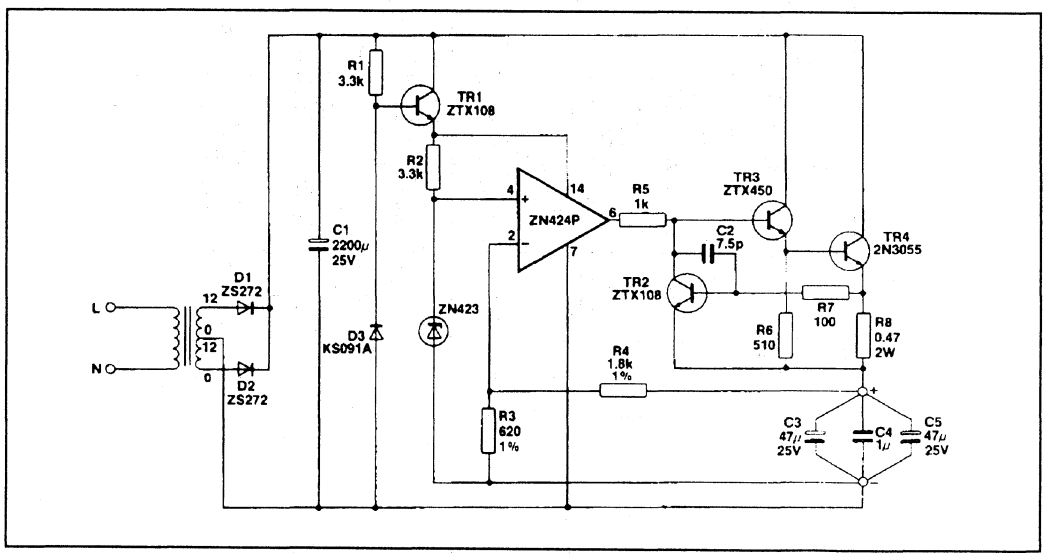


Fig.6 5V. 1.0A power supply

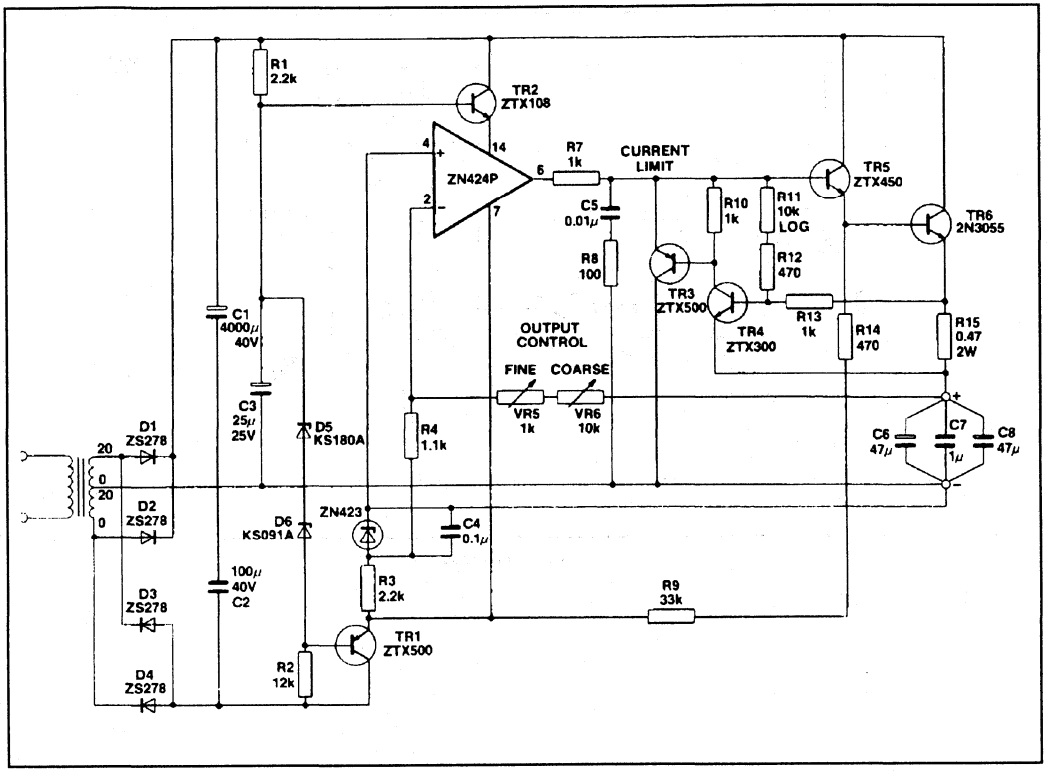


Fig.7 0V to 12V, 1A power supply

0V to 12V, 1A Power Supply

The circuit of Fig.7 provides a continuously variable, highly stable voltage for load currents up to 1A. The output voltage is given by:

$$V_o = \frac{(VR5 + VR6)}{R4} V_{REF}$$

and is controlled by VR5 and VR6 which should be high quality components (preferably wire wound).

The emitter follower stages TR1 and TR2 buffer the bias and reference from the output stages. The negative rail allows the output to operate down to 0V.

The current limit stage monitors output current through R15. As the potential across R15 increases due to load current, TR4 conducts and supplies base current for TR3, thus diverting part of the output from the ZN424P via TR3 to TR5.

Shaping is achieved by the network C5, R8 together with the output decoupling capacitors which also maintain low output resistance at frequencies above 100kHz.

The power supply has the following performace characteristics:

Output noise and ripple (full load) <100μV rms
Output resistance (0 to 1A) 1MΩ
Temperature coefficient ± 100ppm/°C

Variable 100mA to 2A Current Source

In the circuit of Fig.8 the output current is set by the resistor R in the collector of TR2, which may be switched to offer a range of output currents from 100mA to 2A with fine control by means of VR3 which varies the reference voltage to the non-inverting input of the ZN424P.

The feedback path from the output to the inverting input of the ZN424P maintains a constant voltage across R, equal to $(V_{CC} - V_{IN})$ and hence a constant current to the load given by $(V_{CC} - V_{IN})/R$.

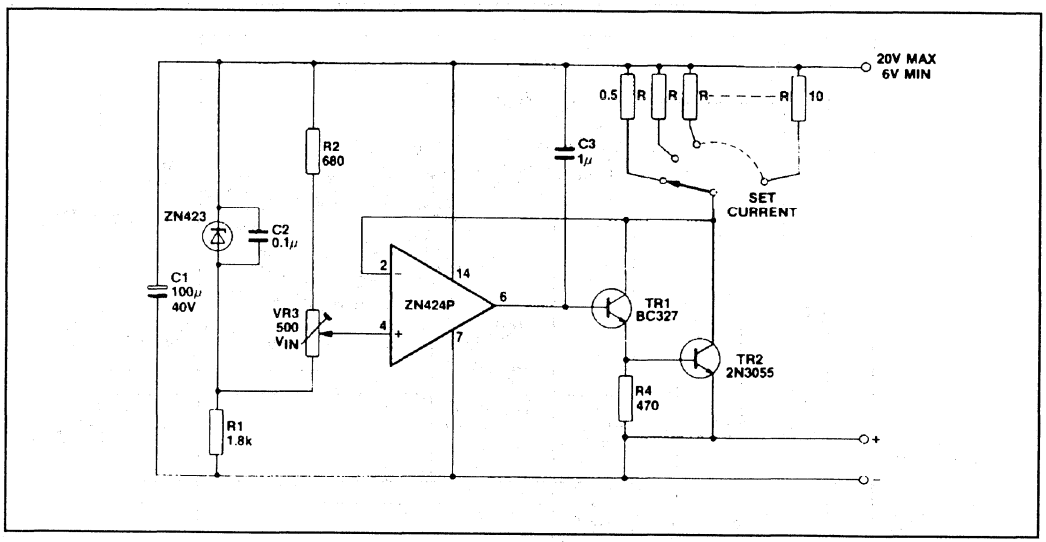


Fig.8 Variable current sources

ZN458

2.45V PRECISION REFERENCE REGULATOR

The ZN458 is a monolithic integrated circuit providing a precise stable reference source of 2.45V in a two lead package without the need for an external shaping capacitor.

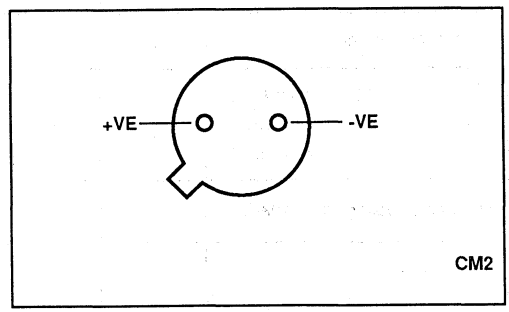


Fig.1 Pin connection - bottom view

FEATURES

- Guaranteed 5mV Maximum Deviation over Full Temperature Range
- Low Temperature Coefficient 0.003%/°C
- Low Slope Resistance - 0.1 Ohms
- Very Good Long Term Stability - 10ppm
- Low Noise - 10 microvolts
- Internally Shaped
- Tight Tolerance ±1.43%
- Two Pin Package
- Wide Operating Current 2-120mA

ABSOLUTE MAXIMUM RATINGS

Dissipation	300mW
Operating temperature range	-20°C to +70°C
Storage temperature range	-55°C to +150°C

ORDERING INFORMATION

Device	TC (ppm/°C)	Temperature range
ZN458	99	-20°C to +70°C
ZN458A	49	-20°C to +70°C
ZN458B	29	-20°C to +70°C

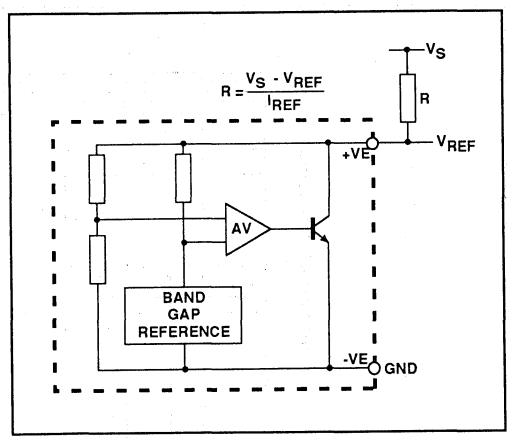


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test conditions
Output voltage	V_{REF}	2.42	2.45	2.49	V	Measured at 2mA
Slope resistance	R_{REF}	-	0.1	0.2	Ω	
Reference current	I_{REF}	2.0	-	120	mA	
Maximum change in V_{REF} ZN458	ΔV_{REF}	-	10	22	mV	-20 to +70°C
ZN458A		-	6	11	mV	
ZN458B		-	4	6.5		
RMS noise voltage 1Hz-10kHz		-	10	-	μV	
V_{REF} drift at 70°C		-	±10	-	ppm/1000 hours	

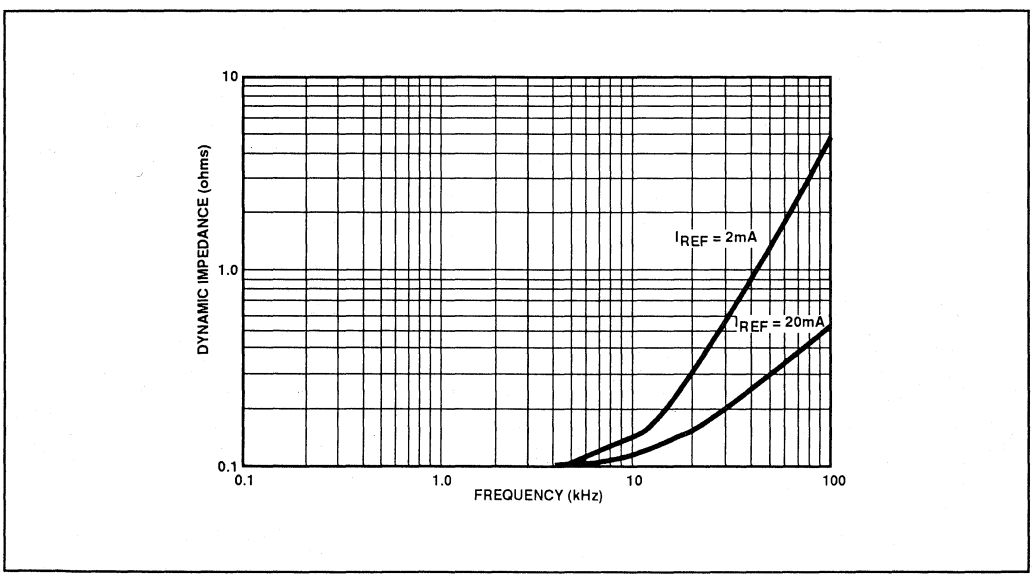


Fig.3 Dynamic impedance

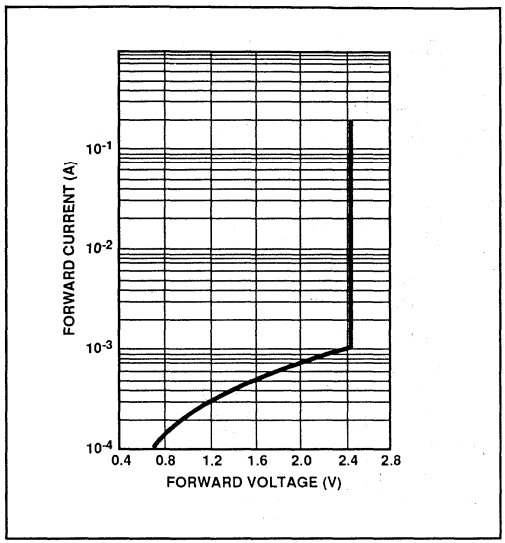


Fig.4 Forward characteristic

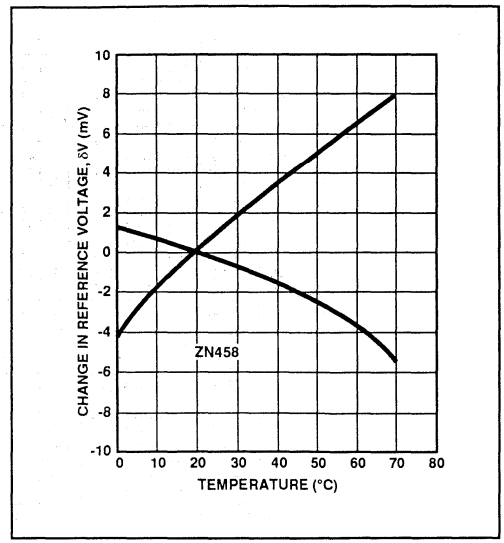


Fig.5 Temperature characteristic (typical)

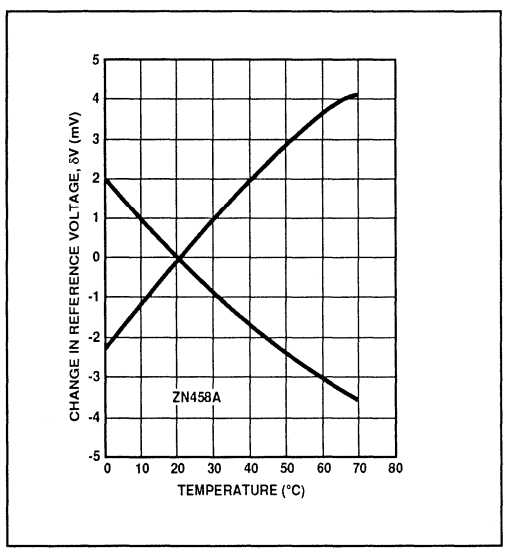


Fig.6 Temperature characteristic (typical)

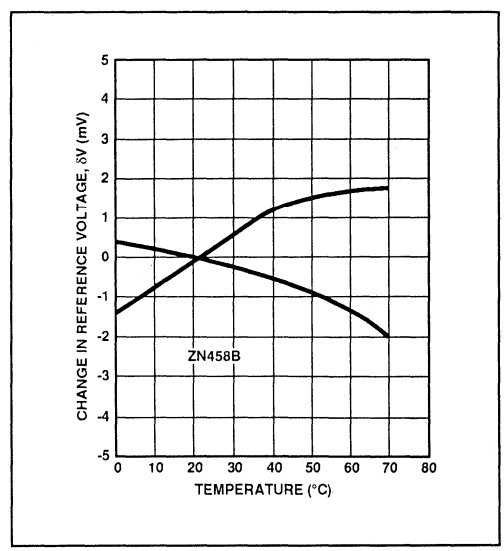


Fig.7 Temperature characteristic (typical)

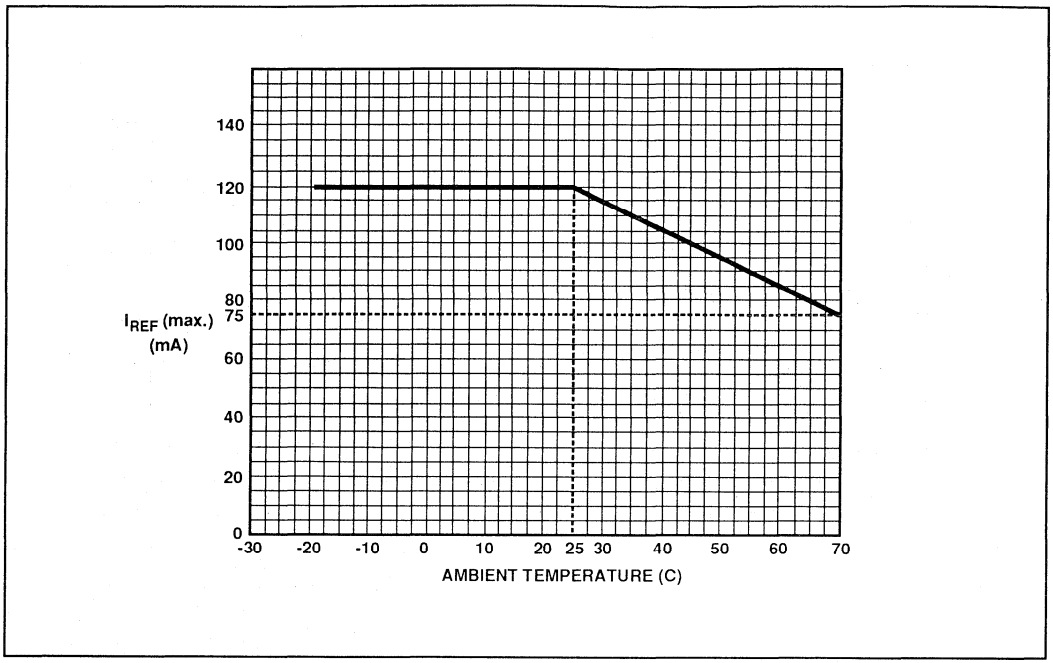


Fig.8 Derating curve

Section 8
Standard ECL

GEC PLESSEY
SEMICONDUCTORS

3028-2.1

SP1648
ECL OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of an inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0V dc supply or a -5.2V dc supply, depending upon system requirements.

Operating temperature range: 0°C to +75°C (Plastic)

Supply voltage	GND PINS	SUPPLY PINS
+5.0V dc	6,7	2,3
-5.2V dc	2,3	6,7

ORDERING INFORMATION

SP1648 MP (Industrial - Miniature Plastic Package)

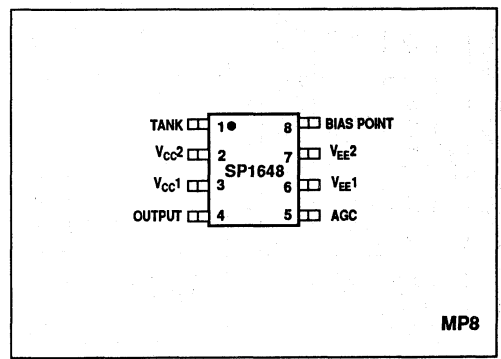


Fig.1 Pin connections (not to scale) - top view

ABSOLUTE MAXIMUM RATINGS

Power supply voltage V_{CC} - V_{EE} +8.0V
Output source current<40mA
AGC input V_{CC} to V_{EE}
Storage temperature range-55°C to +150°C (Plastic)
Operating junction temperature MP<150°C

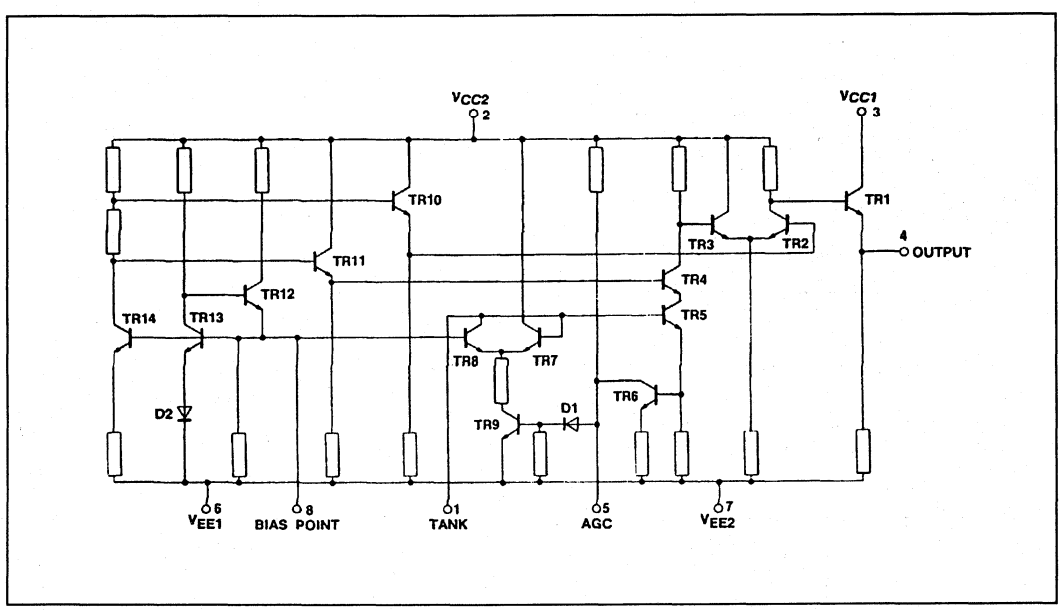


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: +5.0V

Characteristic	Symbol	Pin under test	SP1648 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH} Max.	V_{IL} Max.	V_{CC}	I_L	V_{EE} (Gnd)
Power supply drain current	I_E	7	-	-	-	40	-	-	mAdc	-	-	2,3	-	6,7
Logic '1' output voltage	V_{OH}	4	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	-	1	2,3	3	6,7
Logic'0' output voltage	V_{OL}	4	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	1	-	2,3	3	6,7
Bias voltage	V_{bias}*	8	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	-	-	2,3	-	6,7
			Min.	Typ. Max.	Min.	Typ. Max.	Min	Typ. Max.						
Peak-to-peak tank voltage	V_{p-p}	1	-	- -	-	500 -	-	- -	mV	see Fig.4	-	2,3	3	6,7
Output duty cycle	V_{DC}	4	-	- -	-	50 -	-	- -	%	see Fig.4	-	2,3	3	6,7
Oscillation frequency	f_{max}	-	-	- -	200	225 -	-	- -	MHz	see Fig.4	-	2,3	3	6,7

Test temp.	V_{IH} Max.	V_{IL} Min.	V_{CC}	I_L
-30°C	+1.960	+1.410	5.0	5.0
+25°C	+1.800	+1.300	5.0	5.0
+85°C	+1.680	+1.180	5.0	5.0

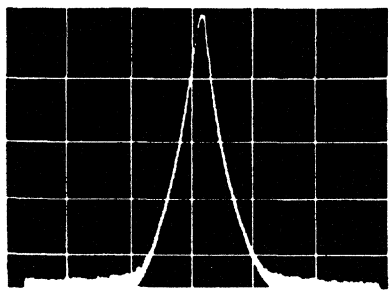
Thermal Characteristics:

MP8 Θ_{JA} = 163°C/W
Θ_{JC} = 57°C/W

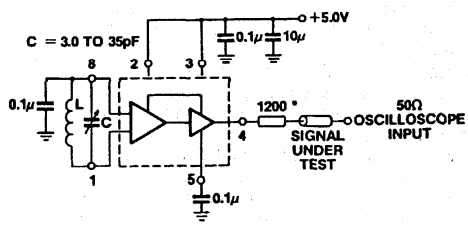
Supply Voltage: -5.2V

Characteristic	Symbol	Pin under test	SP1648 Test Limits -30°C Min.	-30°C Max.	+25°C Min.	+25°C Max.	+85°C Min.	+85°C Max.	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH} Max.	V_{IL} Max.	V_{CC}	I_L	V_{EE} (Gnd)
Power supply drain current	I_E	7	-	-	-	41	-	-	mAdc	-	-	6,7	-	2,3
Logic '1' output voltage	V_{OH}	4	1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	-	1	6,7	3	2,3
Logic'0' output voltage	V_{OL}	4	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	1	-	6,7	3	2,3
Bias voltage	V_{bias}*	8	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	-	-	6,7	-	2,3
			Min.	Typ. Max.	Min.	Typ. Max.	Min	Typ. Max.						
Peak-to-peak tank voltage	V_{p-p}	1	-	- -	-	500 -	-	- -	mV	see Fig.4	-	6,7	3	2,3
Output duty cycle	V_{DC}	4	-	- -	-	50 -	-	- -	%	see Fig.4	-	6,7	3	2,3
Oscillation frequency	f_{max}	-	-	- -	200	225 -	-	- -	MHz	see Fig.4	-	6,7	3	2,3

Test temp.	V_{IH} Max.	V_{IL} Min.	V_{CC}	I_L
-30°C	-3.240	-3.790	5.2	5.0
+25°C	-3.400	-3.900	5.2	5.0
+85°C	-3.520	-4.020	5.2	5.0



B.W. = 10kHz
Center Frequency = 100MHz
Scan Width = 50kHz/div
Vertical Scale = 10dB/div



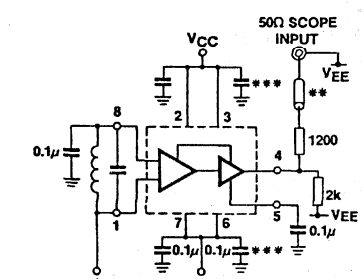
*The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

Fig.3 Spectral purity of signal at output

OPERATING CHARACTERISTICS

Fig.2 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 through TR14 provide this bias drive for the oscillator and output buffer. Fig.3 indicates the high spectral purity of the oscillator output.



*Use high impedance probe (>1.0MΩ must be used).

**The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

***Bypass only that supply opposite ground.

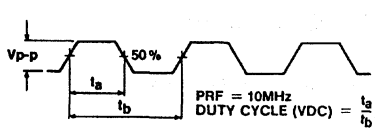


Fig.4 Test circuit and waveforms

When operating the oscillator in the voltage controlled mode (Fig.5), it should be noted that the cathode of the varactor diode, (D) should be biased at least $2V_{BE}$ above V_{EE} (≈1.4v for positive supply operation).

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Fig.6.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figs.7, 8 and 9. Figs.7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6pF typical). Fig.8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1kΩ resistor in Figs.7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51kΩ) in Fig.9 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\,(max) + C_S}}{\sqrt{C_D\,(min) + C_S}}$$

where $f_{min} = \dfrac{1}{2\pi\sqrt{L(C_D\,(max) + C_S)}}$

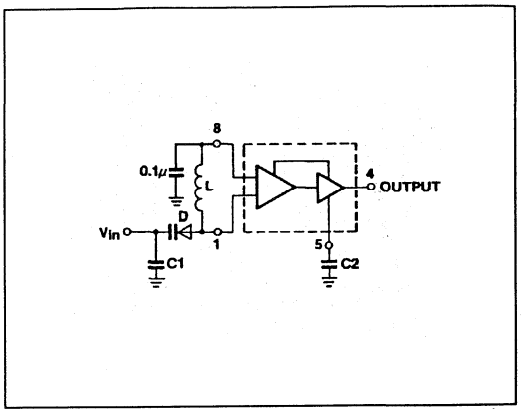


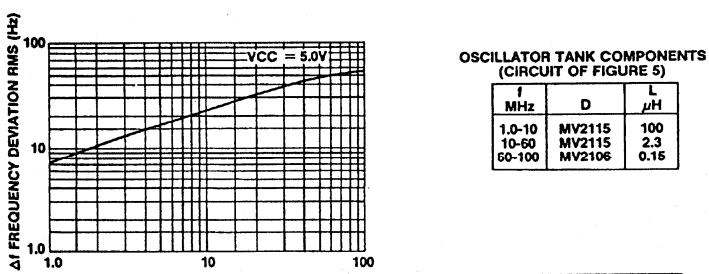
Fig.5 The SP1648 operating in the voltage-controlled mode

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

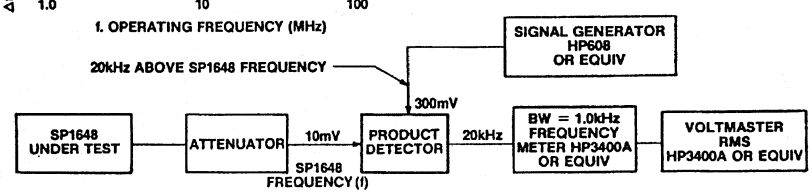
Good RF and low-frequency by-passing is necessary on the power supply pins (see Fig.3).

Capacitors (C1 and C2 of Fig.5) should be used to by-pass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.



OSCILLATOR TANK COMPONENTS
(CIRCUIT OF FIGURE 5)

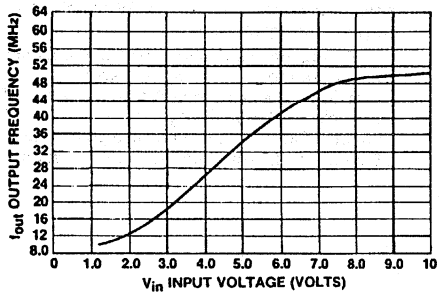
f MHz	D	L μH
1.0-10	MV2115	100
10-60	MV2115	2.3
60-100	MV2106	0.15



$$\text{FREQUENCY DEVIATION} = \frac{\text{(HP5210A OUTPUT VOLTAGE) (FULL SCALE FREQUENCY)}}{\text{1.0VOLT}}$$

Note: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimised prior to testing.

Fig.6 Frequency deviation test circuit



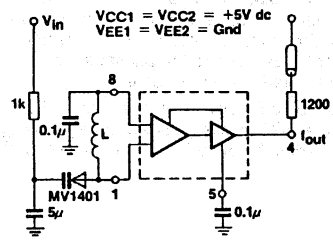
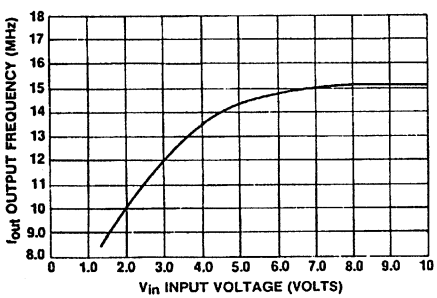


Fig.7



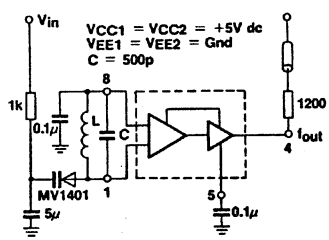
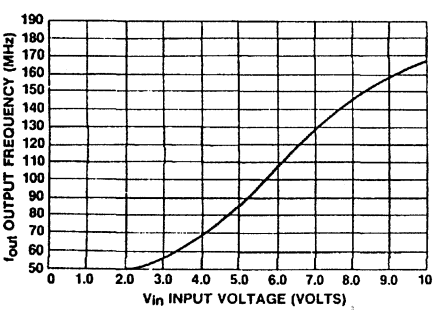


Fig.8



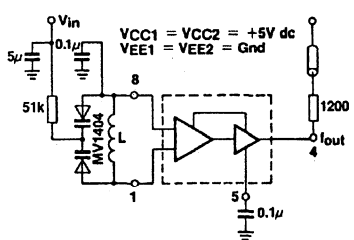


Fig.9

For output frequency operation between 1MHz and 50MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All by-passing should be as close to the package pins as possible to minimise unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0V supply is used, -5.2V if a negative supply is used).

At frequencies above 100MHz typ. it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by attaching a series resistor (1kΩ minimum) from the AGC to the most positive power potential (+5.0V if a +5.0V supply is used, ground if a -5.2V supply is used).

Section 9
Application Notes

GEC PLESSEY
SEMICONDUCTORS

DIGITAL TO ANALOG CONVERTERS

A digital to analog converter (DAC) is a device which converts a digital data input into a corresponding analog output. This output takes the form of a voltage or current.

IDEAL OUTPUT CHARACTERISTICS

If a unipolar voltage output and nominal binary coding are assumed, then the ideal transfer function of a linear DAC may be written as:

$$V_{out} = V_{FS} (B_1.2^{-1} + B_2.2^{-2} + B_3.2^{-3} + ... + B_n.2^{-n})$$

where B_1 is the most significant bit input (MSB) and B_n is the least significant bit input (LSB). Bits 1 to n can each assume a value of '1' or '0'. the number of bit inputs a DAC possesses is known as the **resolution** of the converter.

The smallest increment if output voltage is that contributed by the LSB and is equal to $V_{FS}.2^{-n}$.

The terms 'MSB', 'LSB' etc., are frequently used interchangeably to describe either the digital input or the corresponding analog output.

The maximum output from a DAC is known as full-scale output (V_{FSO}).

It occurs when all inputs are '1' and is equal to $V_{FS}\left(\frac{(2^n - 1)}{2^n}\right)$. For example the maximum output of a 3-bit DAC is $^7/_8\ V_{FS}$.

The transfer function graph of an ideal 3-bit DAC is shown in Fig.1. For each of the 8 input codes there exists a discrete analog output level, represented by a point on the graph. It

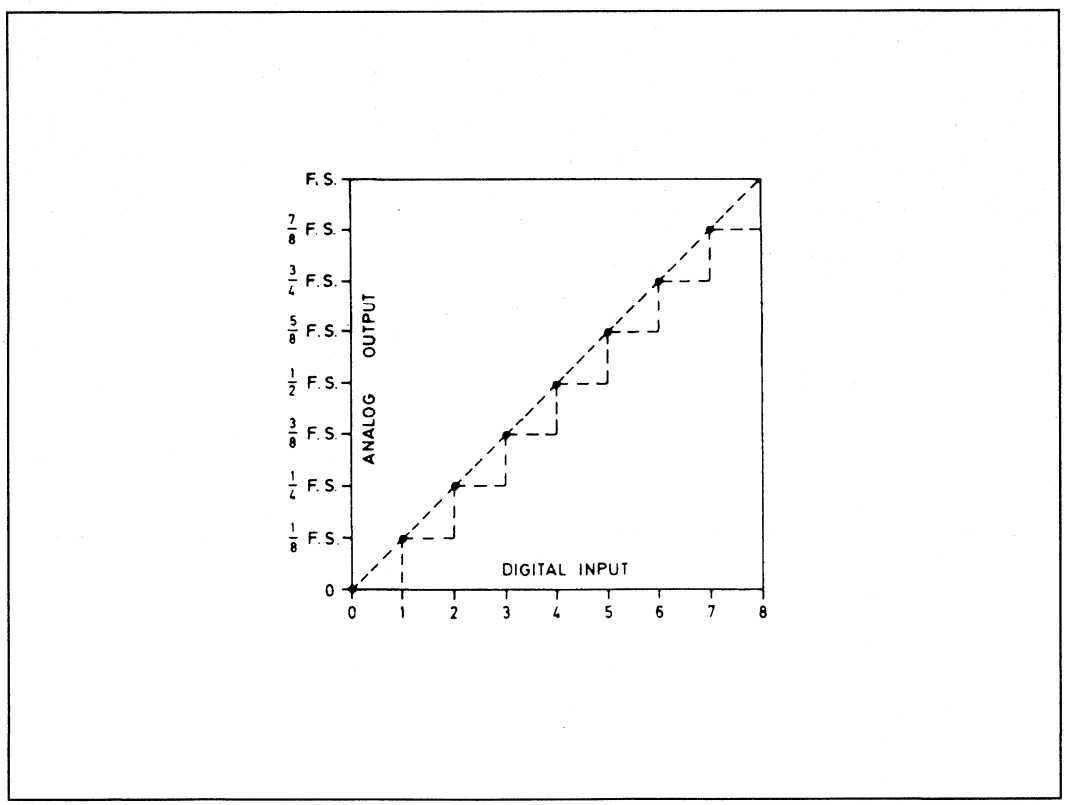


Fig.1 Transfer characteristics of ideal 3-bit DAC

should be emphasised that the transfer characteristics is not a continuous function and it is, therefore, not strictly correct to join the points with a continuous line, since this would imply that non-integral input codes and corresponding levels existed. However, a straight line is often drawn between zero and full-scale to represent the 'ideal' transfer function on which all the points should lie.

Similarly, if the input code of a DAC is incremented using, say a binary counter and clock generator, then the analog output will be a staircase waveform. DAC transfer functions are frequently drawn as a staircase, since this is a convenient way of illustrating various errors that may occur in a DAC. However, such a graph is, strictly speaking, a plot of analog output v time rather than output v input code.

PRACTICAL DAC CIRCUITS

Fig.2 shows an example of a 3-bit DAC circuit based on a voltage-switching R-2R ladder network, a technique widely used in GEC Plessey Semiconductors converters.

Each 2R element is connected either to 0V or V_{FS} (V_{REF}) by transistor switches. Binary weighted voltages are produced at the output of the R-2R ladder, the value being proportional to the digital input number.

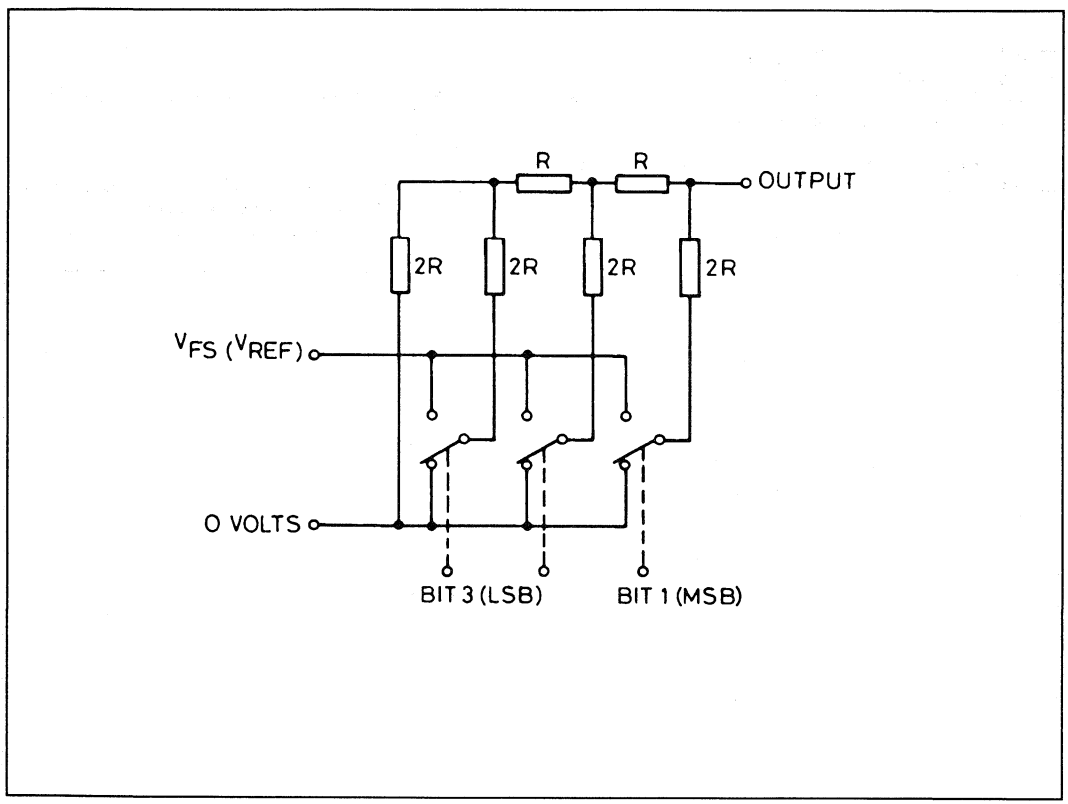


Fig.2 3-bit voltage switching DAC

For example, it is fairly easy to see that if bit 1 is '1' and bit 2 and 3 are '0' then an output of $V_{FS/2}$ is produced. This is because the resistance of the ladder looking from the output through the first R is 2R, which forms a 2:1 attenuator with the 2R is series with the MSB switch. Output voltages for other input codes can similarly by calculated, and it can be seen that the ladder may be extended to any number of bits.

D-A PARAMETERS AND DEFINITIONS

Converter errors

The ideal DAC assumes that all the resistors are perfectly matched and that the switches have zero resistance. In a practical converter this will not be the case and various errors will occur in the output.

Monotonicity

When the input code of a DAC is increased in 1 LSB steps the analog output of the DAC should also increase, staircase fashion. If the output always increases in this manner then the DAC is said to be monotonic, i.e. the output is a single-valued function of the input. If, due to errors in the bit weighting, the output of the DAC decreases at any step, as shown in Fig.3, then the DAC is said to be non-monotonic.

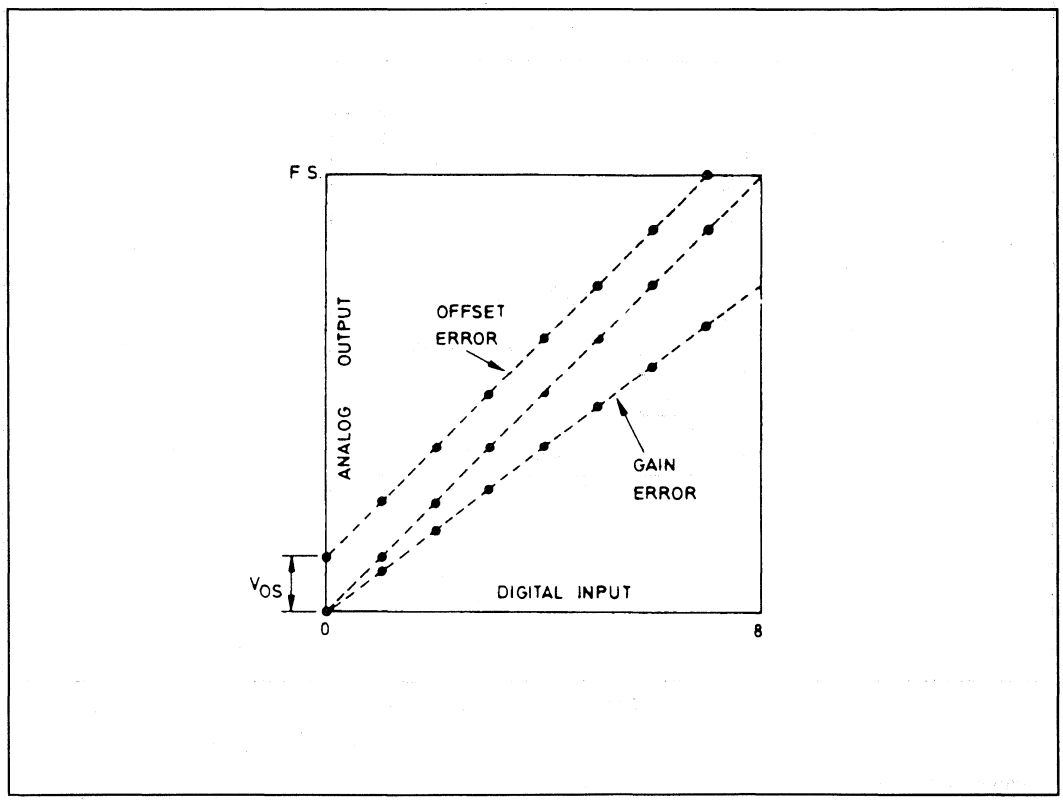


Fig.3 Non-monotonic DAC

Offset (zero error)
Assuming unipolar operation and normal binary coding, when the input code is zero then the DAC outputs should also be zero. However, due to package lead resistances and offset voltages in the switches this will not be the case, and a small output offset may be exist. This has the effect of shifting the transfer function so that it no longer passes through zero, as shown in Fig.4.

Gain error
If the reference voltage of a DAC is exactly the nominal value then the transfer characteristics of the converter should follow the ideal straight line. However, due to imperfections in the converter the transfer function may diverge from this line, as shown in Fig.4. This error is known as gain error and is the difference between the slope of the actual transfer characteristics and the slope of the ideal transfer characteristics.

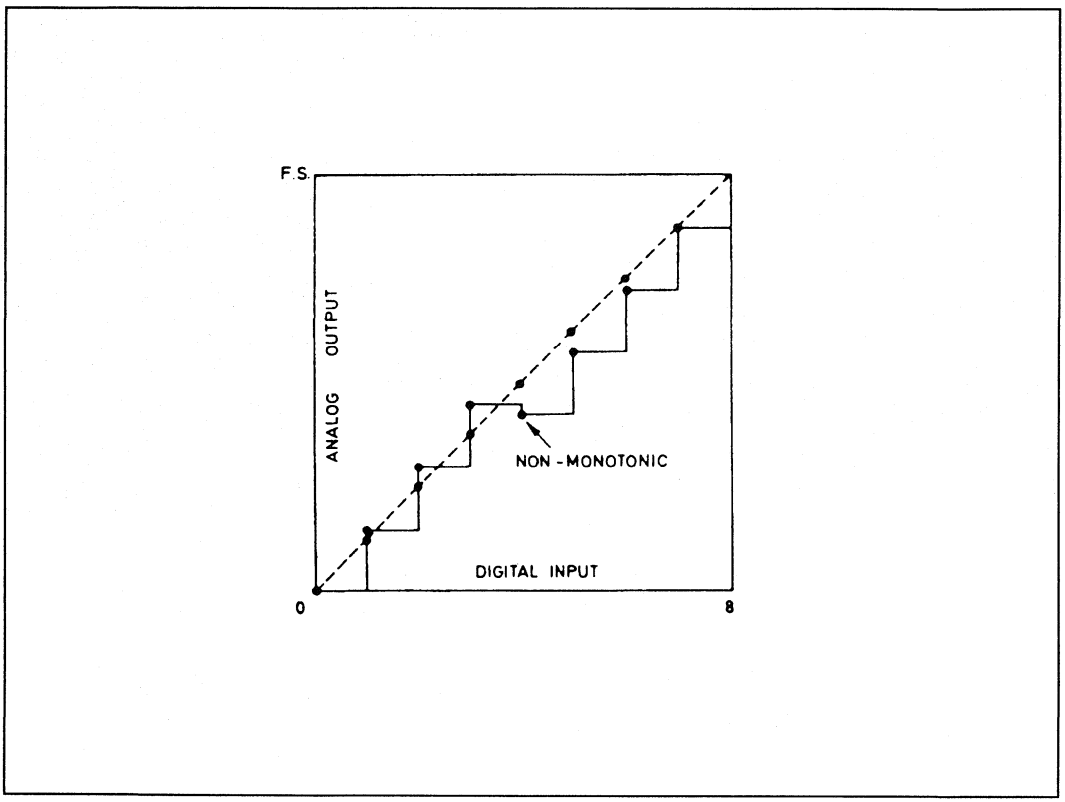


Fig.4 Illustrating offset and gain errors

Linearity errors
Offset and gain error may be trimmed out so that the end points of the transfer characteristics lie at zero and V_{FSO}. However, even when this has been done, some or all of the intermediate points may not lie on the 'ideal' line. These errors, which cannot be trimmed out, are known as linearity errors.

Non-linearity (linearity error)
This is the maximum amount, given either as a percentage of full-scale or fraction of an LSB, by which any point on the transfer characteristic deviates from the ideal straight line passing through zero and V_{FSO}. Non-linearity is illustrated in Fig.5. A linearity error within the range $\pm^1/_2$LSB assures monotonic operation. Note however that the converse is not true and a DAC may still be monotonic with large linearity errors, which is also shown by Fig.5.

Differential non-linearity
This is the maximum difference, specified as a fraction of an LSB, between the actual and ideal size of any one LSB analog increment. This can be seen as an error in the step height of a DAC staircase. A positive value of differential non-linearity means that the step height is larger than nominal, whilst a negative value means that it is smaller than nominal. If it is more negative than -1LSB then the DAC is non-monotonic. However, positive differential non-linearity may assume any value and a DAC can still be monotonic, as shown in Fig.5.

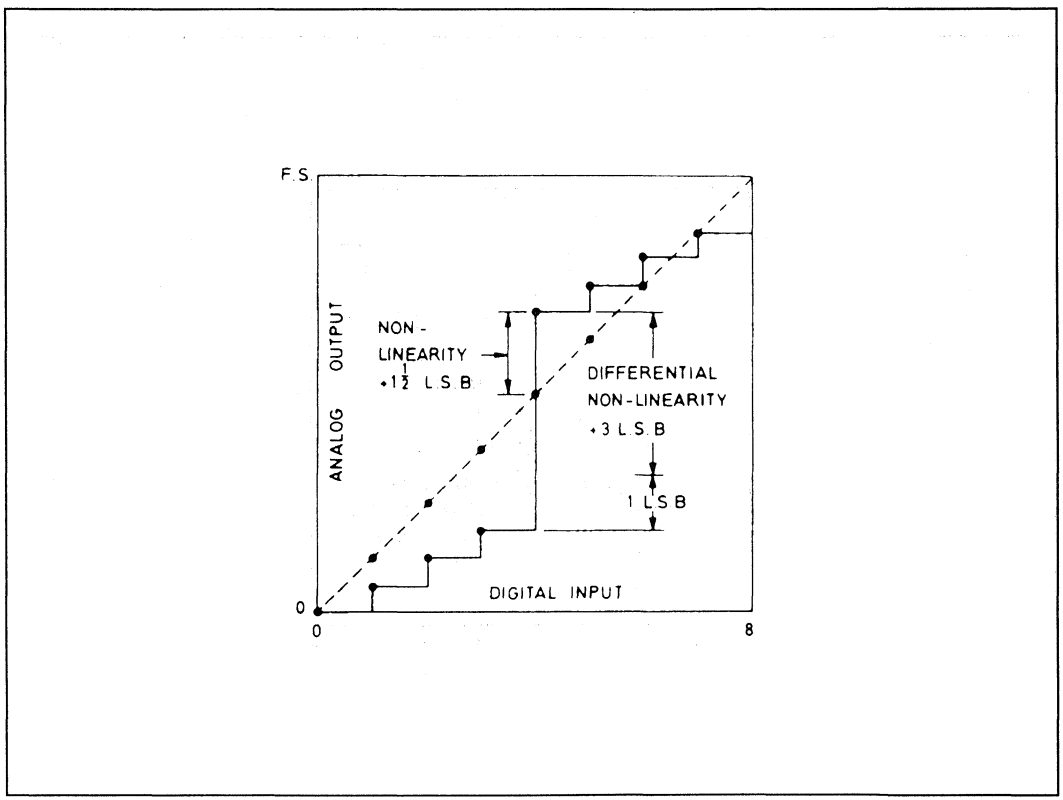


Fig.5 Illustrating linearity errors

Resolution

As stated earlier, the resolution of a DAC is simply the number of bit inputs that a DAC possesses, which indicates the smallest analog increment that the converter can produce as a fraction of V_{FS}. e.g. 8 bits = 1 part in 2^8(256). Resolution implies nothing about the accuracy of a DAC, which is defined by linearity and other errors.

Useful resolution

If an n bit DAC has a differential non-linearity of say -1.5LSB then it is non-monotonic. However, if the LSB input is made permanently '0' then the DAC becomes an n - 1 bit device with an LSB equal to twice the original LSB. The differential non-linearity error thus becomes -0.75 (new) LSB and the device is monotonic at a resolution of n - 1 bits. This is illustrated in Fig.6, which shows the transfer characteristic of a 3-bit DAC that has a useful resolution of 2 bits.

Due to manufacturing tolerances a proportion of n-bit converters will have only n - 1 ot n- 2 bit useful resolution. In applications not requiring n - bit useful resolution these reduced resolution versions offer a significant price advantage. The useful resolution of GEC Plessey Semiconductors DACs is guaranteed over their full operating temperature range.

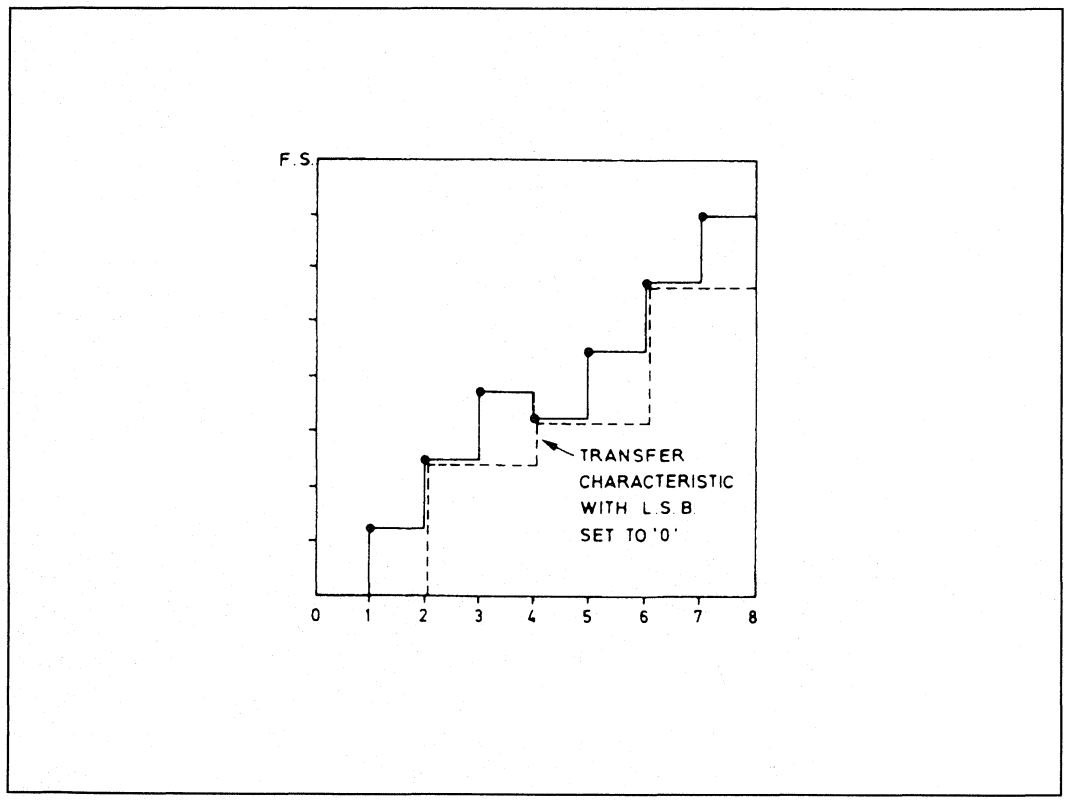


Fig.6 Non-monotonic 3-bit DAC with useful resolution of 2 bits

Settling time

Settling time is the time taken after a transition of the input code for the output of a DAC to settle to within $\pm^1/_2$LSB of its final value. This varies depending on which bits are being changed. It may be specified for a change of 1LSB which generally gives the most optimistic (fastest) figure. More conservative figures are given by the most major transistion (where the MSB changes in one direction and all other bits change in the opposite direction, e.g. 01111111 to 10000000 or vice versa) or by a change from all bits off to all bits on (00000000 to 11111111) or vice versa.

BIPOLAR OPERATION

The discussion so far has been concerned only with DACs producing a single polarity (usually positive) output voltage. In some applications a bipolar (both positive and negative) output range may be required.

This can be achieved by adding a negative offset of $\frac{V_{REF}}{2}$ to the analog output, as shown in Fig.7. For all input codes where the MSB is '0' the output voltage is then negative, and for output codes where the MSB is '1' the output voltage is positive. Where the input coding is normally binary but the output voltage is offset by $\frac{-V_{REF}}{2}$ then the input code is referred to as offset binary.

The transfer function of a 3-bit DAC with offset binary coding is shown in Fig.8.

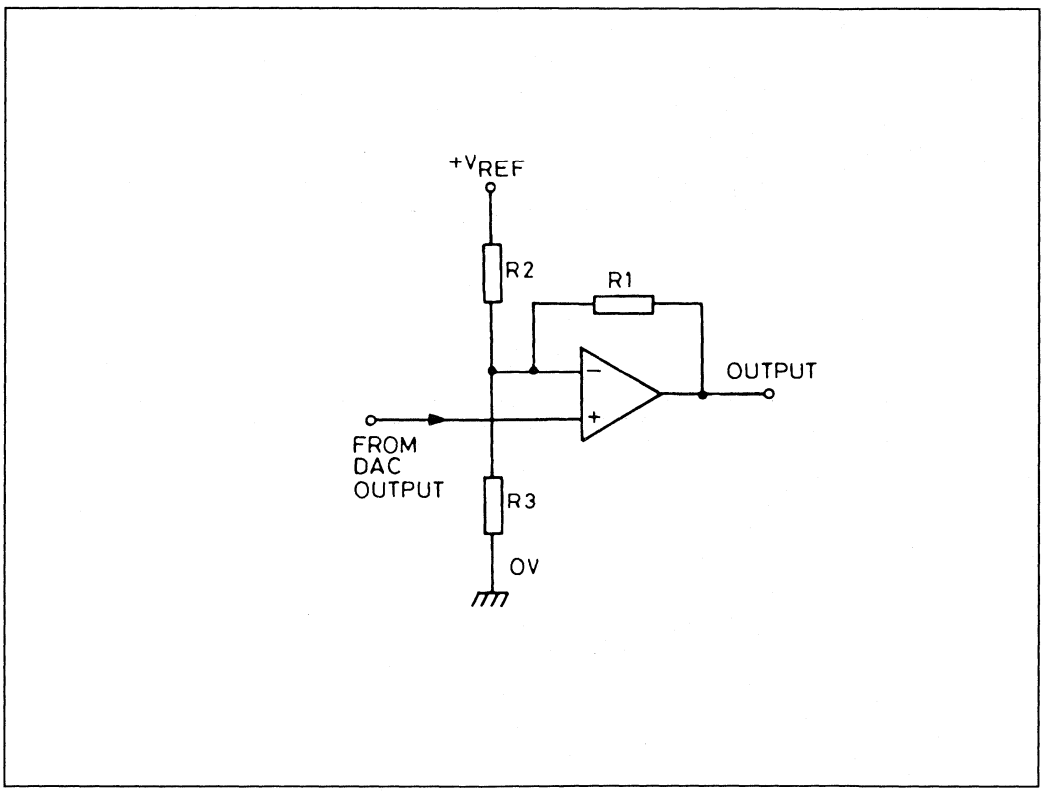


Fig.7 Bipolar operation of a DAC

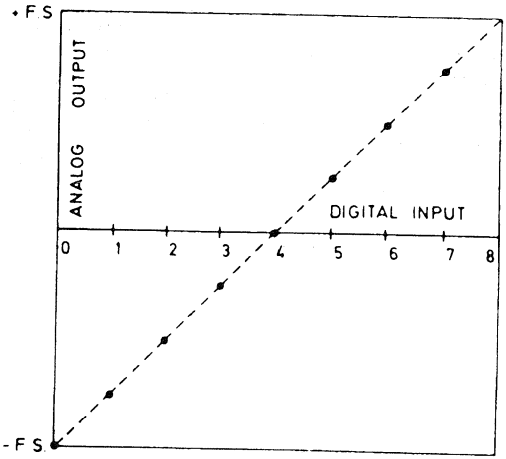


Fig.8 Bipolar operation of a 3-bit DAC

ANALOG TO DIGITAL CONVERTERS

An analog to digital converter (ADC) is a device which converts an analog input into a corresponding digital output code.

IDEAL OUTPUT CHARACTERISTICS

Assuming a unipolar voltage and binary coded output the transfer function of an ideal n-bit ADC is given by:

$$V_{FS}\,(B_1.2^{-1} + B_2.2^{-2} + B_3.2^{-3} + \ldots + B_n.2^{-n}) = V_{in} \pm {}^1/_2\text{LSB}.$$

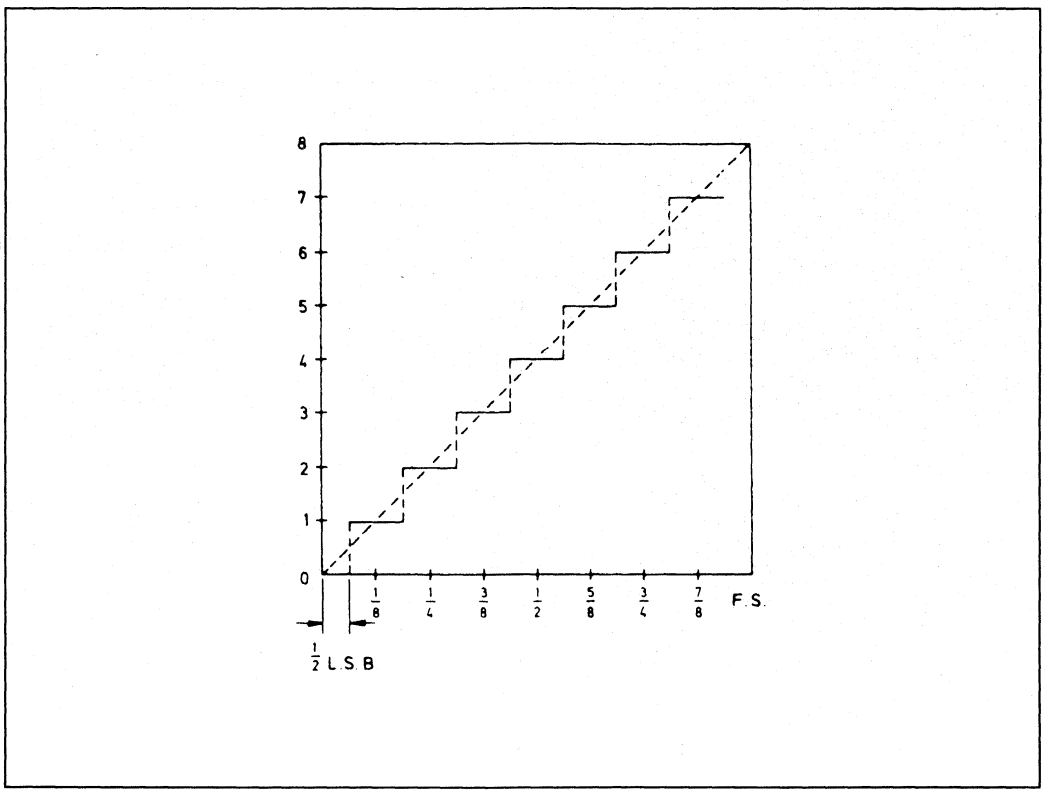


Fig.9 Ideal 3-bit ADC transfer characteristics

The transfer function of an ideal 3-bit ADC is shown in Fig.9. In this case there are 8 digital output codes corresponding to the 8 input codes of a DAC. However, unlike the analog output of a DAC, the analog input of an ADC can vary continuously, which means that each digital output code, with the exception of 0 and 7, exists over an analog increment of 1LSB. The zero of an ADC is usually trimmed so that the transitions between codes occur $\pm {}^1/_2$LSB on either side of the nominal analog input for a particular code. For example, the nominal input for output code 2 is ${}^1/_4\,V_{FS}$. The transition from 1 to 2 occurs at $\frac{3}{16}\,V_{FS}$ and the transition from 2 to 3 occurs at $\frac{5}{16}V_{FS}$.

As with a DAC, an 'ideal' straight line may be drawn through the transfer characteristic of an ADC.

PRACTICAL A-D CONVERSION METHODS

There are many methods of performing an analog to digital conversion; all of these methods are used in the current range A-D converters.

Parallel (flash) coversion

In an n-bit parallel converter (Fig.10) a resistor ladder is used to generate 2^n -1 voltage levels from 1LSB to (2^n -1) x LSB which are fed the reference inputs of 2^n -1 voltage comparators. the analog input signal is fed to the second input of each comparator, and is thus compared simultaneously with each of the 2^n -1 voltage levels. At the point in the comparator chain where the reference voltage exceeds the input voltage the comparator outputs will change over from low to high. The comparator outputs are encoded into whatever digital output coding is required.

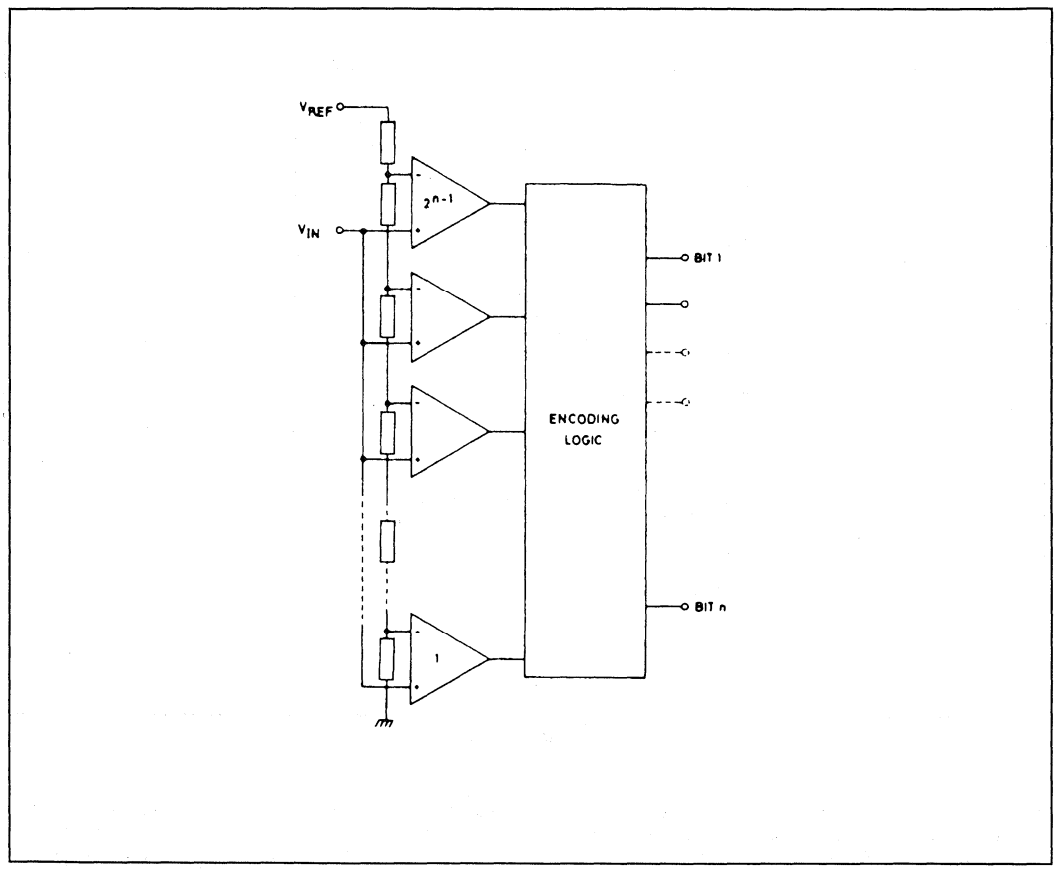


Fig.10 Parallel A-D converter

Since the only delays involved in the conversion are the propagation delay of one comparator plus logic propagation delays, parallel converters are very fast and may perform in excess of 10 million conversions per second. However, due to the large number of comparators required (63 for a 6-bit converter, 255 for an 8-bit converter) they are expensive to produce. Applications include digital video systems, digital storage oscilloscopes and radar data processing.

Staircase and comparator

In this type of ADC the input code of a DAC is incremented by a binary counter to give a staircase waveform, as shown in Fig.11. This is compared with the analog input and when the staircase exceeds the analog voltage the comparator output changes state and stops the clock. The count reached by the binary counter is thus the ADC output code. This method of A-D conversion is relatively slow, requiring 2^n -1 clock pulses for a full-scale conversion, where n is the number of bits. This conversion method is used in the ZN425 series of dual-purpose D-A/A-D converters.

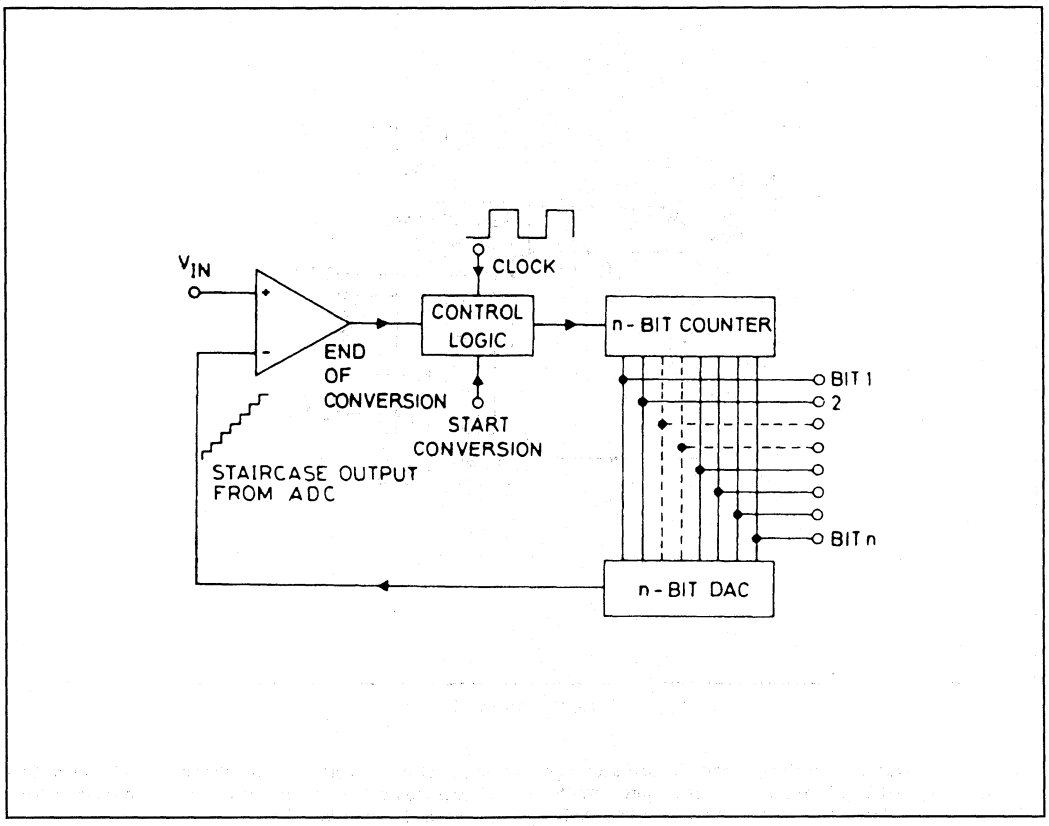


Fig.11 Staircase (ramp) and compare ADC

Tracking converters

As its name implies, a tracking converter can follow changing analog inputs. The principle operation is similar to that of the staircase and compare type of converter, but it uses an up/down counter and a window comparator, as shown in Fig.12. when the DAC output is less than the analog input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analog input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analog input $\pm^1/_2$LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in Fig.13. A tracking converter has speed advantages over a staircase and compare type, since the counter of the latter type can only count up, and must therefore be reset between conversions. In the case of a tracking converter, once it has performed an initial conversion starting from zero, any subsequent conversion require only that number of clock pluses necessary to track any increase or decrease in input voltage.

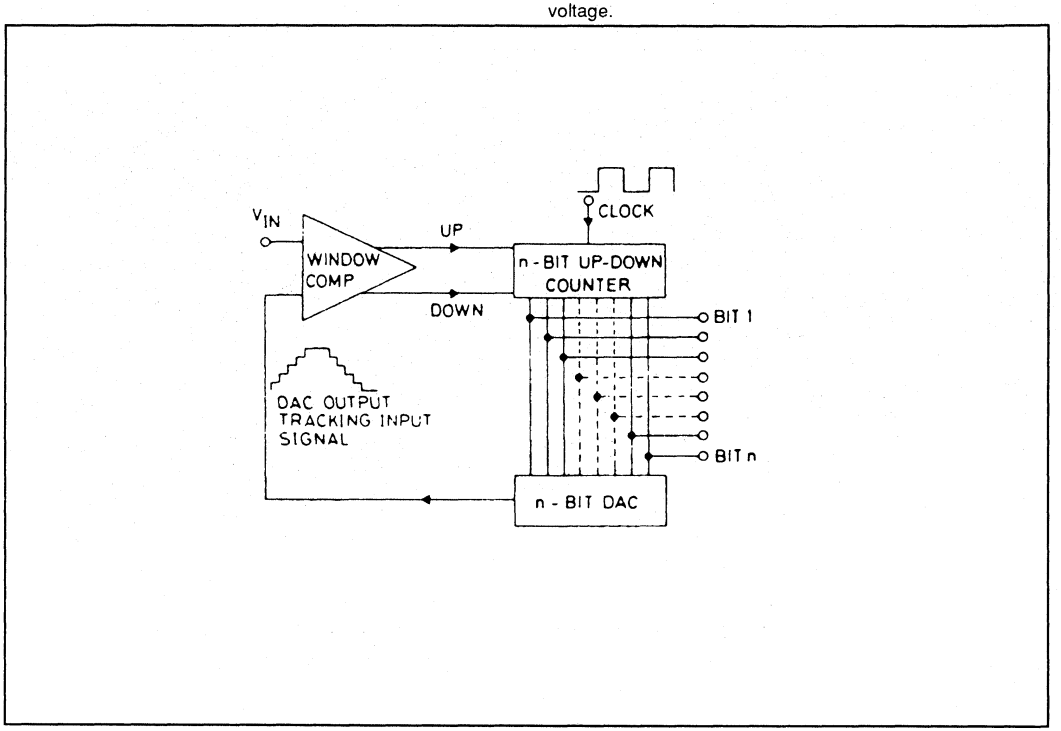


Fig.12 Tracking ADC

As an extreme example consider an analog input that change from V_{FSO} to (V_{FSO} -1LSB). The staircase and compare converter will require 2^n - 1 clock pulses for the first conversion and 2^n - 2 clock pulses for the second conversion.

The tracking converter on the other hand, will require 2n -1 clock pulses for the first conversion but only one clock pulse for the second conversion. This is illustrated in Fig.14.

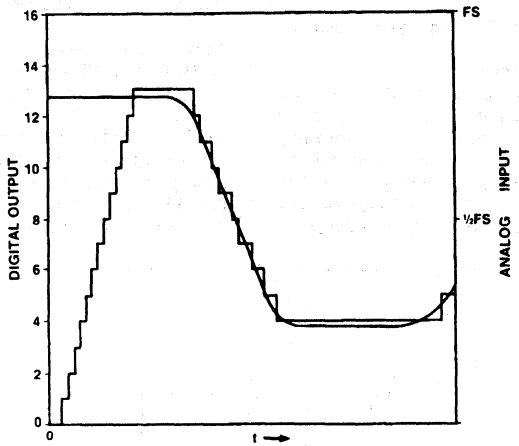


Fig. 13 Operation of tracking ADC

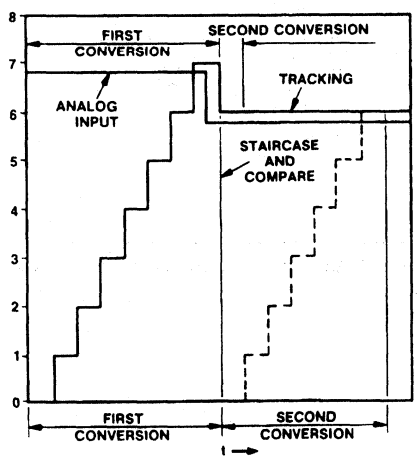


Fig. 14 Comparsion of ramp and compare and tracking ADC

In general it can be said that a tracking converter will follow signals whose rate of change is less than ±1LSB x clock frequency. If this condition is met there is no need to use a sample-and-hold circuit on the analog input.

A tracking technique is used in the ZN433 series of converters.

Successive approximation converters

The operation of a staircase and compare ADC is analogous to weighing, say an 11 gramme weight, on a balance by adding one gramme weights until the scale tips, which is clearly a very slow method. A faster procedure, known as successive approximation, uses weights of 16, 8, 4, 2 and 1 grammes. The 16 gramme weight is tried first and is discarded because it tips the scale. The 8 gramme weight is tried next, and is left on the pan. Next the 4 gramme weight is tried and discarded, and the 2 and 1 gramme weights are tried and retained. The final result is the sum of the weights remaining on the scale pan, and the operation has taken 5 'cycles' as opposed to 11 'cycles' for the staircase and compare method.

The principle of a successive approximation ADC is identical. the MSB of a DAC is first set to '1' and the output is compared to the analog input. If it is greater than the input the MSB is reset to '0', otherwise it is left at '1'. The next bit is then set to '1' and the DAC output is again compared to the analog input. Again it is either reset or left at '1' depending on the result of the comparison. This procedure is repeated for every bit down to the LSB, and the final code to the DAC is the output code of the ADC. A successive approximation cycle is illustrated in Fig.15.

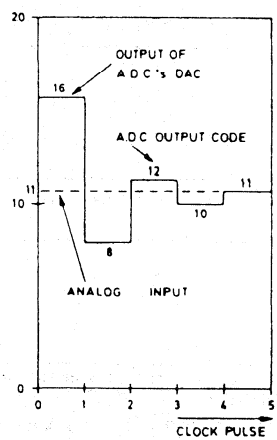


Fig.15 Operation of a successive approximation ADC

The successive approximation technique is used in most of the GEC Plessey Semiconductors data converters that operate below video speeds.

Dual-slope converters

Dual-slope integration is one of the slowest methods of A-D conversion, but it offers high resolution at a modest cost.

A block diagram of a dual-slope converter is shown in Fig.16.

It operates in the following manner: Switch S1 is closed by the control logic, S4 is opened and the input voltage is integrated for n clock periods, where n is usually the maximum count of the counter. At the end of this time the integrator output voltage, V_o, is $\frac{-V_{in}\, n\, T_c}{RC}$ where T_c is the clock period. This is shown in Fig.17.

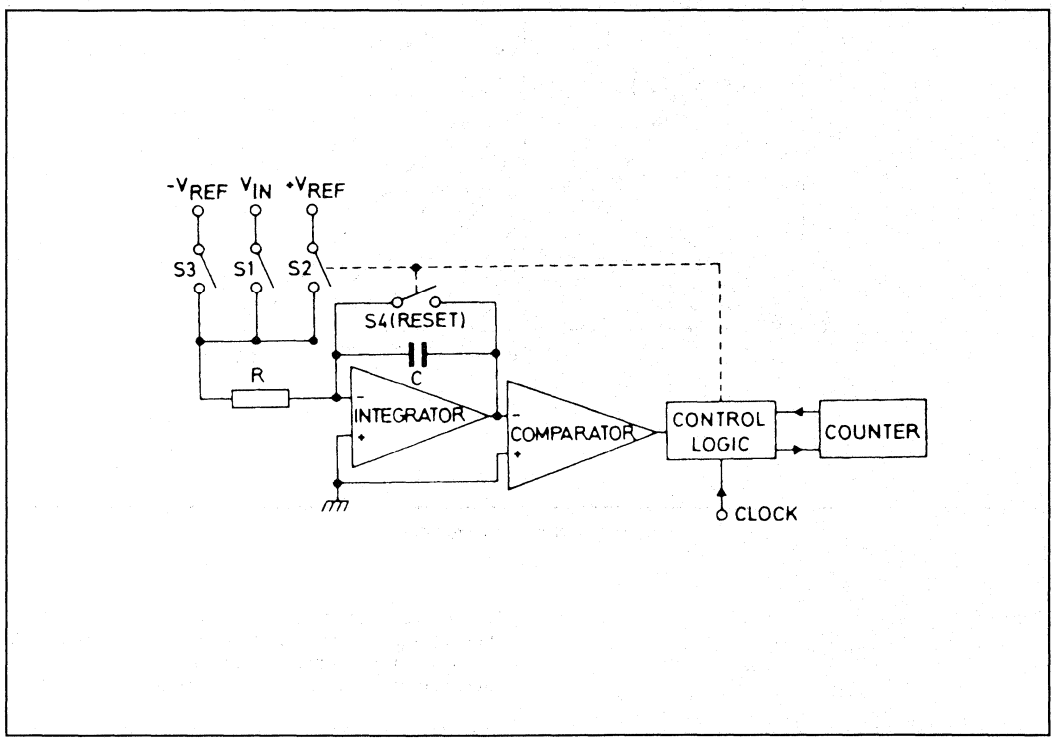


Fig.16 Dual-slope ADC

During this period the polarity of the input signal is detected by the comparator. At the end of the integration period S1 is opened and, depending on the polarity of V_{in}, either S2 or S3 is closed to connect the integrator to a reference voltage of opposite polarity to V_{in}. The counter is now allowed to count from Zero until the integrator output reaches 0V, when the comparator output changes state and the counter is stopped. Since the integration is over the same voltage range (V_o),

$V_o = \frac{-V_{REF}\, X\, T_c}{RC}$, where X is the count reached by the time the integrator output crosses zero.

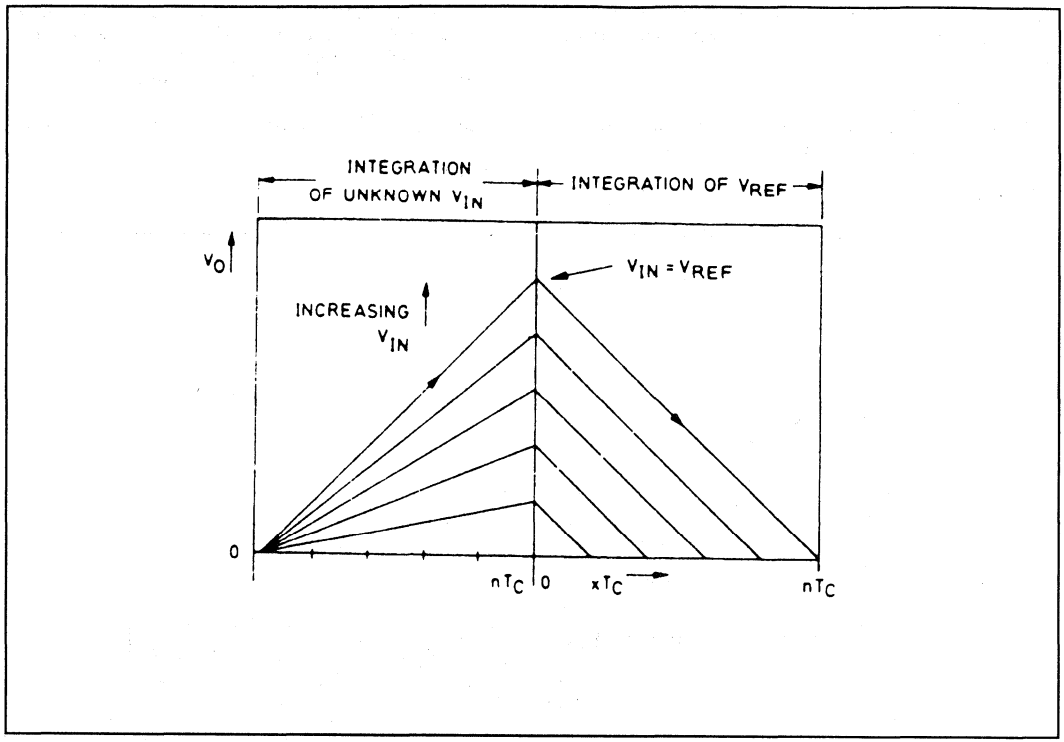


Fig.17 Operation of dual-slope ADC

Thus

$$\frac{V_{in} n T_c}{RC} = \frac{V_{REF} X T_c}{RC}$$

$$\text{or } X = \frac{V_{in} n}{V_{REF}}$$

Since n and V_{REF} are both fixed the output count is proportional to the input voltage. Since both the first and second integrations occur under identical conditions the converter is unaffected by any long term variations in T_c, R or C, as demonstrated by the disappearance of these terms from the final equation. The only factors affecting the accuaracy of the converter are (1), the stability of V_{REF} (2) the stability of the 'on' resistance of S1 to S3 and (3) drift in the integrator and comparator op-amps. These affects can be minimised by careful design.

Dual-slope converters are generally used where high resolution and low cost are more important than speed, for example in digital voltmeters.

The ZNA216 is a DVM logic sub-system containing the clock, counter and all control logic necessary for dual-slope converter or DVM.

A-D PARAMETERS AND DEFINITIONS

A-D converter errors

Like DACs, practical ADCs are subject to a number of error sources, and since most ADCs contain a reference DAC, many of these error sources are the same for both types of converters.

Quantising error (uncertainty)

Quantising errror is an ADC specification that has no counterpart in DAC specifications. For each input code of a DAC there is a unique analog output level, but for any ADC output code there is a 1LSB range of analog input levels. It is thus not possible to tell from the output code the precise value of the analog level, there being a quantising error or uncertainly of $\pm^1/_2$LSB. Since all ADCs have this inherent quantising error the parameter is frequently not quoted in specifications.

Missing codes

Missing codes are perhaps best explained by considering the operation of a staircase and compare type 3-bit ADC which has a non-monotonic DAC, as shown in Fig.18. The reference DAC exhibits non-monotonicity at input code 4, i.e. step 4 of the staircase decreases. There is thus no way in which the counter can be stopped at this code. If the analog input is less than the DAC output for code 3 then the comparator will stop the counter before 4 is reached. If the analog input is greater than output 3 it must also be greater than output 4, so the comparator will not change state at code 4.

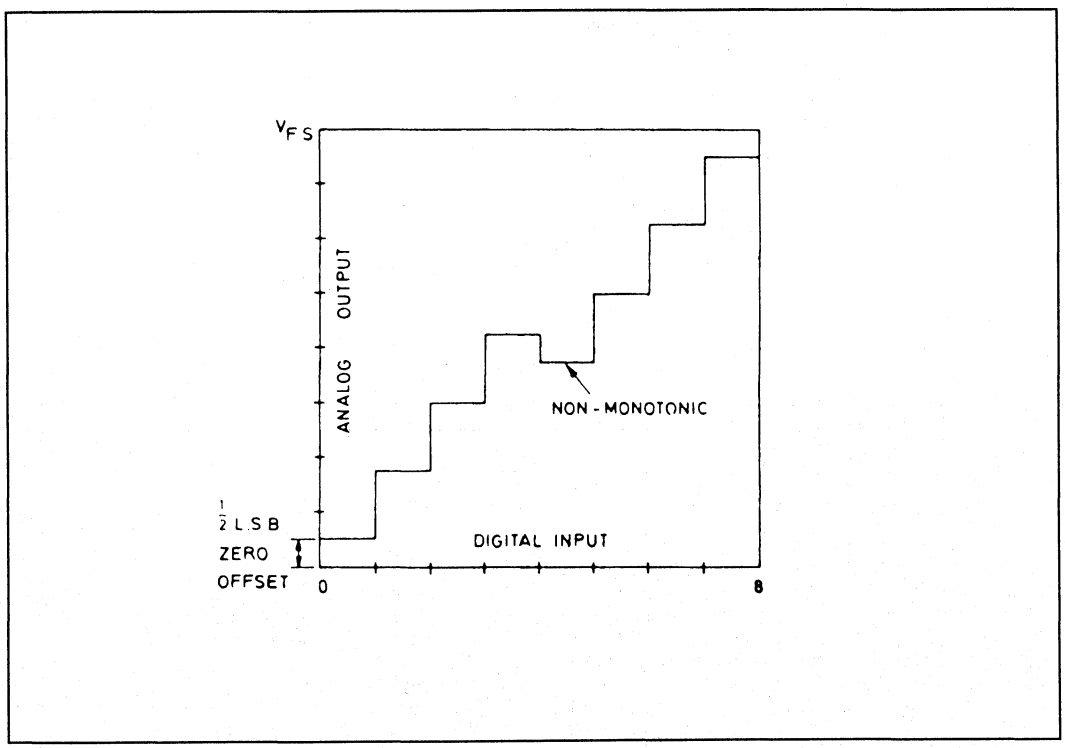


Fig.18 Non-monotonic DAC used in an ADC

Output code 4 will thus never appear and is known as a 'missing' code. The transfer function of an ADC with a missing code is shown in Fig.19.

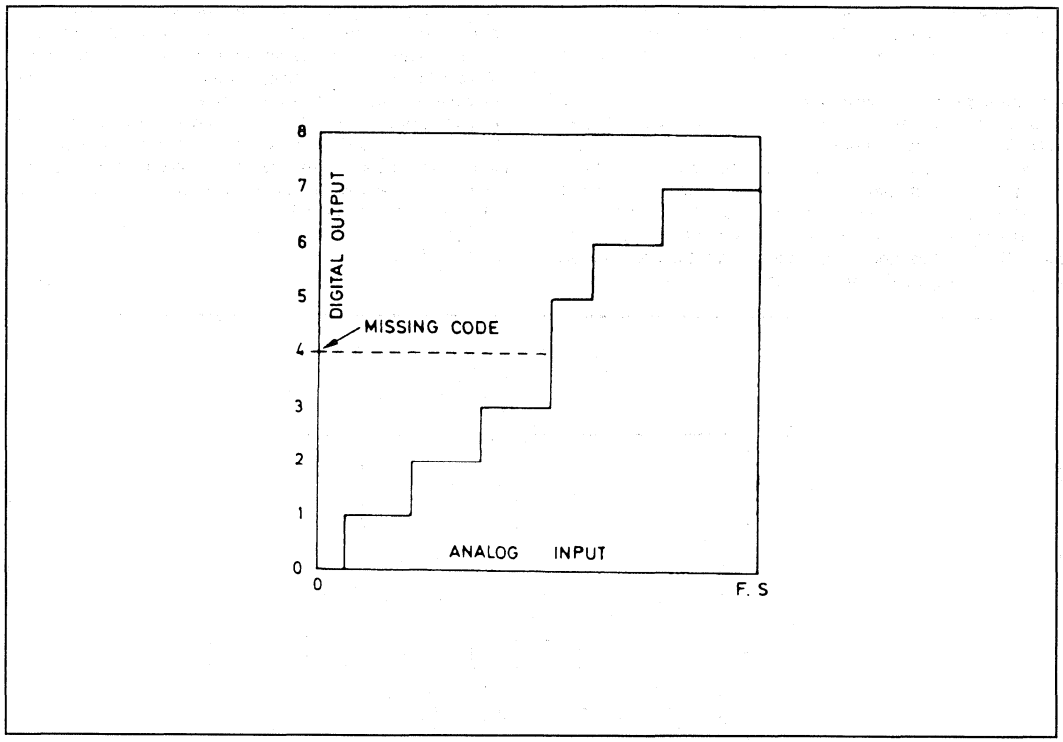


Fig.19 ADC with missing code

Zero transition
As explained earlier, the zero of an ADC is usually trimmed so that the output transition from 0 to 1 occurs at an input level corresponding to $^1/_2$LSB, i.e. $1/2 \frac{V_{FS}}{2^n}$. However, as supplied the reference DAC of an ADC IC will not have the $^1/_2$LSB offset necessary to achieve this. This zero transition will thus occur at 1LSB plus the DAC zero error, plus the comparator offset voltage. These three parameters are frequently lumped together as the (untrimmed) zero transition of the ADC.

Gain error
This is the difference between the slope of a line drawn between the actual zero and full-scale transition points and that of a line drawn through the ideal transition points.

Non-linearity (linearity error)
Non-linearity is the maximum amount by which any actual transition points deviates from the corresponding ideal transition point. It is specified as a percentage of full-scale or a fraction of an LSB. A linearity error of less than $\pm^1/_2$LSB assures no missing codes.

Differential non-linearity
This is the maximum difference between any 1LSB increment of the analog input and the ideal size of an LSB increment

$\frac{V_{FS}}{2^n}$. Differential non-linearity of less than 1LSB guarantees no missing codes.

Resolution
The resolution of an ADC is simply the number of bits outputs that the converter possesses. As with a DAC, resolution implies nothing about the accuracy of a device.

Useful resolution
Useful resolution is the resolution (number of bits) at which an ADC has no missing codes, which for GEC Plessey Semiconductors ADCs are guaranteed over the operating temperature range. As with DACs, an n-bit ADC may have a useful resolution less than n bits, for reasons previously explained.

Conversion time
The time taken for an ADC to perform a complete conversion is known as the conversion time. For successive approximation converters conversion time is fixed by the number of bits and the clock frequency. However, for the other types, conversion time may vary with input voltage. for example, a ramp and compare ADC requires 2n -1 clock pulses for a full-scale conversion but only one clock pulse for a one bit conversion. It is thus important to check exactly what is being specified.

BIPOLAR OPERATION

As with a DAC, an ADC may be used for bipolar operation.

Taking the ZN427 as an example the input is offset by $\frac{+V_{REF}}{2}$ so that the input voltage presented to the ADC is always positive, even with negative input voltages down to $\frac{-V_{REF}}{2}$.

The principle of offsetting an ADC input is illustrated in Fig.20, whilst the transfer function of a 3-bit bipolar ADC is shown in Fig.21. In this case the **output** coding is known as offset binary.

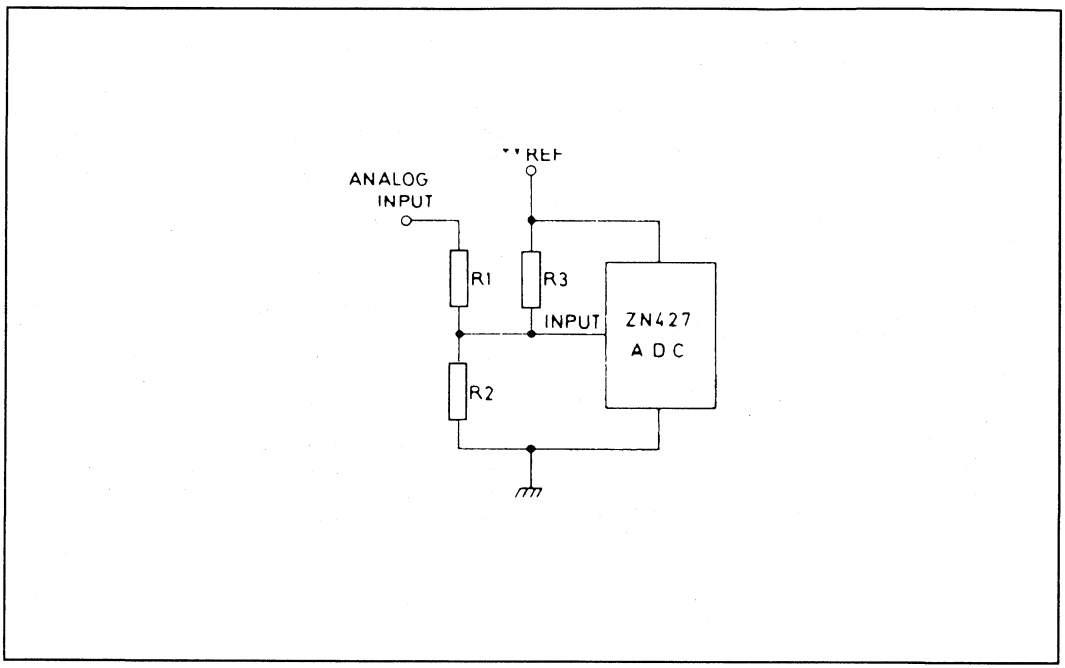


Fig.20 Bipolar operation of an ADC

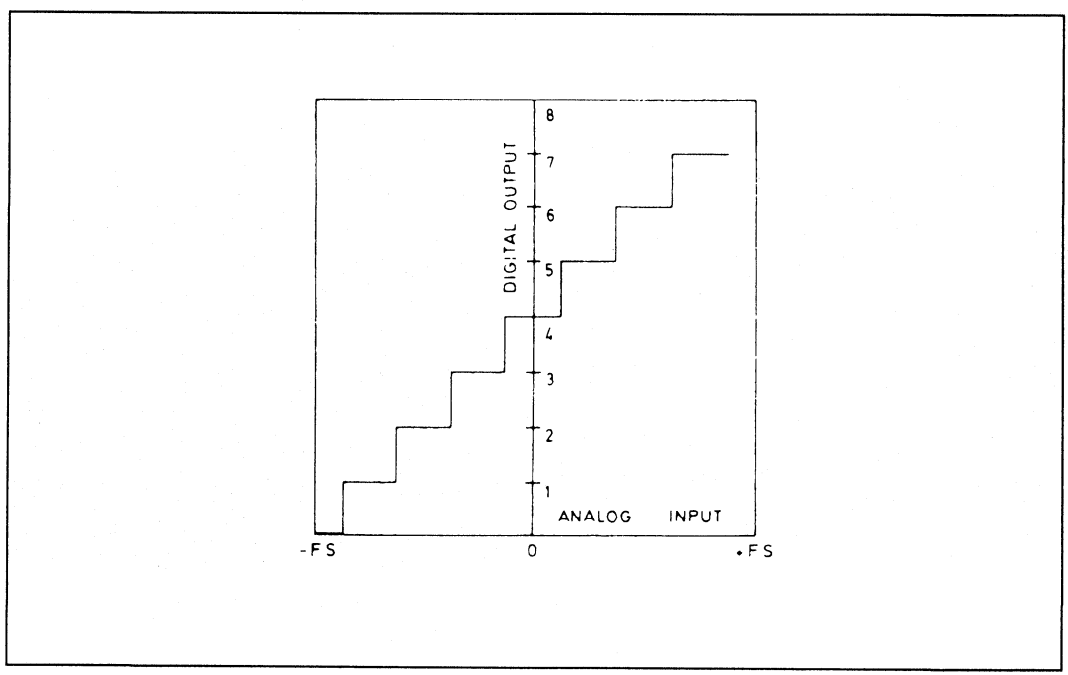


Fig.21 Bipolar transfer characteristics of an ADC

EVALUATION AND COMPARISON OF HIGH SPEED ADCs

High speed ADCs are used in many varieties of applications; each application may require special consideration of one or more particular parameters. For example, designers of video (radar or TV) would pay particular attention to differential linearity, whereas designers using the ADC for measurement systems would need to pay attention to integral linearity. Other systems may need accurate information on analog power bandwidth or bit error rate.

Specification requirements therefore differ from application to application, and this can make comparisons of ADCs difficult. Outlined below are important tests and evaluation methods, starting with the most simple and progressing to the more sophisticated.

ADC evaluation falls into two main groups: the first group utilises high speed digital–to–analog converters to reconstruct the digital output into an analog form that can then be displayed on an oscilloscope. The second group of methods looks directly at the digital data. This requires a high speed logic analyser and usually a GPIB compatible desk top computer.

TESTS USING DAC RECONSTRUCTION

Method 1, Low Speed Ramp (Fig.1)

This test is very simple. A linear full scale triangular wave (or ramp) is applied to the ADC input, at a frequency that is less than $f_{CLOCK}/(2x2^N)$, where N=number of bits. This ensures that all the timing intervals are displayed. The output from the ADC is then reconstructed with a DAC which should have a greater resolution than the ADC to ensure that all output codes are displayed. The results can then be viewed on a good high resolution oscilloscope.

The resultant staircase has vertical voltages that are due to the DAC and horizontal time intervals that are due to the ADC. Therefore any vertical errors can be ignored as they are due to the DAC alone. The horizontal time intervals can be viewed in more detail by using the oscilloscope to invert and add the input signal. The remainder will be the quantisation noise. The error will be 1 LSB high $\pm$½ an LSB. Beware of 'scope input overload and the delay between the two signals when using this method.

A major point of interest on this reconstructed ramp is the mid–step or zero crossing where a large differential error or high speed group of glitches can occur. This is a common problem with many ADCs as the digital section of the ADC is changing from 10000000 to 01111111. All the binary outputs are changing at once and hence large current spikes can result.

Another cause of zero crossing error is four stage design. Within most 8–bit flash ADCs the reference chain and/or the comparators are split into four ranks. The device can then behave as four 6–bit devices. This can give poor differential steps at seven critical codes along this ramp.

Reference Voltage Considerations

The overall accuracy of the staircase will be mostly proportional to the reference voltage. This is because the internal comparator offsets will remain constant while the bit size will vary proportionally to the external reference voltage. Therefore it is important to consider the reference voltage before making comparisons between ADC linearity figures. Disadvantages of the ramp method are (a) it is difficult to obtain numerical results – although this can be achieved using a Tektronix 7854 scope – and (b) this test does not reflect the accuracy at speed.

Method 2. Near Nyquist Beat (Fig. 2)

The Nyquist frequency is exactly one half the clock frequency. If a sinewave analog input is set close to this frequency in an unfiltered system, a beat will result. The beat frequency will be

$$f_B = \left| \frac{f_C}{2} - f_{in} \right| \quad (3MHz \text{ in Fig. } 2)$$

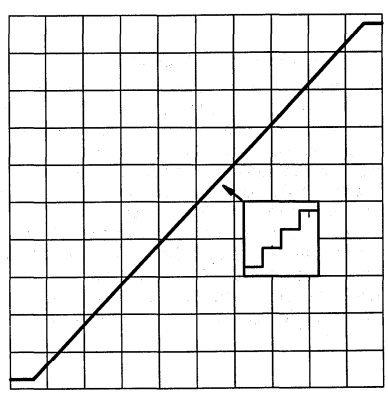


Fig. 1 ADC linearity. 1kHz ramp input sampled at 100MHz (2V I/P to ADC)

This test is primarily for evaluation of analog bandwidth. The comparators acquire the input voltages at each end of the input dynamic range on successive samples. An ADC that can slew both positively and negatively fast enough to produce an undistorted sinewave beat contains an extremely fast comparator section. Disadvantages of this method are (a)

again it is difficult to produce a numerical value of merit. (b) scope triggering is delicate and (c) DAC overshoot can cloud the results.

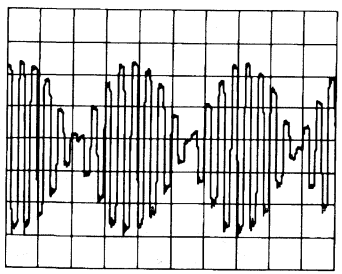


Fig. 2 ADC near Nyquist beat. 47MHz input sampled at 100MHz, 2V I/P to ADC

TESTS USING DIRECT DIGITAL ANALYSIS

This group of tests is performed by acquiring the digital data directly from the ADC. The data is usually acquired by a high speed logic analyser and then transferred to a desk–top computer for analysis. The ADC is usually driven with a sinewave of full amplitude. The following gives the more popular methods of analysing and plotting the data. It is essential with all the following methods that the input is set to precisely full scale.

Most of the methods below benefit from phase locked sampling (stationary sampling). In most cases this enables the number of samples taken to be greatly reduced, therefore improving test/evaluation times.

Method 1. Histogram Test (Fig.3)

This test plots the output code against occupancy of the code. A histogram is produced that should theoretically form a sinewave cusp. Deviations from this cusp will represent differential and integral linearity errors. A differential error would weight the probability of a code being occupied, either more or less than it should be over a large number of samples. This distorts the cusp in a positive or negative direction at the code in question. The advantage of this test is that it will indicate the dynamic accuracy of the ADC, i.e. the accuracy to input frequencies up to Nyquist. This is of course not practical using a DAC and oscilloscope. The disadvantages of this method are that (a) it requires a large number of samples and (b) as a cusp is formed, direct reading of linearity from the curve is difficult.

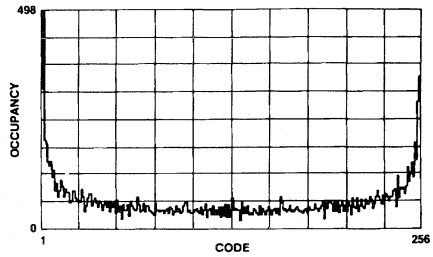


Fig. 3 Histogram test at 30MHz input

Method 2. Non–linearity in LSB (Fig. 4)

This test is almost identical to the histogram method. The same data can be used within the desk–top computer. Again a large numer of samples are taken and again the occupancy of each code is plotted. The subtle difference is that a $\sin^{-1}$ weighting is applied to the results which removes the cusp. The linearity is then plotted:

$$\left[1 - \frac{(Actual\ Probability)}{(\sin^{-1}\ Weighted\ Probability)}\right].$$

As the cusp has been removed, the resulting graph shows at a glance differential non–linearity in terms of LSB. This test can also be performed up to Nyquist limits. Disadvantages are that random errors are averaged out.

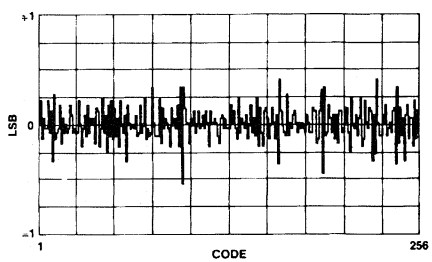


Fig. 4 Differential non–linearity in LSB

Method 3. Accumulation Error (Fig. 5)

Again, this test can be performed from the initial data. The data is processed to give a graph of integral linearity which can be expressed in two main ways – 'end point' or 'best fit'. The 'best fit' method allows the points to be compared with a line

drawn through the average of the results. The 'end point' method is more severe as the line is defined by the end points of the results. From fig.5 we could quote an integral linearity of ±0.5LSB for 'best fit' but only ±0.75 LSB for 'end point'. Therefore it is very important to know which method has been used before comparing integral linearity figures.

To form the graph a statistical method is used with many samples taken. The results are corrected for the sinewave cusp and a graph plotted of levels against deviation from the previously defined straight line. This method can also be performed at frequencies up to Nyquist Fig. 6 shows a plot of end point integral linearity at near Nyquist frequencies for a typical 8–bit flash ADC. As this test represents the total deviation from a theoretically perfect ADC it is a very useful measurement. It also gives a clear representation of distortion caused by the quantising system.

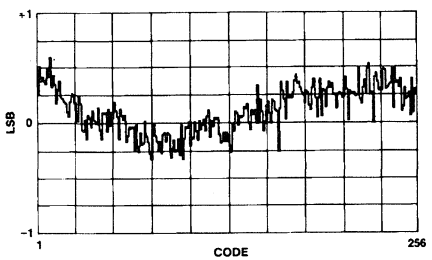


Fig. 5 Accumulation error (integral)

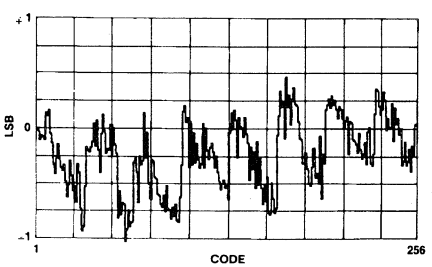


Fig. 6 Accumulation error at 30MHz

Method 4. Sinewave Curve Fit.

This test is similar again in that the data acquired by a logic analyser is processed by a desk–top computer. The computer generates theoretically perfect sinewave data, from which the actual ADC information, contained in the logic analyser, is subtracted. The data for the perfect ADC is produced by curve fitting: the Least Squares method is usually used to minimise the error between the actual and theoretical data. A theoretically perfect digitised sinewave which has exactly the same amplitude, frequency and phase as the actual data is required. The remaining difference between these groups of data now represents not only differential and integral linearity but also noise and aperture uncertainty effects. The disadvantages of the method are that (a) the programming must be very precise, (b) DC offset errors are ignored.

Method 5. Fast Fourier Transform

The fast Fourier transform (FFT) is simply a numerical method for conversion from the time domain to frequency domain. The method is based on the fact that any waveform can be constructed from a number of discrete pure sinewaves of different frequencies and amplitudes.These frequencies can then be plotted to give the spectrum of the signal.

Two methods are used for acquiring the data. The first and most popular, as in the previous methods uses a logic analyser, which transfers the data to a desk–top computer for FFT calculations. The second method (usually using a waveform analyser) uses a DAC to reconstruct the data which is digitised and sent to the computer for FFT. The spectral information from this method contains DAC distortions within the results. This can be an advantage if a complete system is to be analysed.

The FFT contains not only linearity information but also other errors that deteriorate the signal–to–noise ratio. Linearity errors cause sidebands to be produced in the frequency domain and so measurement and analysis of the system can be performed in great detail.

The disadvantages of the FFT method are (a) it is important to choose the input frequency to avoid coincidence between the fundamental and harmonics reflected back into the baseband by the sampling technique, (b) the input signal has to be exceptionally pure with very low harmonic content.

Choice of Tests

To form a good general assessment of a high speed ADC it is necessary to perform the DAC reconstruction tests as they not only show any gross problems with minimal effort, but also give a clear picture of any gross problems with the analog bandwidth and slewing performance of the ADC.

For an evaluation and experimentation system the accumulation methods give a clear picture of performance but for a test system the sinewave curve fit or FFT methods test a wider range of parameters.

OTHER TEST AND CONSIDERATIONS

Aperture Uncertainty

Aperture uncertainty refers to the amount of jitter at the instant the sample is taken. In other words the time taken between one sample point and the next may not be exactly the same in the following cycle. This uncertainty is usually in the order of picoseconds and so measurement is incredibly difficult. Aperture uncertainty is also found within the comparator section of the ADC. The aperture uncertainty will be increased if the comparators take slightly differing times to respond to the sample request. The results from techniques using stationary sampling are probably more than 20% inaccurate at high frequency. The effects of aperture uncertainty can also be masked by the phase jitter on the clock signal used for the ADC.

Metastable States

This exotic term is used when discussing missing or random data errors. There is a finite probability that when a comparator is latched it is at balance. This in fact would be a very rare event, as noise and hysteresis would tend to trip the comparator within the time it is being latched. Nevertheless figures as high as 1 missing sample in 10^9 have been quoted.

A balanced comparator would in fact cause an error within the decode ROM and in many ADCs that causes an all '0's output code for that sample.

Mountain Climb Effect

The 'mountains' here are are in fact the spikes produced by the fast edges of the clock. If they are not adequately removed from the reference chain and analog input an interesting effect occurs: as the clock edge speed is increased the reconstructed output will show a DC shift, sometimes above one LSB. This is due to the sample being taken at exactly the same time as the sample edge disturbs the input signal. The result is a 'DC' shift because they will always remain in phase. Good layout using split grounds and good decoupling will minimise this problem.

Data Valid Time

This is an important and frequently ignored parameter. It is simply the proportion of time that the output data is valid, expressed as a percentage of the minimum clock period. If the ADC has a maximum frequency of 100MHz i.e. a minimum period of 10ns, a 70% data valid time indicates that the data would be valid for 7ns and could be acquired at any time within this period. This is important as the shorter the time, the harder it is to design the system. High cost can result if extra latches and delay lines are needed to collect the data consistently over the specified temperature range.

HIGH SPEED ADC BIT ERROR RATE MEASUREMENT

This application note describes a system which can be used to measure the number of bit errors per second produced by a high speed ADC. The technique can be used at low frequency or with full amplitude near Nyquist input conditions (50MHz).

INTRODUCTION

It has been generally assumed that the only way to make accurate ADC bit error rate measurement is to use a very large high speed memory to capture vast amounts of data, then a computer would be needed to sift through this data to find and count the number of bit errors. This method becomes impractical at very high data rates with today's ADCs as the size of high speed memory required to capture the data becomes too large and costly.

The measurement technique described here needs neither the computer or memory, yet it gives a readout of errors per second *in real time*. This is achieved using standard lab equipment.

BASIC THEORY OF THE TECHNIQUE

Before examining this system at near Nyquist input frequency the explanation can be simplified by first describing a low input frequency system. Then it can be shown how this simple system can be modified to measure bit errors with a full amplitude near Nyquist input.

Low Speed System

If the slew rate of the input signal to the ADC under test is set to a very low frequency (say, f') it is certain that at a clock frequency of f_c at least one sample would be taken between each of the comparators within the flash ADC. The resulting reconstructed DAC output would then show all 2^N levels.

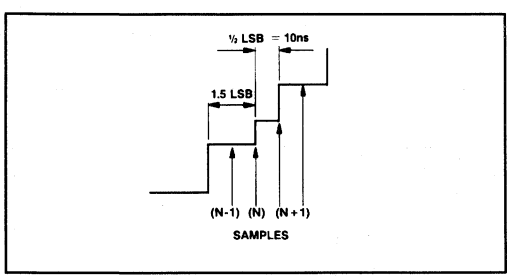


Fig. 1

If f' is calculated for a specific f_c and N (number of bits) it can be ensured that the data from the ADC will never change by more than one LSB between any two successive samples. See Fig.1.

Therefore, at the output of the ADC, (DATA N) – (DATA (N–1)) $\leq$ 1LSB.

This rule will only break down if a code error or a bit error occurs. It will be discussed later how to count the resulting error codes, but first to set up this system the value of f' must be calculated.

Calaculation of f'

From Fig 1 a general formula can be derived for f' in terms of N, f_c and the minimum differential linearity error (e_{min}).

To do this must first be calculated the maximum rate of change of voltage which gives one LSB change at the output of the ADC, each time we take a sample.

The rate of change of the input is $\frac{\Delta V}{\Delta t}$

The voltage at the input for a 1 LSB change at the output is:

$$\Delta V = V\,p - p\,\frac{1}{2^N - 1}N = \text{number of bits}$$

Now to take into account the minimum differential linearity:

$$\Delta V = \frac{V\,p - p}{2^N - 1}(e_{min})$$

Δt is simply $\frac{1}{f_c}$ ie . one clock cycle

$$\text{Therefore } \frac{\Delta V}{\Delta t} = \frac{\frac{Vp - p}{2^N - 1}(e_{min})}{\frac{1}{f_c}} \frac{Vp - p\,f_c\,(e_{min})}{2^N - 1} \qquad ...(1)$$

It is now possible to calculate the sinusoidal input frequency f' which gives this maximum rate of change of input voltage.

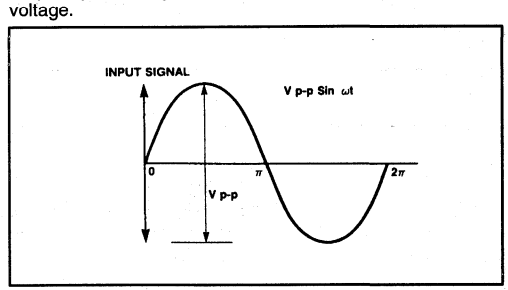


Fig. 2

The maximum rate of change of a sinewave is when ωt = 0, π or 2π

$$\text{ie . when } \frac{dV}{dt}(Vp - p\ sin\ \omega t) = o, \pi\ or\ 2\pi$$

$$\text{Now} \frac{dV}{dt} Vp - p\ sin\ \omega t = Vp - p\ \omega\ cos\ \omega t$$

Therefore as $|\cos \omega t| = 1$ for ωt = 0, π or 2π, the maximum rate of change must be given by:

Vp–p ω x 1

Therefore $\frac{dV}{dt}\ max = Vp - p\ 2\pi f$ ...(2)

Hence, when $\frac{dV}{dt}\ max = \frac{\Delta V}{\Delta f}$

The required conditions are satisified. ie. when equation (1) = equation (2).

$$\frac{Vp - p\ f_c\ (e_{min})}{2^N - 1} \quad Vp - p\ 2\pi f$$

Cancelling Vp–p and rearranging for f' gives:

$$f' = \frac{f_c(e_{min})}{2\pi(2^N - 1)} \qquad ...(3)$$

As we now have a general formula for the maximum input frequency at which the ADC outputs only change by 1 LSB we can calculate f' for our 100Mhz 8–bit device (e_{min}) = ½ LSB.

$$f' = \frac{100MHz\ 0.5\ LSB}{2\pi(2^8 - 1)}$$

$$\text{Therefore } f' = \frac{100MHz\ 0.5}{1602}$$

f' = 31.2kHz

The analog input must therefore be set to less than 31.2kHz to ensure that the output code only changes by 1 LSB or less between each sample. A safety factor can be applied to this frequency but we must not go too low as we need to measure errors on as many levels as possible within each second (20kHz is a suitable low frequency).

COUNTING THE BIT ERRORS

Before proceeding with any bit error measurement we must first make sure that the device is not producing code errors.

This is easily done by viewing the reconstructed 20kHz sinewave output on a scope. As code errors occur on every cycle they are easily visible on an 8–bit device.

As stated previously, a bit error has occurred if the difference between any two adjacent codes is greater than I LSB. We can therefore detect the occurrence of any bit error by subtracting data (N–1) from data N and then looking for a result greater than one.

This system delays the 8 bits output by one clock cycle and then sums this with the complement of the original data, thus producing the difference between data N and data N–1. If the LSB is ignored the resulting 7 bits should remain at zero unless a bit error occurs. Bit errors are detected by the OR gate. These pulses can then be counted using a frequency counter yielding a result in errors per second.

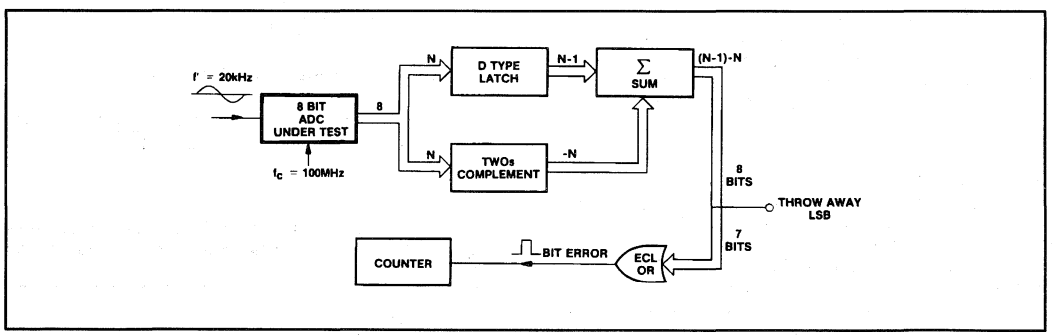


Fig. 3

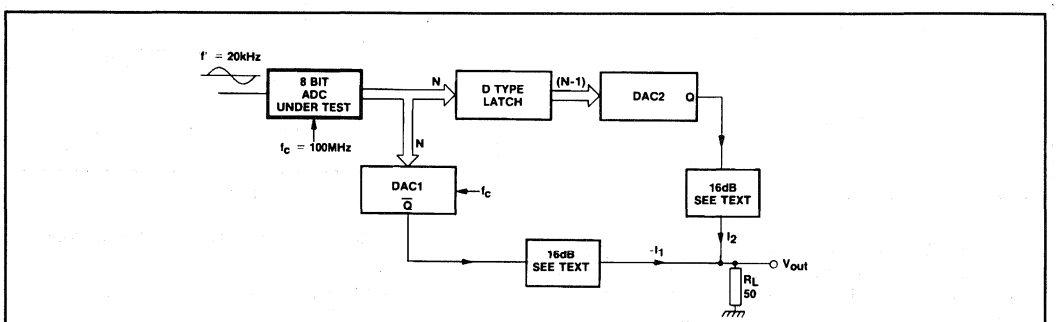
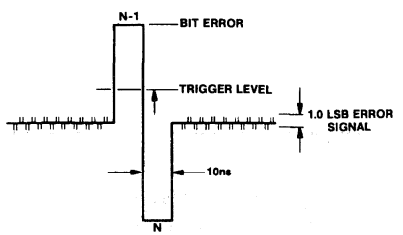


Fig. 4

Analog Technique

This analog technique is an alternative to the digital subtraction method. Digital subtraction can be very difficult at 100MHz and above. (However it can be ideally suited to production testing). The analog technique now described takes advantage of the very high speed latched DACs now available. These 200MHz or 400MHz DACs can be used to reconstruct the data. The subtraction can than be performed very simply by summing the true and inverse analog DAC output currents into a 50Ω load (Fig 4).

V_{out} will be a small error voltage signal 1 LSB high, unless of course a bit error,occurs in which case a pulse is produced with an amplitude proportional to the erroneous code the error has caused. The pulse will also be seen on the next cycle of the clock, due to the one cycle delay in the latch. On this second cycle a negative going voltage will be seen.



NOTE: This waveform can only be seen on a non storage scope with full intensity on the scope and a very bad ADC in circuit, as it may only trigger the scope 1–200 times per second.

Fig.5

Counting these bit errors is very simple as most scopes produce a trigger output signal from the rear panel. This can be connected directly to a counter. The scope trigger level can be adjusted so that the normal 1 LSB error is ignored. The scope trigger must be set to DC and normal with the time base at about 100ns/div.

The system can be calibrated to look for bit errors greater than a chosen number of bits. This is done by switching off the LSBs of DAC1 to produce the error amplitude above which bit errors are to be counted. The scope trigger is then set so that triggering is just lost. The LSBs can then be reintroduced into DAC 1 and the errors counted on the counter as above. This technique is most useful when small code errors are present as these need to be ignored to measure the remaining bit errors.

Attenuators

These are placed in the path of the current flowing to the summation resistor, and provide a cleaner signal on the scope. This is due to the fact that most current output DACs are very capacitance sensitive. The attenuators reduce the amount of scope input capacitance seen by the DAC outputs. The settling times of the DACs are therefore much improved.

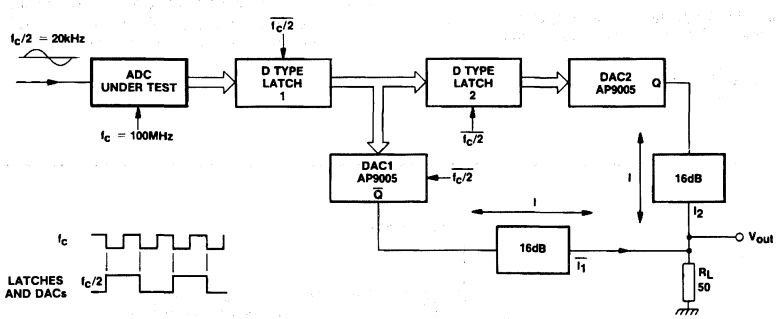
HIGH SPEED INPUT BIT ERROR MEASUREMENTS

Measurement of Bit Error with Full Amplitude near Nyquist Input Signals

The bit error rate of an ADC is not only dependant on the clock mark–to–space ratio and temperature, but also on the frequency of the analog input, and of course the input amplitude.

The definitive test for bit errors within an ADC would therefore be with a full amplitude near Nyquist input signal at maximum ambient temperature and 1:1 clock mark–to–space ratio.

This measurement can be achieved by adding a simple D type latch (Clocked at $f_c/2$) to the output of the ADC and again we can follow the previous analog measurement technique to measure the bit error rate, under high frequency input conditions.



The length of cable from each DAC to the load should be adjusted for minimum glitches on V_{out}.

Fig.6

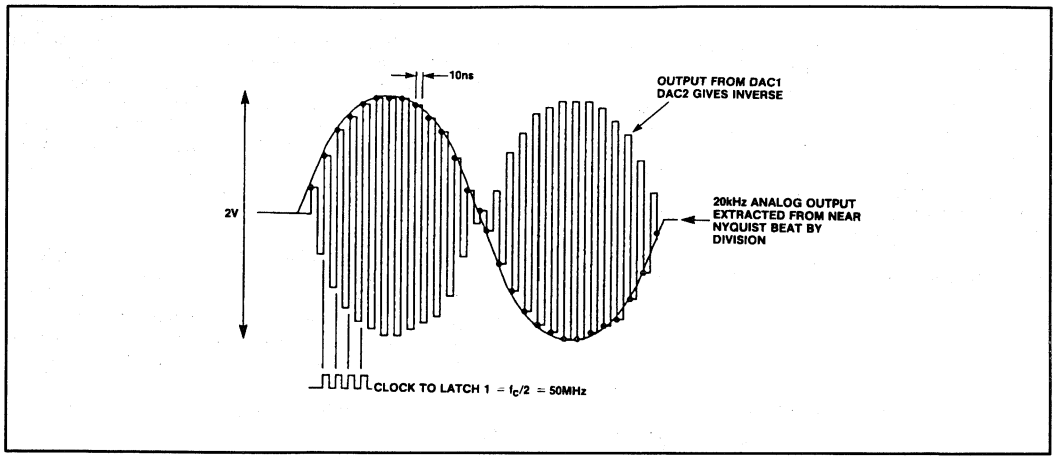


Fig.6

D type latch 1 will now divide the output data. This means that every other data word is discarded. The reason for doing what seems to be a waste of good output information is to extract the envelope from Nyquist beat pattern (see Fig. 7)

If the analog input to this system is set correctly (f'a) we can again be confident that even though the input frequency is at near Nyquist, there will be only one LSB change at the output of the ADC, but this time on every other clock cycle.

The analog input frequency must be within f' of nyquist

$$f'a = \frac{f_c}{2} \pm f'$$

In general the lower of the two resulting frequencies is chosen

$$f'a = \frac{f_c}{2} - f'$$

The general expression for the near Nyquist input frequency that will produce only one LSB change every clock cycle is:

$$f'a = \frac{f_c}{2} - f'$$

$$f'a = \frac{f_c}{2} - \frac{f_c(e_{min})}{2\pi\ (2^N - 1)}$$

Therefore $$f'a = \frac{f_c}{2}\ 1 - \frac{(e_{min})}{\pi\ (2^N - 1)} \qquad ...(4)$$

Where: f_c = *clock frequency*
N = *number of bits*
f'_a = *analog input frequency*
(e_{min}) = *minimum differential error*

We can now determine this input frequency for the 100MHz 8–bit device.

$$f'a = \frac{100MHz}{2}\ 1 - \frac{0\ .\ 5}{\pi\ (2^8 - 1)} = 49\ .\ 9687MHz$$

The two analog waveforms from each DAC are summed in R_L to produce the small 1 LSB error signal as before. The only difference between this and the low speed test is that due to the fact that the ADC output was divided by 2. The displayed error count must now be multiplied by 2.

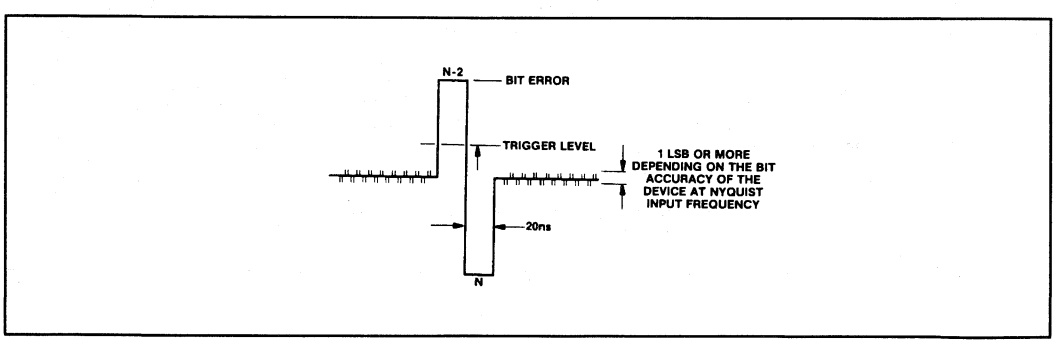


Fig.8

It is wise to add a small safety margin to this input frequency, as some lesser products will show significant deterioration of accuracy with input frequency. A frequency of 49.98MHz is a good standard for tests on 100MHz ADCs.

The results from the counter (connected to the trigger outputs of the scope) will be in counts per second. As the total number of operations per second is 10^8 (f_c = 100MHz) a result of 4 counts per second would be equal to 4 x 2 in 10^8 ie. 8 in 10^8 bit errors.

It is possible when using the high speed technique to simply switch the analog input from 49.98MHz to 20kHz to find the low frequency error rate (don not forget to multiply the result by x 2 if the division is not removed).

The system timing allows both the data capture time and mark space ratio to be adjusted without affecting the measurement technique. These adjustments can be made to the system by connecting the HP8640 (used as a master oscillator) to a HP8082 pulse generator. The HP8640 also drives the divide by 2 circuit. The pulse generator (HP8082) drives the clock of the ADC via a fast comparator.

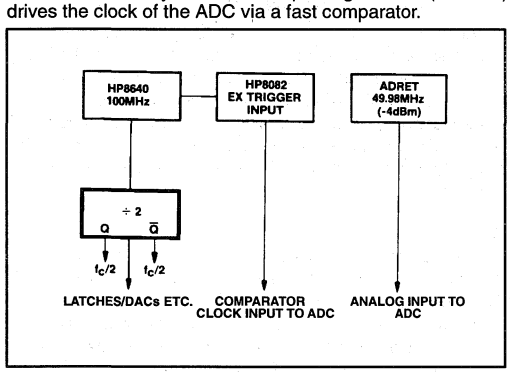


Fig. 9

EQUIPMENT AND SETTINGS FOR FULL NYQUIST BEAT BIT ERROR RATE TEST

HP8640 or equivalent (master system clock) +10dBm, 100.000MHz, AM = off, FM = off, RF = on.

HP8082 (clock conditioning for ADC, driven from 8640)

Ext trig, slope/polarity = pos, rate = 100m 10m

◄ knob position

Pulse delay = 2n – 5n, Pulse width = 5n – 50n

Trans time = 1n – 5n, Amplitude (into 50Ω) =1.0–2.0 both, vernier =, offset = on, use output (right)

neg pos = pos, normal = compl.

ADRET or equivalent (analog input to ADC. Another HP8640 could be used). 49.98MHz, –4.98MHz, 4dBm (adjust to full amplitude reconstructed output)

Counter (to count triggers ie. bit errors from external trigger out of scope). Philips M6671 was used with all buttons out apart from power.

Measuring time = 1 second, hold off = 0, set to freq A, use A input, trigger (Pushed in)

Scope (any 300MHz scope with trigger out), 5mV/DIV. AC coupled (full BW), trig = normal DC –ve slope time base 100ns/div.

Power Supplies

+5V at 220mA, –5.2V at 1.52A, +12V at 108mA.

Attenuator

Two 50Ω attenuators set to 16dB.

CONCLUDING REMARKS

We have shown that an accurate and consistent measurement of bit errors can be achieved using general lab equipment, two latches and a little ingenuity. This technique can be used even when the ADC is performing under the most severe input and clock conditions.

The major advantage of this method is that the result from the counter is in real time. Therefore it is much easier to see the effects of small parametric changes to the setup of the ADC on the bit error rate result. This allows easy optimisation of all the critical factors which effect the bit error rate within a system.

Measurements have been performed on standard products versus competitive products to optimise GPS data conversion products for the lowest bit errors. In general, GPS products have performed better than the competitive products at high analog input frequency and voltage. This is simply due to the higher input analog bandwidth of these devices. This extra speed yields comparators that can regenerate their full output drive quickly. This in turn greatly reduces the probability of metastable states, and therefore reduces the bit error rate, under all conditions. When the mark–to–space ratio is adjusted to give a longer period for the input comparators to regenerate a full output, the bit error rate from the ADC is improved still further, in all devices evaluated so far. The optimum mark–to–space ratio was found to be 7ns – 3ns.

We realise the effects of bit errors on systems such as digitised scopes, multi quadrant transmission systems, radar systems, video printers etc. It is hoped that this application note will provide a quick and effective method, for the evaluation and comparison of this important device parameter.

SP973T8 - An 8-Bit Wideband Flash ADC with TTL Outputs

AN72-2.2

This Application Note covers both general ADC system Design and practical circuit ideas to support the SP973T8 30MHz Flash TTL ADC.

DYNAMIC RANGE

The dynamic range of any flash ADC can be calculated very simply. As each extra bit causes a doubling of the number of comparators used in the device input, this in turn causes a two to one improvement in the dynamic range of the device. A two to one improvement is 6dB, so if we multiply the number of bits by 6, we get the approximate dynamic range of the device in decibels.

This can be further refined by taking into account the shape of the remaining quantisation noise produced by the ADC. Theoretically this gives a constant 1.8dB improvement above the 6 x N figure. However in any practical system we would have a variation in the amplitude of the quantisation noise, caused by the differential linearity error within the ADC. Therefore an ADC with an accuracy of $\pm\ ^1/_2$ LSB will not have the full 1.8 dB advantage. It can be shown that tor a $\pm\ ^1/_2$ LSB device an improvement of about 1.2 dB is seen.

Hence, for an ADC with N bits and $\pm\ ^1/_2$ LSB accuracy, the theoretical maximum dynamic range is given by:-

6 x N + 1.2. For an 8- Bit device we have: 49.2dB

The Bit accuracy of many ADCs falls sharply with increasing analog input frequency; all GEC Plessey Semiconductors' standard products are tested dynamically to avoid such problems.

ANALOG INPUT

The SP973T8 is a high speed flash ADC with a wideband input. Therefore the input circuitry is guaranteed not to slew rate limit at high input frequency. This is very important when digitising pulses or when high accuracy is required, up to the Nyquist frequency limit.

The Nyquist limit is simply one half of the clock frequency, and if any signal is applied to the ADC input above this limit it will be reflected, by the clock, back into the passband of the ADC. This effect is called *aliasing.*

In many systems anti-aliasing filters are required to prevent any high level inputs above fc /2.

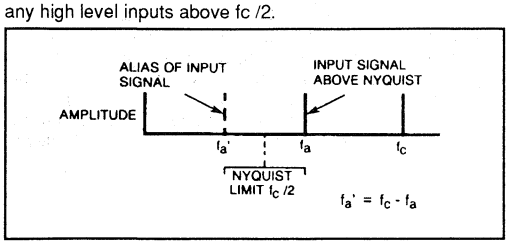


Fig.1

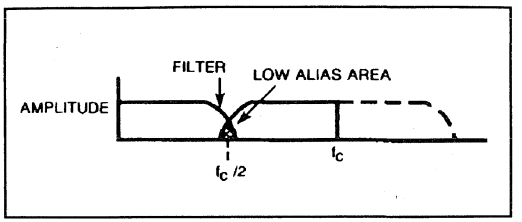


Fig.2

With many video ADCs on the market the analog bandwidth of the input stage will produce slight distortion, and hence produce intermodulation products which can be above the Nyquist frequency limit. With these ADCs restricting the analog input bandwidths is largely ineffective, as it is the ADC itself which causes signals above Nyquist to be generated.

These distortion effects would be difficult to determine from the specification of the device, as they are difficult to test in production. To make matters even worse, sometimes when specifing signal to noise of a device the alias signals are ignored.

Bit Accuracy

One parameter sometimes specified by manufacturers, which will show the true bandwidth and quality of an ADC, is Bit Accuracy. For any ADC to maintain + 1 LSB at near Nyquist frequency requires an input stage with excellent bandwidth and very low distortion. (see 'near Nyquist beat' test in Application Note AN56; for further information)

To achieve this within the SP973T8 an input bandwidth of over 80MHz was required; this maintains virtually ideal characteristics within a 10MHz input bandwidth.

The high f_T (7GHz) of WS process has made high input bandwidths possibb on a device with similar and in most cases lower power consumption than competitive products.

DRIVING THE INPUT CAPACITANCE

Not only is it important to have low distortion within the ADC but also the circuit driving the ADC must show equivalent wideband performance.

High speed flash 8-Bit ADCs have 255 comparators all connected to the input. The SP973T8 is no exception, and hence it has an input capacitance of about 40pF. This capacitance is slightly voltage-dependent and therefore it is important to provide a good quality low impedance drive for the SP973T8.

GEC Plessey Semiconductors provides an op-amp with the required performance: the SL541.

SL541

The SL541 is a bipolar device with high slew rate and excellent pulse handling, plus very good overload performance. The device has been used by many manufacturers as the op-amp driver in ADC systems.

One reason for this is the provision for adjustable open loop gain. The open loop gain can be reduced by a single resistor for stable operation at closed loop gain as low as unity.

The SP973T8 input requires a high current drive at high frequency. Therefore it is advised that one of the GEC Plessey Semiconductors range of high performance transistors is used within the op-amp feedback loop (2N3904 or equivalent).

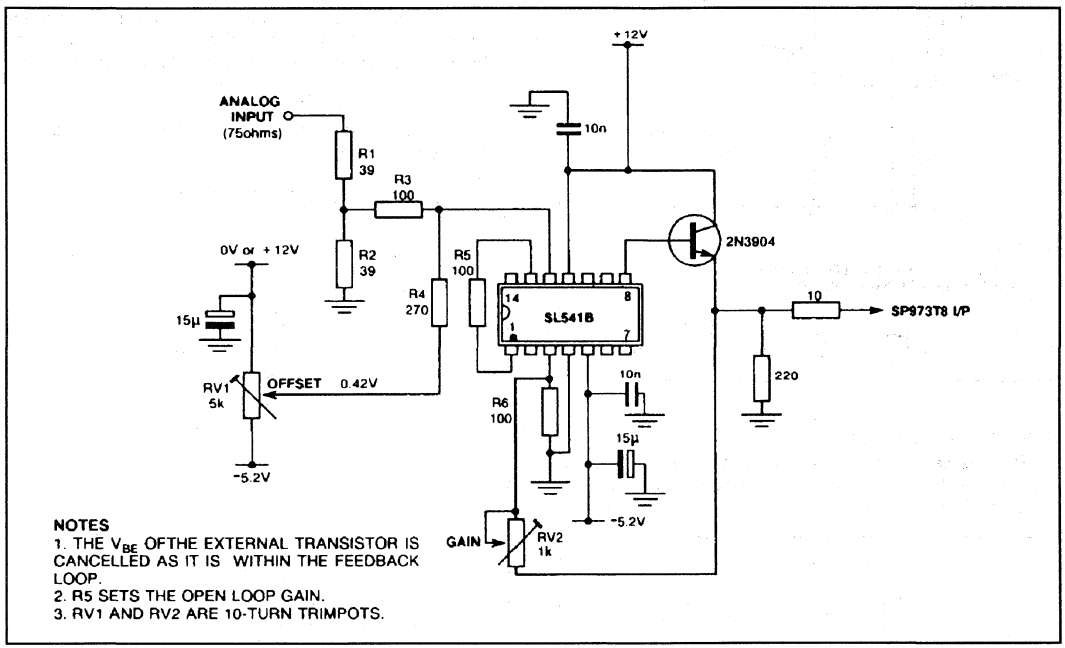


Fig.3

OTHER ADC DRIVERS

Another device of interest for ADC input driving is the SL6140 400MHz Wideband Amplifier. Although this device may not have the current drive required for precision at high speed, its AGC capabilities can be very useful in wide dynamic range applications. The SL6140 has current sourced outputs which require pull-up resistors. See also the ZN428 DAC for AGC input control from a microprocessor.

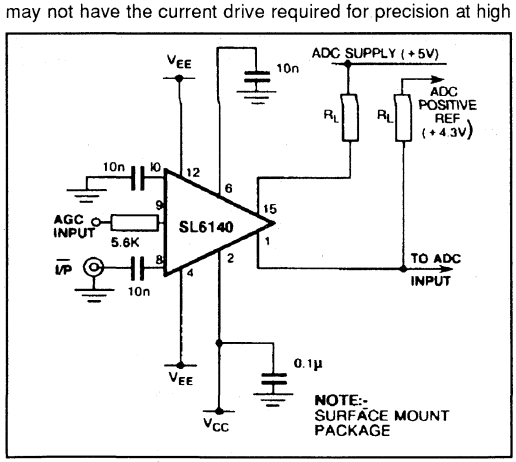


Fig.4

CLOCK INPUT

The SP973T8 is specified as a 30MHz ADC. However, the typical production device will perform adequately at clock frequencies of over 50MHz with an input of up to 10MHz.

Unlike many ADCs the SP973T8 has an internal clock amplifier and buffer. This amplifier has been introduced to avoid one of the most difficult problems when using an ADC in a system design: clock pickup. A fixed frequency at up to 30MHz with TTL type levels, would cause crosstalk resulting in reduced performance (patterning on video signals, etc.)

The clock input has been designed so that both differential or single ended drive can be used at low voltage levels. Pins 5 and 6 can be used differentially and will accept standard ECL. For single ended operation pin 6 can be decoupled to ground, and pin 5 driven with a 1Vpeak to peak signal. Pin 6 will then bias to +3.8V and can then be used to bias pin 5 through a resistor for AC coupled clock applications. See Fig 5.

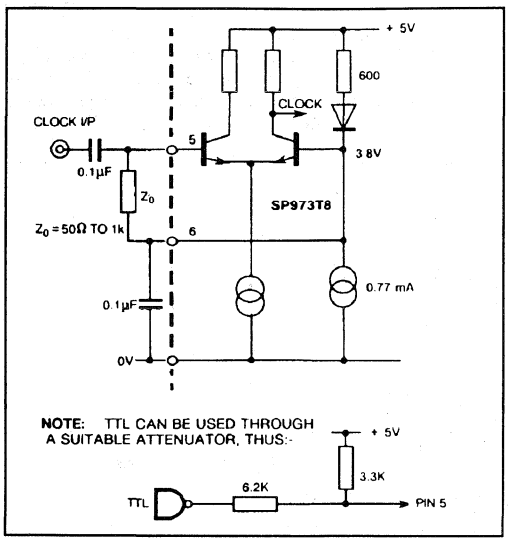


Fig.5

REFERENCE VOLTAGES

The internal reference chain requires two DC voltages applied to the top and bottom of the internal resistor ladder, as shown in Fig 6.

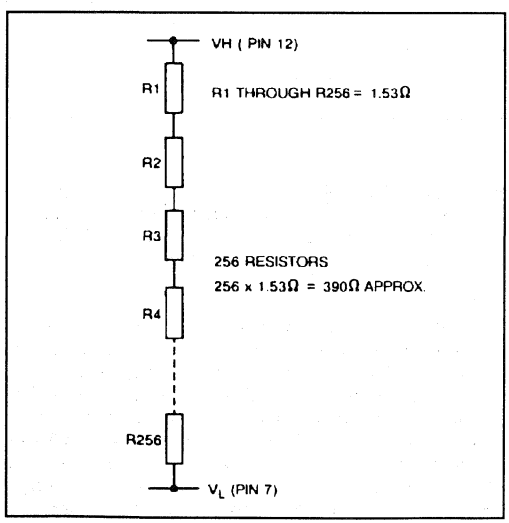


Fig.6

The best differential linearity from any flash ADC is achieved when the maximum reference voltage is applied to the reference chain. This is because the offset voltages of each internal comparator will remain constant, so increasing the reference voltage will improve the ratio of Bit size to offset voltage and hence improve the overall accuracy. For the SP973T8:

VH Max = + 4.5V

VL Min = + 1.9V

Therefore the recommended values for VH and VL are

VH = + 4.3V

VL = + 2.3V

The tolerance on the reference chain's absolute resistance is about + 25% from batch to batch, therefore the current taken by the reference chain for worst case conditions is approximately

$$\frac{2V}{390\text{-}0.25\text{x}390} = 6.8\text{mA}$$

Using a reasonable safety factor 8mA worst case current should be catered for.

SETTING THE REFERENCE VOLTAGES

Method 1

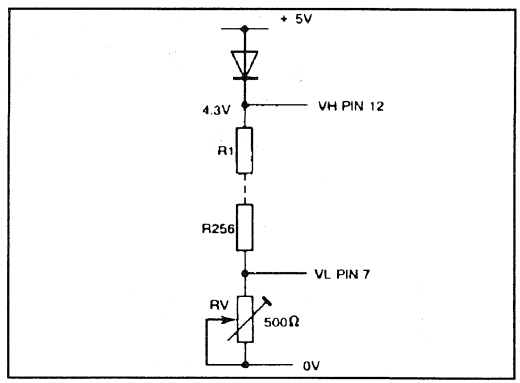


Fig.7

This is the simplest and least precise method. RV is adjusted to maximum resistance then when power is applied RV is decreased until VL = 2.3V.The diode will set VH to approximately 4.3V. There are three main disadvantages with this method. First, setup of RV is needed for each device, second, the 2mV/°C of the diode will change the VH voltage with temperature (over 100mV drift) and third, no supply line regulation is provided.

Method 2

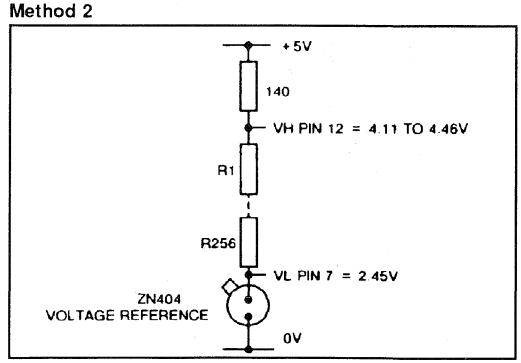


Fig.8

This method is more temperature stable than method 1 and requires no setup as long as a device batch to batch tolerance on VH of 4.11 V to 4.46V can be tolerated.

Once again, no supply line regulation is provided using this method. As the differential linearity of the SP973T8 is well within the ±0.5 LSB limit, the reduced reference voltage has little or no effect (VH -VL = 1.85V)

Method 3 (precision reference voltages)

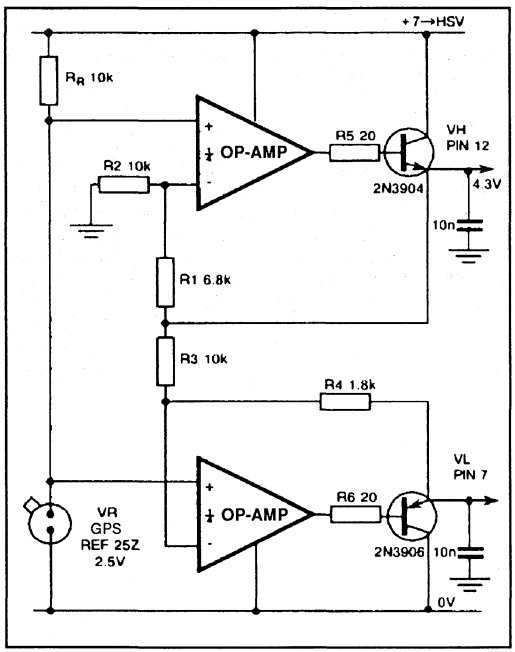


Fig.9

$$VH = \frac{(R1 + R2)}{R2} VR \quad \text{---------- (1)}$$

$$VL = \frac{VR\ (R3 + R4) - VH\ R4}{R3} \quad \text{------ (2)}$$

With R2 and R3 set to 10k. R1 can be calculated by re-arranging equation (1):

$$R1 = \frac{R2\ VH - R2}{VR}$$

R4 can be calculated by re-arranging equation (2):

$$R4 = \frac{R3\ (VR - VL)}{VH - VR}$$

This method gives excellent supply line regulation and precise voltage settings of VH and VL.

The temperature stability will also be excellent and will depend primarily on the input offset with temperature variation of the op-amps used.

The only disadvantage with this method is that a separate supply at least 2V above the ADC supply is required. This is a consequence of the output high voltage from the op-amp (we would require a + 5V output with the op-amp on a + 5V supply!)

SP973T8 OUTPUT DATA (see SP973T8 datasheet Fig. 4 for typical test load)

The output levels are TTL compatible, and switch from 0V to +4V. The output drive is capable of providing a useful output with 10pF loads at clock frequencies of over 120MHz.

The outputs are double latched which gives a very good data valid time. This means that the data can be captured any time within the clock cycle except the first 10ns (t_{pd}). The data is clocked onto the output pins by the falling edge of the clock signal. The typical system would therefore use the rising edge of the clock to capture the data into RAM or directly into a digital to analog converter (the GEC Plessey Semiconductors MV95308 is a suitable complementary DAC).

SINGLE- SHOT OPERATION

To produce a single sample of an analog input the device must be clocked twice. This is due to a one cycle delay inherent within the device.

MID- REFERENCE

This is simply the centre of the reference chain bonded out to pin 10 of the device. One ot its uses is to provide a decoupling point which aids in the removal of digital noise from the reference chain.

Another use is to trim the device integral linearity in precision measurement systems, as shown in Fig. 10.

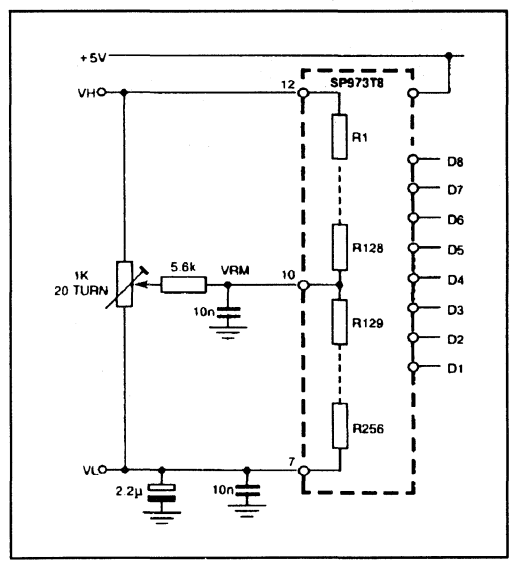


Fig.10

Another and more common use of VRM is to provide a bias input for AC coupled analog inputs, as shown in Fig. 11. Pin 10 is used to bias the analog input.

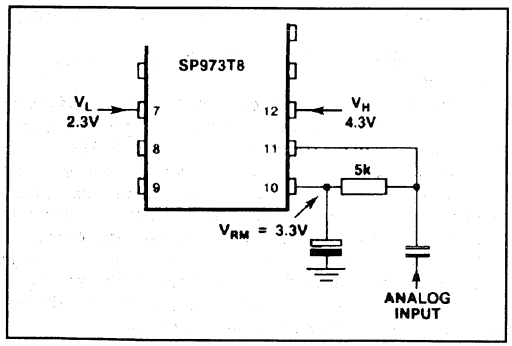


Fig.11

LAYOUT AND GROUND SYSTEM

The main objective when laying out the PCB, is to avoid clock or data edges crosstalking into the analog input or onto the ADC references. This can be achieved most effectively by the use of a split ground plane. One analog and one digital ground plane connected together at one point close to the device, is the most suitable approach.

Supply line decoupling is very important when dealing with a mix of analog and digital signals. Low inductance capacitors should be used located close to the device pins

HIGH FREOUENCY DIGITISATION

The SP973T8 is only one device in our complete range of ADCs. For example, the SP97508 8-Bit 110MHz ADC has ECL outputs and is also designed for wideband applications (refer to Application Note AN65).

SUMMARY

Finally, we hope that a clearer distinction has been made between a standard video ADC and the wideband SP973T8. Not only can a wideband device be used in quality video systems, but also in pulse measurement equipment, digital oscilloscopes, radar I and Q channel, video digitisation, nucleonics collision ionisation pulse measurements - indeed, any other system in which the performance of the equipment is defined by the quality of the ADC.

ZN425E8 8–BIT A–D/D–A CONVERTER APPLICATIONS

1. INTRODUCTION

Digital to analog, (D–A), and analog to digital (A–D), conversion is a specialised field of electronics. It is useful to consider first the general principles of such conversion techniques, and definitions commonly used in the general field of A–D and D–A conversion.

The discussion is limited to 8–bit converters of a type similar to the ZN425E8, illustrated in Fig. 1a.

Digital information, fed into the converter, normally as parallel bits, generates an analog output corresponding to the value of the binary code number entered at the input. Ignoring errors for the moment, and assuming that the analog output is a voltage, the output can be expressed as:

$$V_{out} = V_{full\ scale} \times \frac{\text{Binary input}}{\text{Full} - \text{scale binary input}}$$

which, in the case of the ZN425E8 is

$$V_{out} = V_{ref} \times \frac{\text{Binary input}}{256}$$

The voltage output is obtained using a resistive ladder network shown in Fig. 1b. Switches connect resistors within the network either to the reference voltage or to the ground line according to the state of the binary inputs controlling each particular switch.

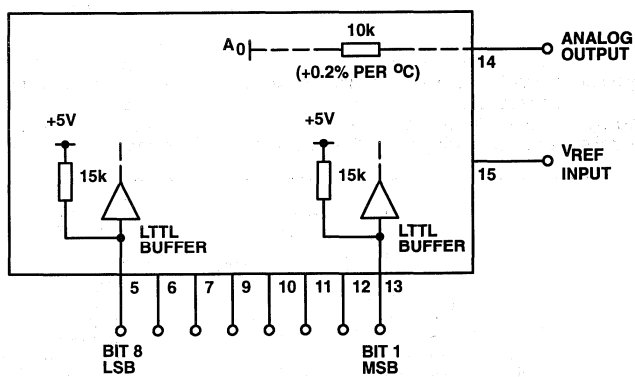


Fig. 1a Basic 8–bit D–A converter

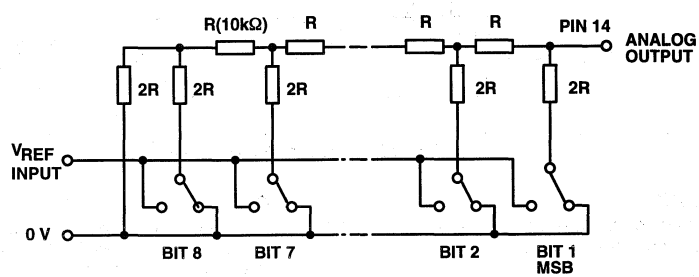


Fig. 1b The R–2R ladder network

The block diagram of the ZN425E8 circuit is reproduced in Fig.2.

The integrated circuit is fully monolothic. It contains a resistive ladder network, a logic input select switch, voltage switches, an internal reference and a counter. The D–A reference may be connected to the internally generated reference or to an external reference voltage. The inclusion of a counter within the circuit considerably extends its application. A 'staircase' waveform can be very simply generated at the analog output by feeding a train of clock pulses into the counter.

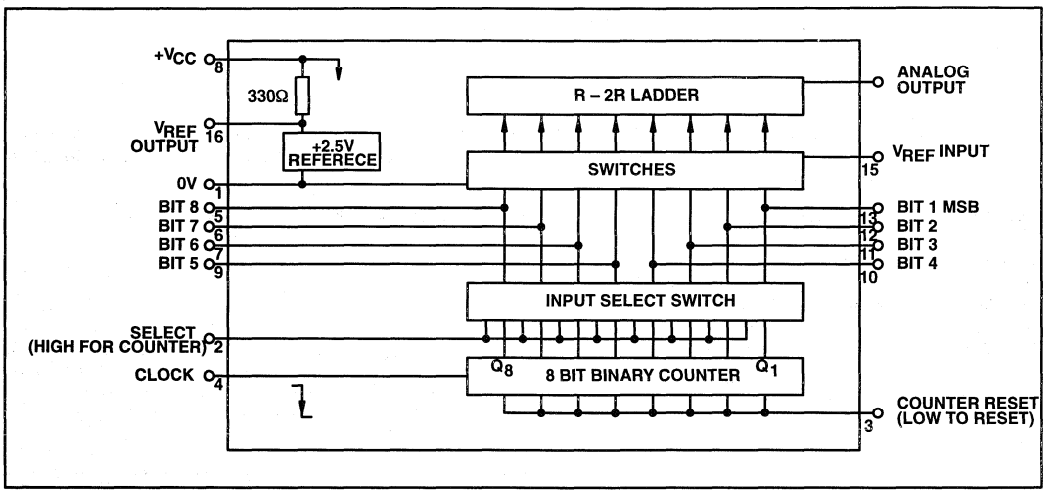


Fig. 2 Block diagram of ZN425E8

The ZN425E8 system operation is outlined in Fig. 3. The counter may be clocked by negative going inputs and reset by applying '0' level to the reset pin.

The digital inputs to the converter may be obtained either from an external source when the 'logic select' pin is at logical '0' or from the counter when it is set to logical '1'. In the latter case the state of the counter appears at the digital input terminals as '0' or '1' levels on open collectors with 15kΩ pull up resistors. In the D – A mode the digital input terminals may be considered as low power TTL inputs.

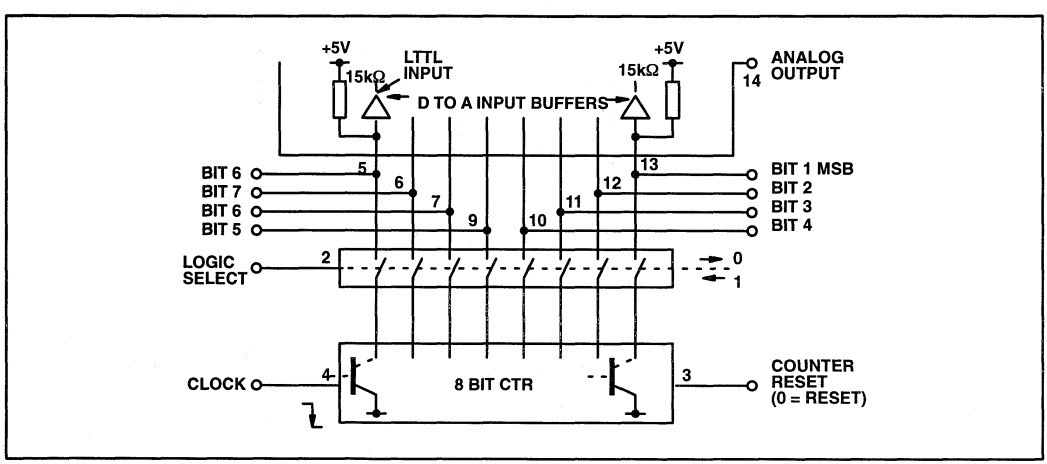


Fig. 3 Outline ZN425E8 operation

1.1 DEFINITIONS

Various terms commonly used when discussing D – A and A – D converter operation are defined below.

RESOLUTION

The resolution is determined by the number of digital inputs, i.e. an 8–bit ADC, (digital to analog converter), is said to have 8–bit resolution. No particular level of accuracy is implied.

STAIRCASE/RAMP

As the binary code is increased step by step, the analog output also increases in discrete steps. If the input code increases at a constant rate the resulting output will be staircase.

Since the number of discrete steps is normally large, e.g. 255 for 8 bits, the staircase is frequently termed a ramp, though this is not strictly accurate.

MONOTONICITY

A DAC is said to be monotonic if an increase in the applied binary coded digital number always produces an increase in the analog output. Waveforms produced by a D–A 'staircase' generator illustrated in Fig. 4a shows the effect on non monotonicity.

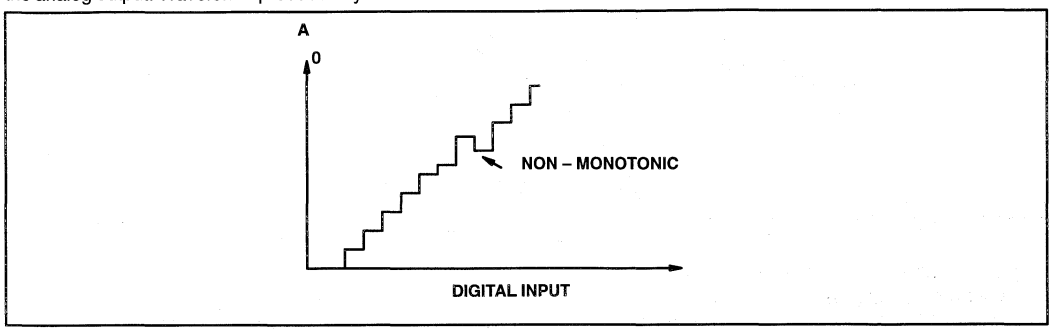


Fig. 4a Non monotonicity

IDEAL DAC OUTPUT

The ideal DAC output of a staircase generator is shown in Fig. 4b.

The output is defined as a set of points on a straight line between zero and full–scale. For an ideal 8–bit DAC.

$$V_{OUT} = \frac{n}{2^8 - 1} \times V_{FS}$$

$$= \frac{n}{255} \times V_{FS}$$

and

$$V_{FS} = \frac{255}{256} \times V_{REF\,input}$$

$$\therefore \quad V_{out} = \frac{n}{256} \times V_{REF\,input}$$

where 'n' is the number represented by the digital input.

For example

$$01101100 = 2^6+2^5+2^3+2^2 = 108$$

gives an output

$$V_{out} = \frac{108}{256} \times V_{FS}$$

$$= \frac{108}{256} \times V_{REFinput}$$

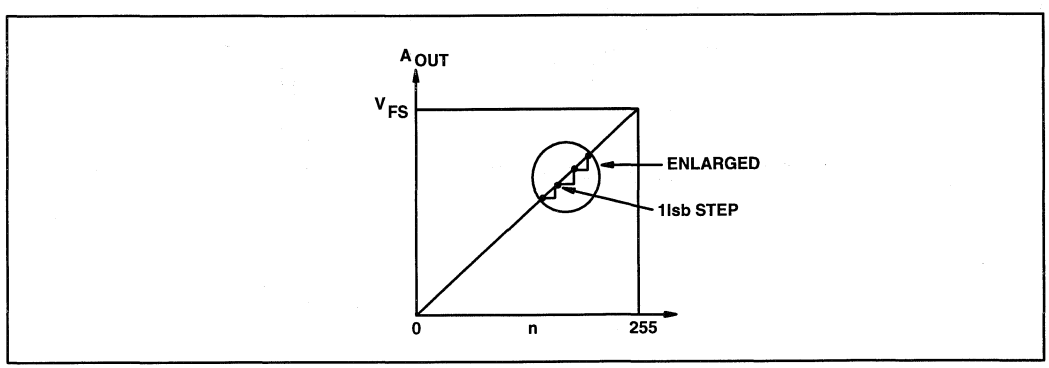


Fig. 4b Ideal DAC output

LINEARITY ERROR

A DAC may deviate from the ideal as shown in Fig. 4c. The error is usually specified as a maximum deviation of the analog output from the ideal output, as a fraction of the least significant bit'. The ZN425E8 has a linearity better than ±½ LSB, and

$$\tfrac{1}{2}LSB = \tfrac{1}{2} \times \frac{V_{FS}}{255}$$

RELATIVE ACCURACY

The error expressed as a percentage of the full scale voltage, V_{FS}, is termed the relative accuracy.

The ZN425E8, an 8–bit converter with ±½LSB linearity, has a relative accuracy

of $\frac{1}{510} \times 100\%$ i.e. approximately 0.2% accuracy

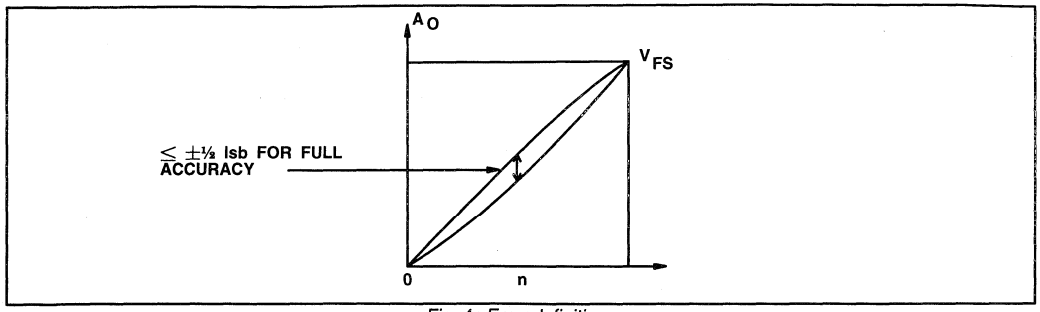


Fig. 4c Error definition

2. D–A/A–D CONVERTER SYSTEM

2.1 8–bit D–A and calibration procedure

The ZN425E8 gives an analog voltage output directly from pin 14, so that the usual current to voltage converting amplifier is not required. However, in order to buffer the resistive ladder output impedance, to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig 5 shows a typical scheme with the 741 as the buffer amplifier. The internal voltage reference source ($V_{REF\ out}$) is used, and to minimise temperature drift the source resistance to the inverting input of the buffer amplifier should be approximately 6kΩ. Calibration procedure is as follows:

(i) Set all bits to LOW and adjust R2 until V_{out} = 0.000V

(ii) Set all bits to HIGH and adjust R1 until V_{out} = nominal full–scale reading – LSB

(iii Repeat (i) and (ii)

e.g. Set F.S.R. to +3.840V –1LSB = 3.825V

$$(1LSB = \frac{3.84}{256} = 15mV)$$

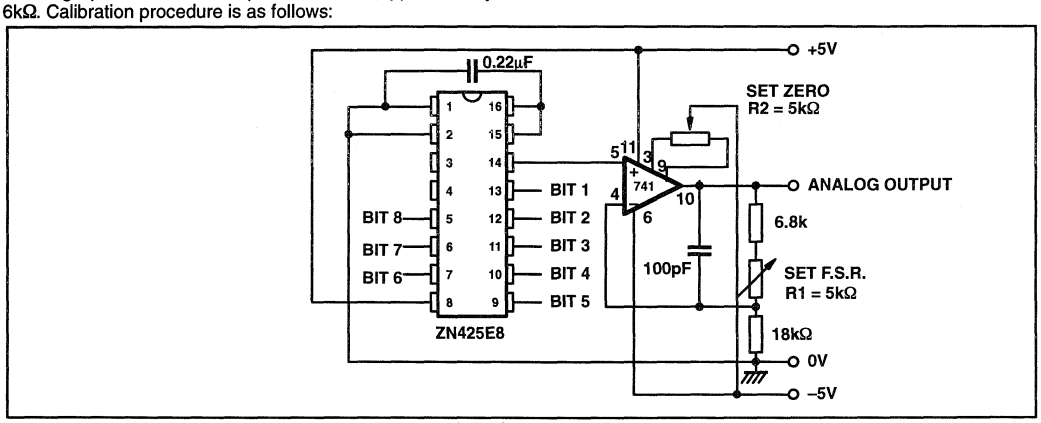


Fig. 5 8–bit DAC using 741 Op Amp

2.2 8 bit A–D and calibration procedure

Fig. 6 shows the ZN425E8 in a counter type ADC which comprises a comparator and a latch and requires an external clock. Upon application of a convert command pulse (15μs minimum) the counter is set to zero and at the same time the state of the latch is altered.

The gate is opened, enabling clock pulses to be fed to the counter input (Pin 4) of the ZN425E8. The analog output of the ZN425E8 begins to ramp up until its amplitude equals that of the analog voltage at the non–inverting input of the comparator. At this point the comparator changes state, altering the latch to its initial resting state, thus inhibiting further clock pulses. Hence the digital number stored in the respective bits of the ZN425E8 is a true representation of the analog input voltage. The diode is included so that when the comparator changes state, its output is effectively clamped at zero (LOW).

Operating clock frequencies can be as high as 400kHz. Improved results may be obtained by using narrow clock pulses to avoid the trailing edge affecting ramp settling. At frequencies above 100kHz a fast comparator should be used for optimum linearity around zero.

The conversion time is dependent upon the analog input and for full–scale reading (F.S.R.) is given by the clock period multiplied by the number of counts.

If F_{clock} = 256kHz,

$$T_{Convert} = \frac{2^8}{256x10^3} \text{Seconds} = 1\text{ms}$$

The calibration procedure is as follows:

(i) Apply continuous CONVERT COMMAND PULSES

(ii) Apply full–scale minus 1½ LSB to analog input and adjust F.S.R. pot until the converter LSB just switches between 0 and 1 with all other bits at 1.

(iii) Apply zero + ½ LSB to analog input and adjust zero pot until the converter LSB just switches between 0 and 1 with all other bits 0.

(iv) Repeat step (ii).

E.g. Full–scale = 4 volts.

$$1\text{LSB} = \frac{\text{Full} - \text{scale}}{256} = \frac{4\text{V}}{256} = 15.63\text{mV}$$

Input for zero setting =½LSB = 7.82mV
Input for full–scale setting = 4V –1½LSB = 3.97656 volts.

After conversion is complete the analog input is available from the ZN425E8 in digital and analog form and therefore the ADC may be used as a sample and hold with infinite hold time. The convert command is replaced by a sample command.

A peak detect circuit may also be constructed using similar techniques, and is described in section 3–4.

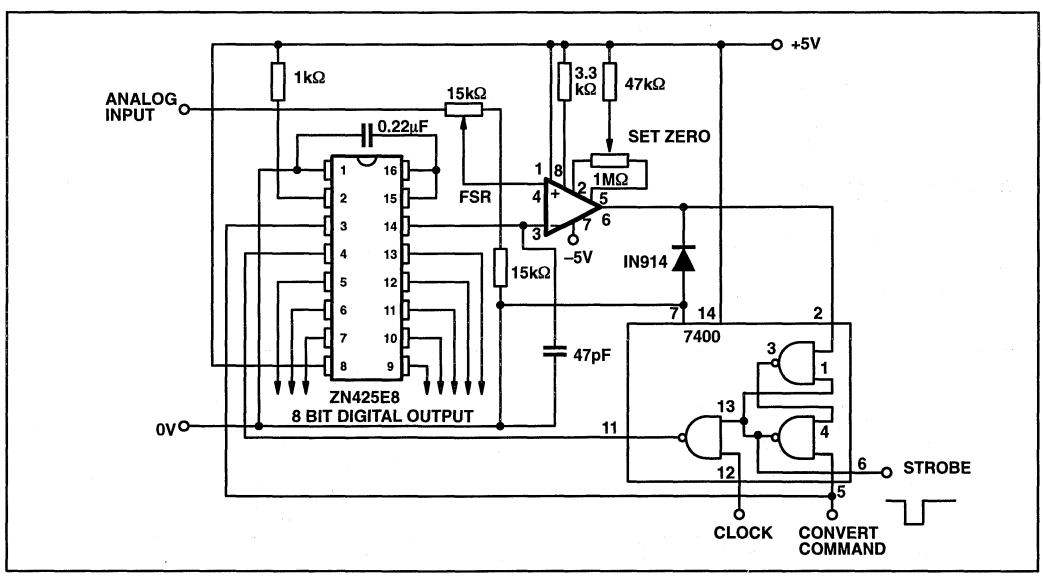


Fig. 6 8–bit A–D converter

2.3 Bipolar operation

Previous circuits described have entailed the use of a uni–polar buffer amplifier (e.g.741) following a DAC as a means of removing the offset voltage, minimising temperature drift and calibrating the DAC. A natural sequel to this is the derivation of a bipolar buffer amplifier which fulfils these conditions. This entails buffering the output of a DAC such that the amplifier output from the buffer is symmetrical about zero. To effect this, the conditions that have to be satisfied are:

(i) When the DAC output = $\frac{V_{REF}}{2}$ (digital input = 1000000) then the buffer amplifier output = zero.

(ii) Gain can be easily selected and suitable resistor values calculated. Actual gain and offset must be capable of fine adjustment.

The circuit of Fig. 7a was first devised as a possible solution.

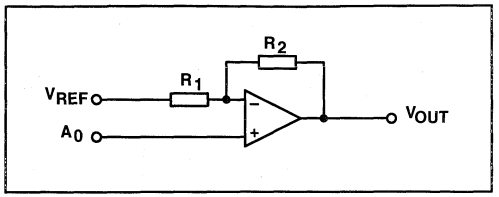


Fig. 7a Bipolar operation, starting point

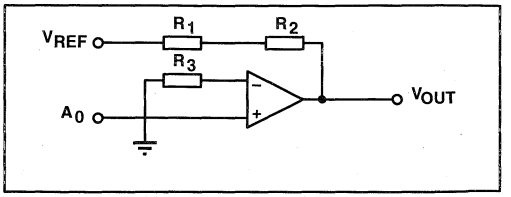


Fig. 7b Bipolar operation, concept progression

If F_N = non–inverting feedback return $= \frac{R1}{R1 + R2}$ and F_1 = inverting feedback return $= \frac{R1}{R2}$

Then V_{OUT} is given by:

$$V_{OUT} = \frac{A_O}{F_N} - \frac{V_{REF}}{F_1} A_O\left(\frac{R1 + R2}{R1}\right) - V_{REF}\frac{R2}{R1} \quad \text{equation 1}$$

$$\text{If } A_O = \frac{V_{REF}}{2} \text{ and } R1 = R2 \text{ the } V_{OUT} = 0 \quad \text{satisfying condition (i)}$$

$$= \text{However Gain } \left(\text{defined as } \frac{V_{OUT}}{A_O}\right) = \frac{R1 + R2}{R1} = 2 \quad \text{and condition (ii) would not be}$$

satisfied since adjusting R1 or R2 would upset the gain on offset. To minimise these disadvantages therefore the circuit
of Fig. 7b was devised using an additional resistance, with its Thevenin equivalent of Fig. 7c. Using equation 1 then an expression for the output voltage V_{out} can be shown as:

$$V_{OUT} = A_O\left[1 + \frac{R2(R1 + R3)}{R1\ R3}\right] - V_{REF}\frac{R2}{R1}$$

$$\text{For } A_O = \frac{V_{REF}}{2} \text{ (Condition (i)) then } V_{OUT} = O$$

$$\text{and } R1 = \frac{R2\ R3}{(R2 + R3)} \text{ i . e . } R1 = \quad \text{parallel combination of R2 and R3}$$

Substituting this expression for R1

$$\text{then Gain } G = \left[1 + \left(\frac{2R2 + R3}{R3}\right)\right] = \left[2 + \frac{2R2}{R3}\right]$$

$$\text{If we let say } R2 = \lambda R3 \text{ the } G = 2(1 + \lambda) \text{ and } \lambda = \left(\frac{G - 2}{2}\right)$$

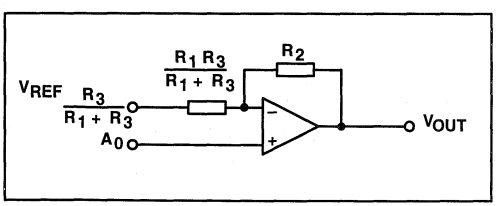


Fig. 7c Thevenin equivalent of Fig. 7b

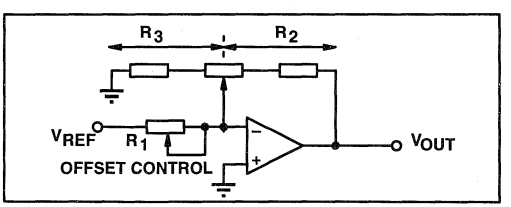


Fig. 7d Bipolar operation, control schematic

$$\text{i . e . } G \geq 2 \text{ from which } R2 = \left(\frac{G - 2}{2}\right) R3$$

$$\text{And } R1 = \left(\frac{R2\ R3}{R2 + R3}\right) = \left(\frac{\lambda}{1 + \lambda}\right) R3 = \left(\frac{G - 2}{2}\right) R3$$

Furthermore the buffer amplifier input impedance =

$$\frac{R1R2R3}{R1R2 + R2R3 + R1R3} = \left(\frac{G - 2}{2G}\right) R3$$

All the above expressions and relationships form a basis for development of the circuit of Fig. 7d whereby by defining a certain gain (G) all ressitor values can be appropriately calaculated as illustrated.

e . g . Let G = 4, then $R_{in} = \left(\frac{4-2}{8}\right) R3 = \frac{R3}{4}$

If R_{in} = 10kΩ (the value required for minimum offset taking into consideration R_{out} of ZN425E8 DAC = 10kΩ) then R3 = 40kΩ.

$$R2 = \left(\frac{G-2}{2}\right) R3 = \left(\frac{4-2}{2}\right) R3 = R3 = 40k\Omega$$

$$\text{And } R1 = \left(\frac{G-2}{G}\right) R3 = \left(\frac{4-2}{2}\right) R3 = \frac{R3}{2} = 20k\Omega$$

It has been shown that $R1 = \frac{R2R3}{R2+R3}$ The simplest approximation ensuring this relationship is by using a potentiometer as a gain control.

The finalised circuit is shown in Fig. 8

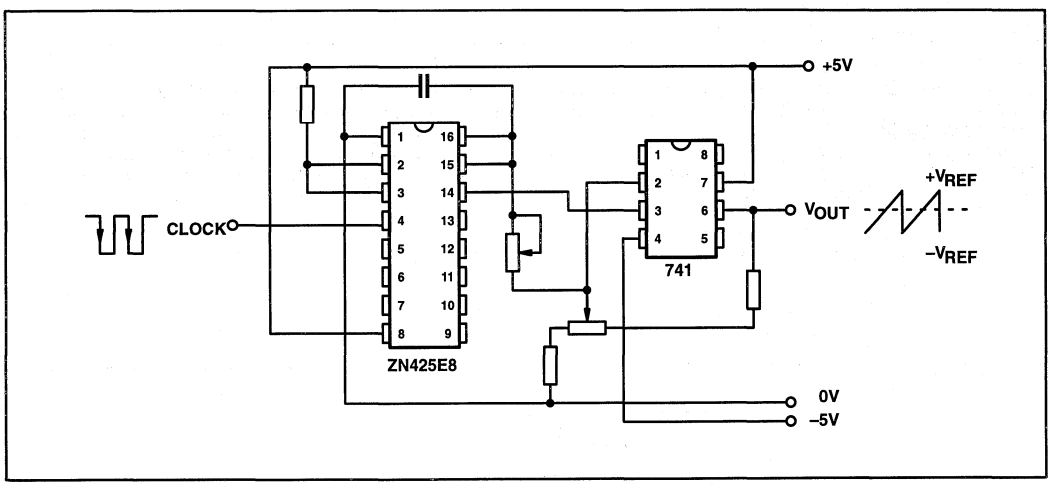


Fig. 8 Bipolar operation, circuit diagram

2.4 Applications

Applications for the use of the ZN425E8 in its D–A or A–D mode are those where 8–bit accuracy suffices. This is the majority of transducer applications particularly as system hierarchy is tending to change with the advent of microprocessors taking the conversion near to the point of measurement. For example, in data acquisition monitoring say 100 channels, it is feasible and economic to use one D–A per channel and multiplex one A–D per 8 channels using a single microprocessor.

If one reference is required to power several converters, additional source current may be provided by an external parallel resistor from supply to reference providing 1.2mA per additional converter in excess of three. In this case the additional earth pin current causes an offset due to a pin resistance of around 0.1Ω.

Specific applications of 8–bit A–D are in conjunction with stress or strain gauges, and many temperature applications. 8–bit D–A may be used for driving chart recorders, programmable power supplies and actuators.

3. Ramp generation

The counter in the ZN425E8 is very convenient for feeding in a clock to generate a staircase. This facility is used in the majority of applications detailed below.

The count rate which may be used to obtain full ramp accuracy, determined by the worst case settling time of 2μs, is 500kHz, giving a cycling time of around ½ms. However, the counters are capable of being clocked at up to 5MHz, though there will be a loss in staircase accuracy at this speed.

3.1 Continuous

This is illustrated by the circuit of Fig. 9 and is simply accomplished in the normal DAC mode by applying clock pulses to the on chip counter (pin 4) of the ZN425E8 which produces a staircase waveform. When the counter is full it returns to its empty state and counting recommences resulting in a continuous ramp.

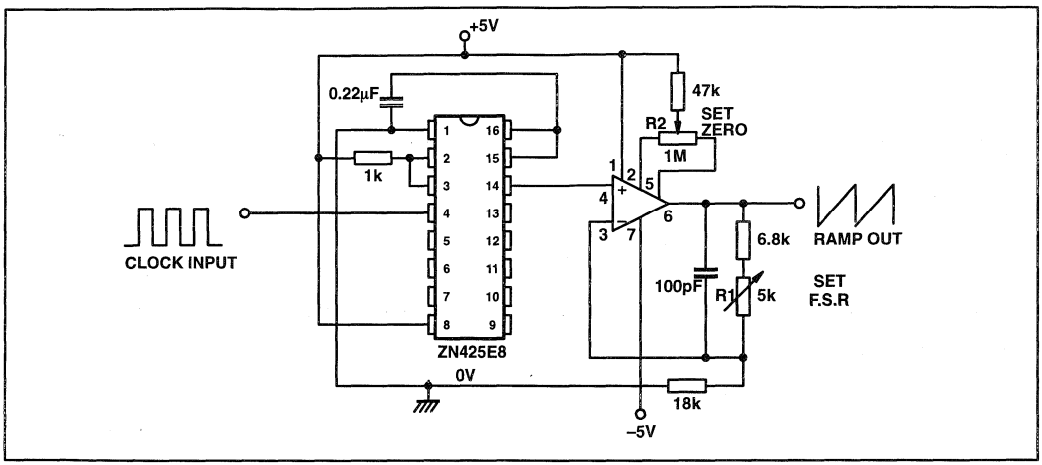


Fig. 9 Precision ramp generator

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary as previously described for the DAC.

The ramp period for 8 bits will be equal to 256 times the clock period, and the maximum amplitude of the ramp from the ZN425E8 using the internal reference voltage will be V_{REFout} −1LSB. Therefore, the peak ramp amplitude from the buffer will be this value times the amplifier gain, which with gain adjustment potentiometer set halfway is

$$2.5V \times \frac{3}{2} = 3.75V$$

A duty cycle drive signal is sometimes required from an input voltage generated by a potentiometer, for example, for actuator drives, or general power control. This may be provided as shown in Fig. 10, where the ZN425E8 provides a continuous ramp, against which the voltage reference is compared. The output from the comparator then provides the duty cycle signal directly.

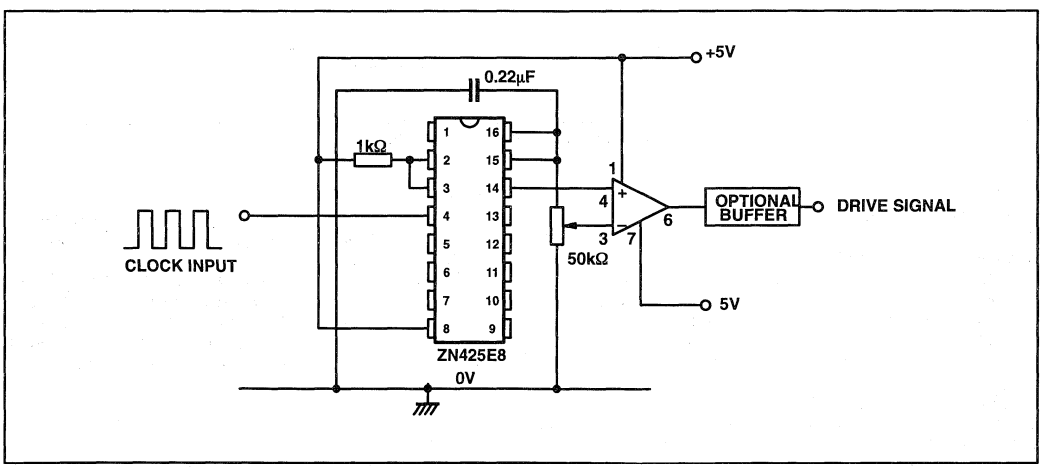


Fig. 10 Duty cycle drive signal

3.2 One shot

A single one shot ramp van be generated quite simply (Figs. 11a and 11b) by using a latch and two capacitors to control the counter reset of a ZN425E8 DAC. Operation is as follows:

The stationary states of the latch are shown, these being initially determined by the charging times of capacitors C1 and C2 which ensures the counter reset of the ZN425E8 (Pin 3) is LOW. Upon operating the START button the states of the latch are altered and HIGH is fed to the counter reset enabling counting of the input clock pulses to commence. The analog output begins to ramp up until the counter is full at which point the MSB goes LOW altering the latch to its initial resting states. This resets the counter and terminates the ramp. It should be noted that even if the start button is held down at the commencement of the operation, only a one shot ramp results, and not a periodic function.

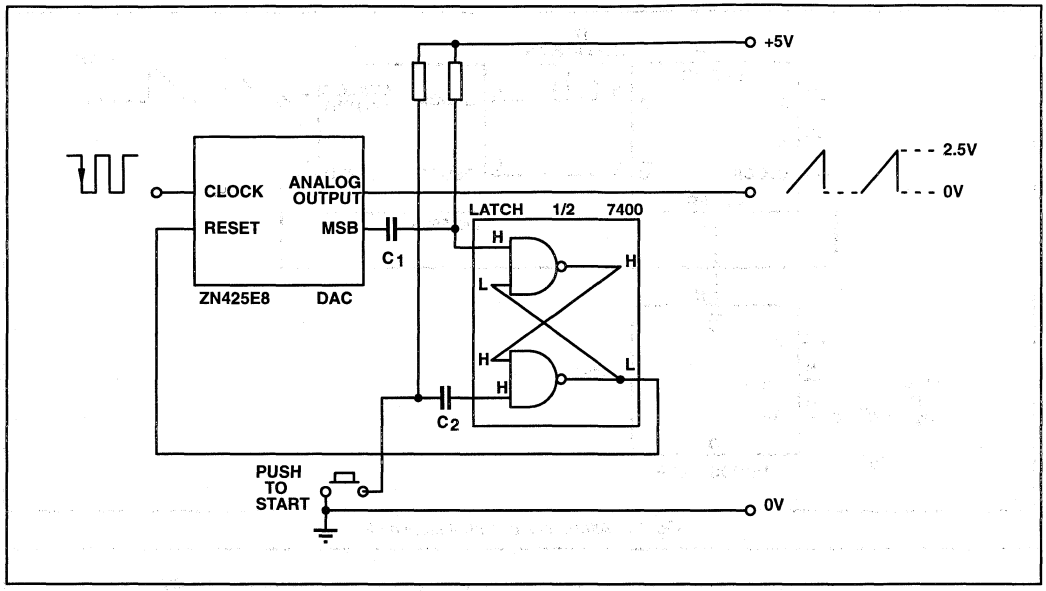


Fig. 11a One shot schematic

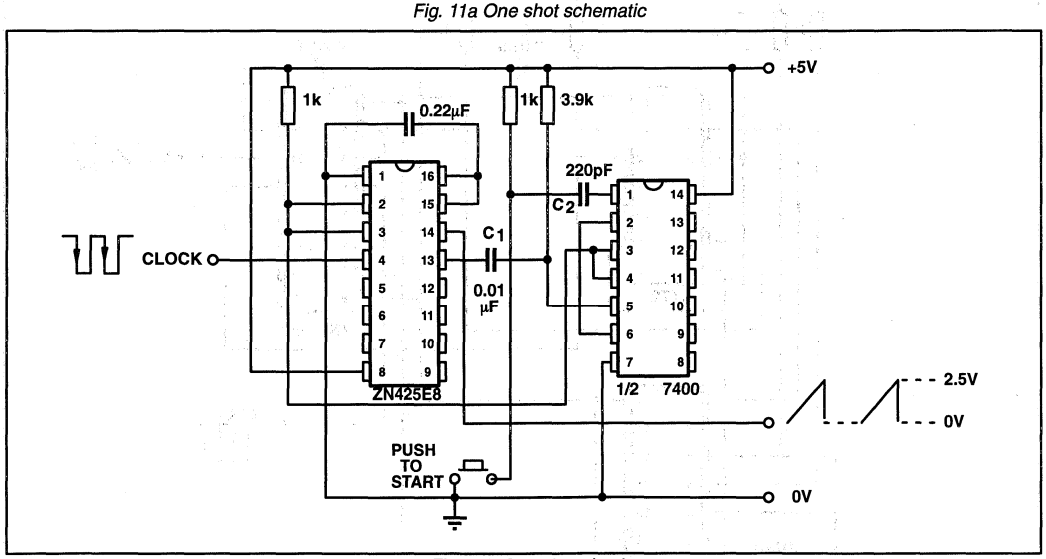


Fig. 11b One shot circuit

A more sophisticated alternative method performing the same function, which replaces capacitors by logic, is outlined in Figs, 11c and 11d. Stationary states of the various logic elements are as indicated. The initial state of the flip–flop is determined by the relative states of the PRESET and CLEAR inputs. Upon switching on the supply the PRESET is held LOW with respect to CLEAR because of the charging time associated with C1 and R1. This results in Q = HIGH, $\overline{Q}$ = LOW, therefore, the counter reset on the ZN425E8 is LOW.

When the start button is pressed, a pulse from the monostable clears the flip–flop, the counter reset goes HIGH enabling the counter of the input clock pulses to commence. The ZN425E8 analog output begins to ramp up until the counter is full, at which point the MSB goes LOW. This is fed to the CLOCK input of the flip flop which then toggles, reverting to its original state, thereby resetting the counter and terminating the ramp. As with the previous circuit only a one shot ramp will be generated even if the start button is held down.

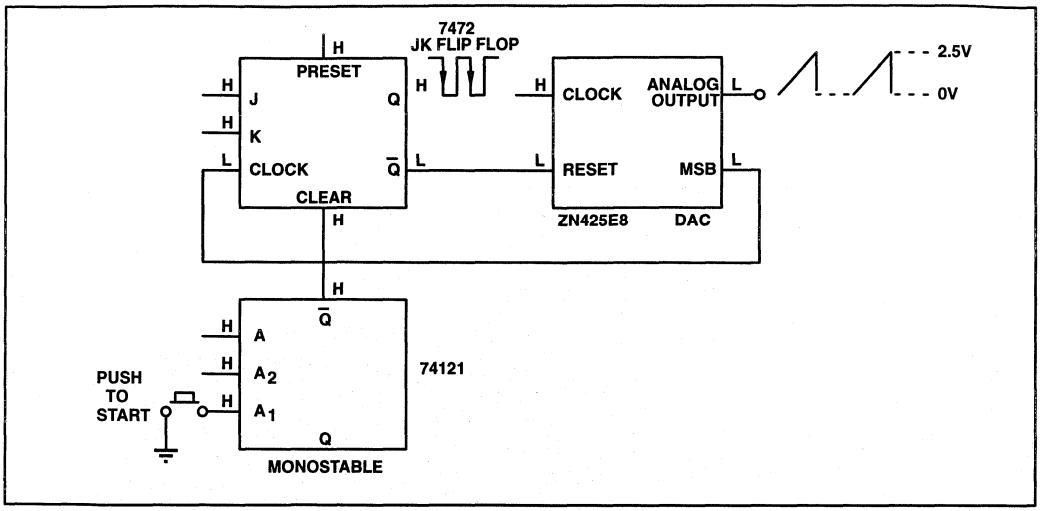


Fig. 11c Alternative one shot schematic

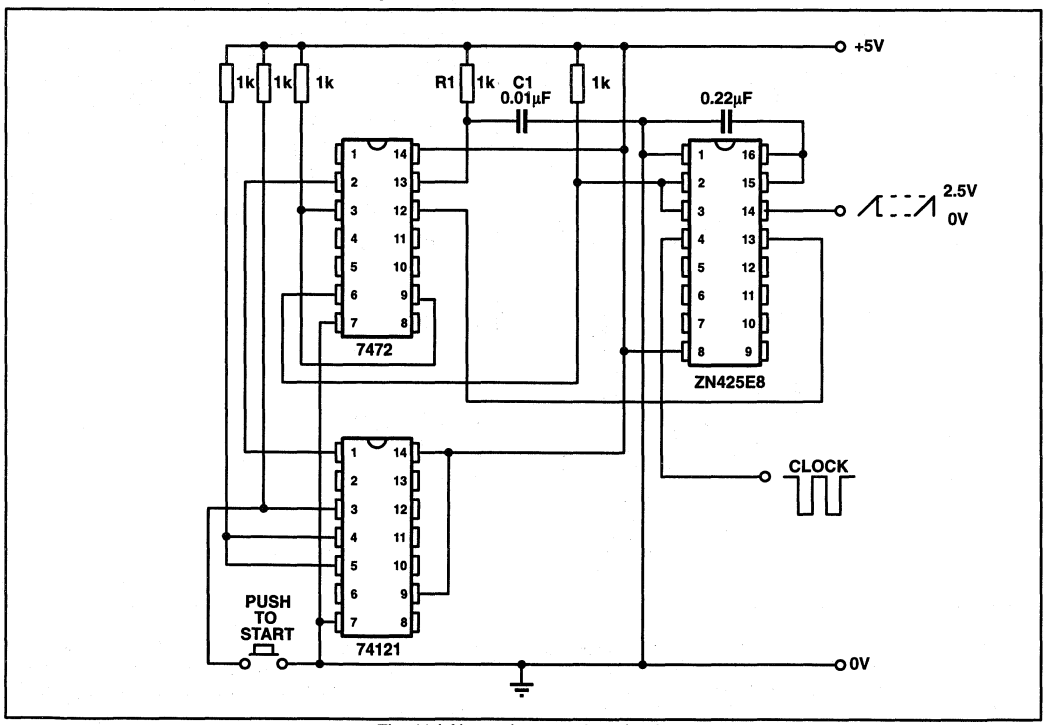


Fig. 11d Alternative one shot circuit

3.3 Weighing and auto zero

The system to be described is intended for either static or on vehicle load indicating applications and employs integrated circuits from GEC Plessey Semiconductors Standard Product range. Variations of the scheme are indicated which increase its range of applications. the overall system is shown in the circuit diagrams of Figs. 12a to 12e.

The basic measuring function is a 3½ digit DVM using the dual slope analog to digital converter principle. This displays an analog input of up to ±1999mV which is scaled as required. All the DVM digital and control functions are carried out by a ZNA116E.

The DVM input is driven from a separate unity gain summing amplifier which accepts inputs from any number of channels each consisting of transducer and pre–amplifier.

Included in the system is a push button auto–zeroing circuit which automatically sets the output of the summing amplifier to zero. This facility eliminates any small zero errors which may have accumulated in the transducer and pre–amplifier chain or any false zero readings which can appear when on–vehicle systems are operated on uneven ground. For this function the ZN425E8 8–bit digital ton analog converter is used. This monolithic integrated circuit also includes an 8–bit binary up–counter an a reference voltage generator and by clocking the counter a voltage ramp of 256 discrete steps is generated. This ramp is level shifted to become symmetrically bipolar with respect to 0V and then applied to the virtual earth of the summing amplifier. This forces the amplifier output through 0V and a comparator circuit detects the 0V condition and inhibits the clock pulses to the counter. The selected ramp output level is therefore held indefinitely unless the auto–zero is switched off when the system reverts to the original zero conditions.

Additional facilities include B.C.D. outputs for data logging purposes and an overload alarm system with warning indications.

The alarm system uses two comparators, into which are set two analog levels, one corresponding to a preset percentage of full load and the other to full load. When the load reaches the first level a 1Hz square wave output is available and a separate output gives a continuous signal at the second level. These outputs may be wire oRed or used separately to drive visual or audible alarms.

It is not essential for the DVM function to be fully bipolar in this application because negative readings occur only as small zero errors. A minor modification enables the circuit to display a lower accuracy negative reading at the same time eliminating one of the ZN423 reference generators.

Further modification, appropriate for some applications, results in a 3 digit display with a 1Hz flashing leading zero to indicate a small negative zero error.

This approach, using a mix of standard function integrated circuits gives maximum system flexibility. For example, an on–vehicle application may require separate auto functions on a number of axles or an overload alarm indication may require duplication. By adding the appropriate integrated circuits the system can be tailored to suit a range of vehicle requirements with a minimum of chip function redundancy and therefore minimum cost.

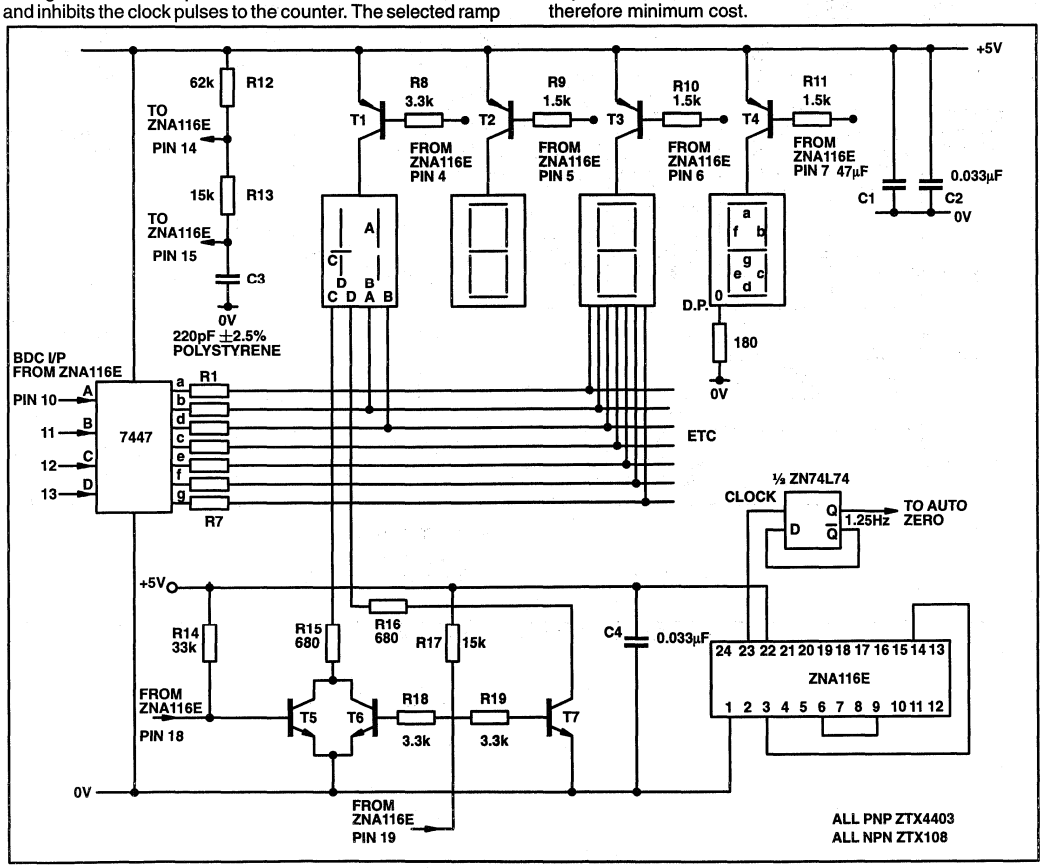


Fig. 12a Display/digit circuit

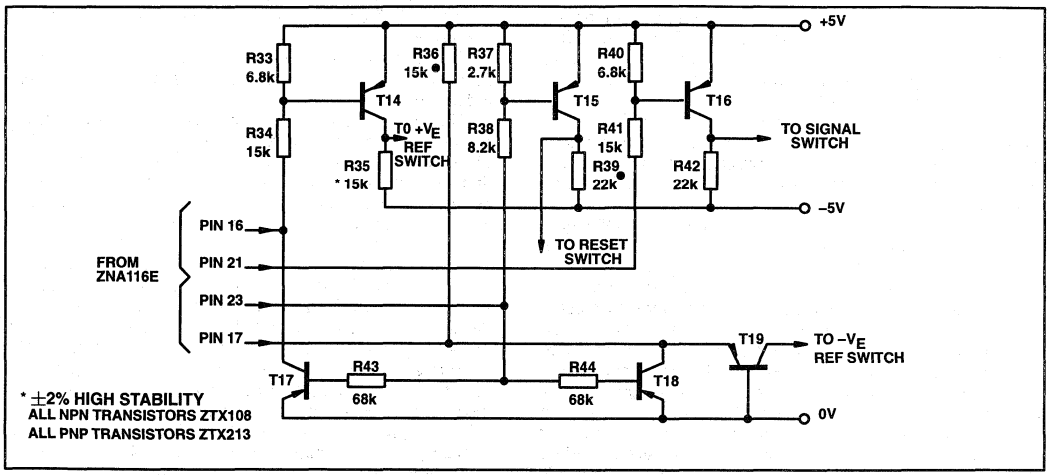


Fig. 12b Analog switch

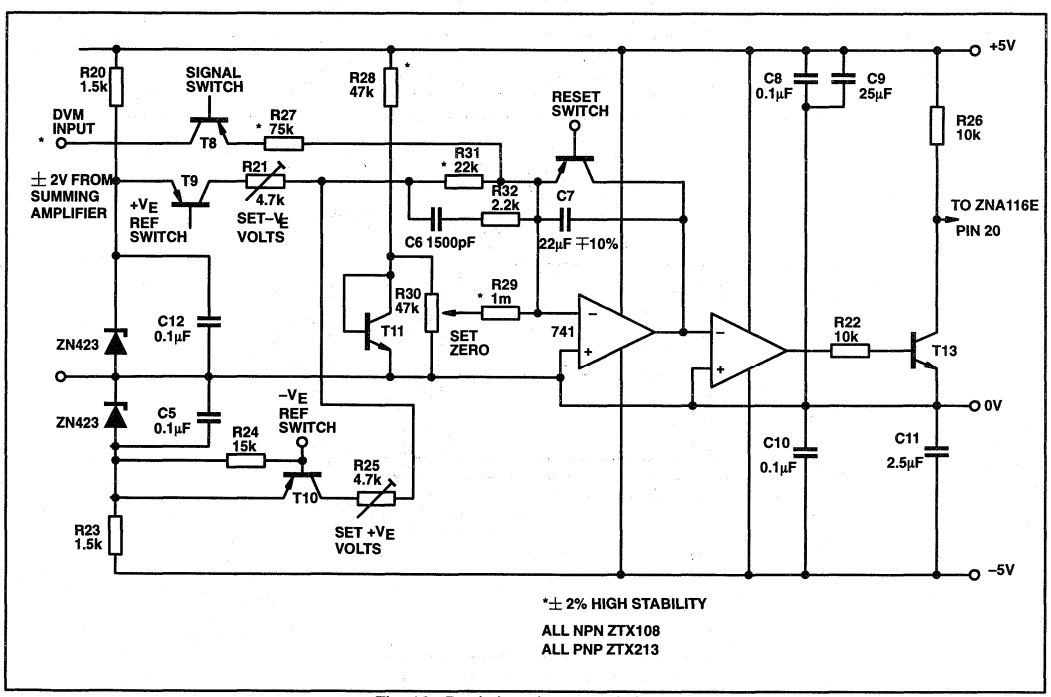


Fig. 12c Dual slope integrated circuit

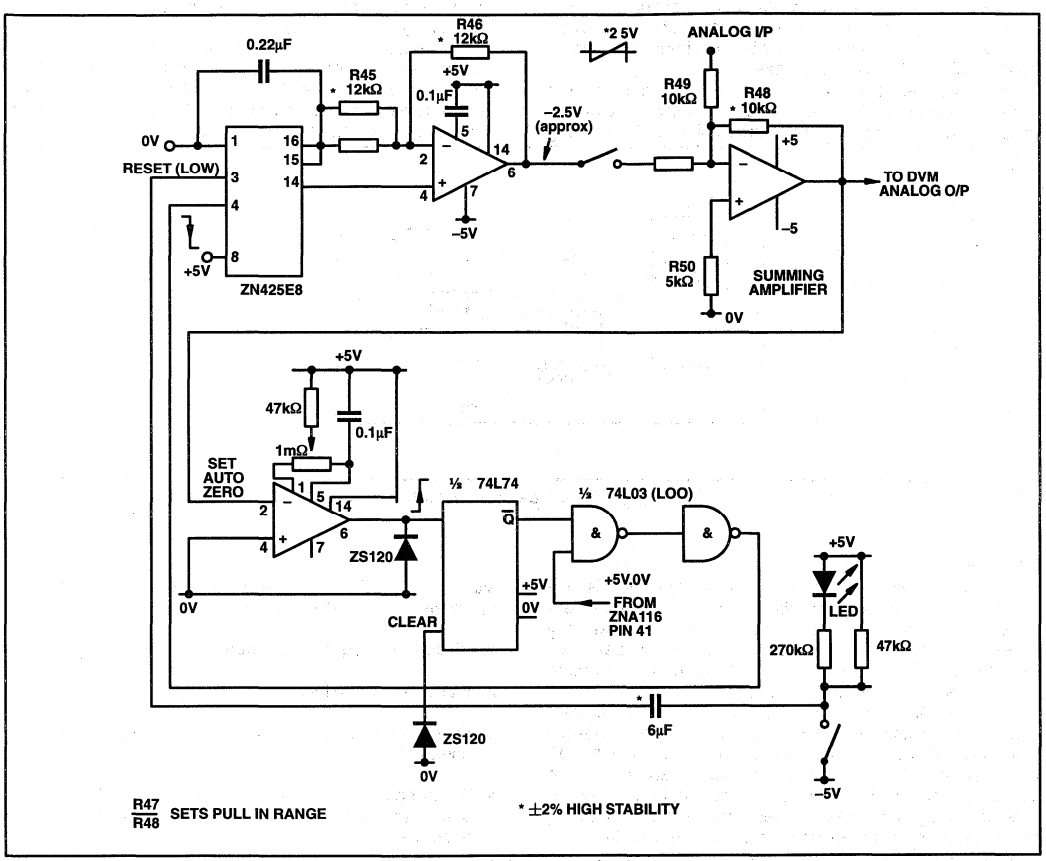


Fig. 12d Auto zero circuit

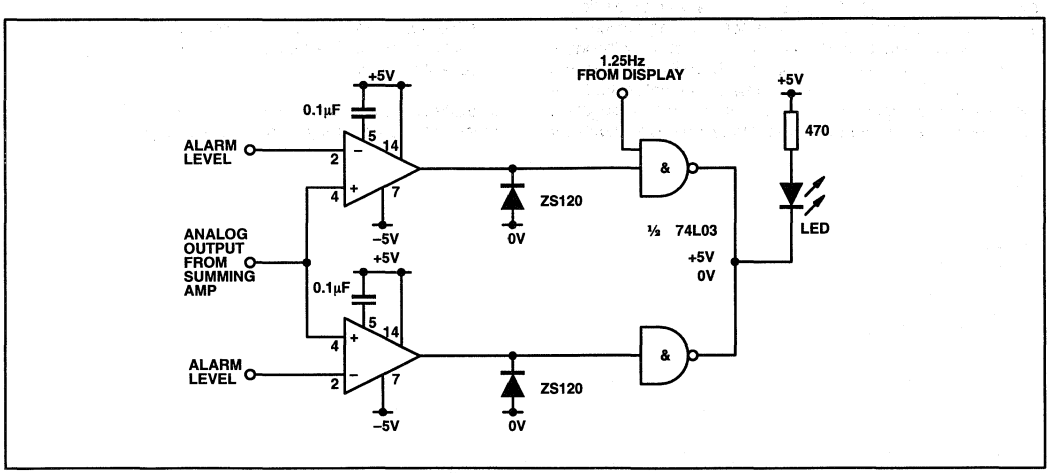


Fig. 12e Alarm circuit

3.4 Peak detect

A peak detect circuit may be constructed simply using the form of A to D system shown in the schematic of Fig. 13. When left running continuously it will hold the maximum input signal level it is able to track i.e. peak detect.

After application of a reset pulse, the state of the comparator enables clock pulses from the Schematic trigger circuit to be fed to the counter of the ZN425E8. The analog output begins to ramp up until it attains the level of the analog input voltage at which point the comparator changes state and inhibits further clock pulses. Therefore, the analog output is held and stored digitally in the bits of the converter. It will continue to hold this level until a further increase in analog input voltage changes the comparator state, enabling the clock, and the sequence is repeated.

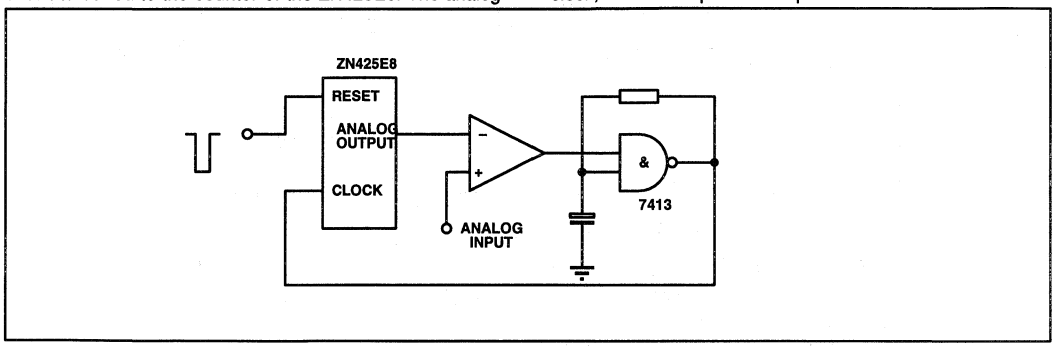


Fig. 13 Peak detect schematic

3.5 Channel selector

Another interesting application of the A–D principle is for a channel selector in communications, e.g. citizens or amateur band. In effect it replaces a multiway switch, mechanically limited to 24 or 30 channels, by a 10 turn potentiometer which can be used with the system of Fig.14 to generate many more discrete steps. typically 64 but up to 256.

The ZN425E8 with internal counter, provides the A–D conversion function, using a single 7400 package for external logic, and a high performance op–amp as comparator. A 7413 dual Schmitt trigger provides the necessary clock and conversion oscillators, no sync is needed here. Channel selection is by the 10 turn potentiometer 'Main Tune' or, optionally, by preset potentiometers, to preferred channels. Resistance values for the pots are not critical.

The binary output is converted to BCD by the 74185 and latched to provide a steady output signal i.e. when a particular channel has been selected no jumps occur during cycling. The conversion oscillator periodically checks the state of the input voltage, by a fresh conversion on the ZN425E8 and updates the latches when the status command indicates that the conversion is complete. The BCD signals drive 7–segment indication of channel number and provide the drive outputs for either a modulo–N digital synthesiser, a crystal bank synthesiser,or a crystal selector. Features of the system are:–

1. Bi–directional, quasi–continuous tuning on a single control.
2. Electronic tuning lock
3. Simple switching between 'tune' and 'preferred channel' operation.
4. Preferred channels selected by preset potentiometers operating through to the synthesiser. Channels are user alterable.
5. Inherent non–volatile 'memory' on potentiometers.
6. Channel number indication shows channel actually in use, particularly suitable for non co–channel working, repeaters, etc.

In addition, a scanning facility can be easily added if the receiver used has a squelch switched output.

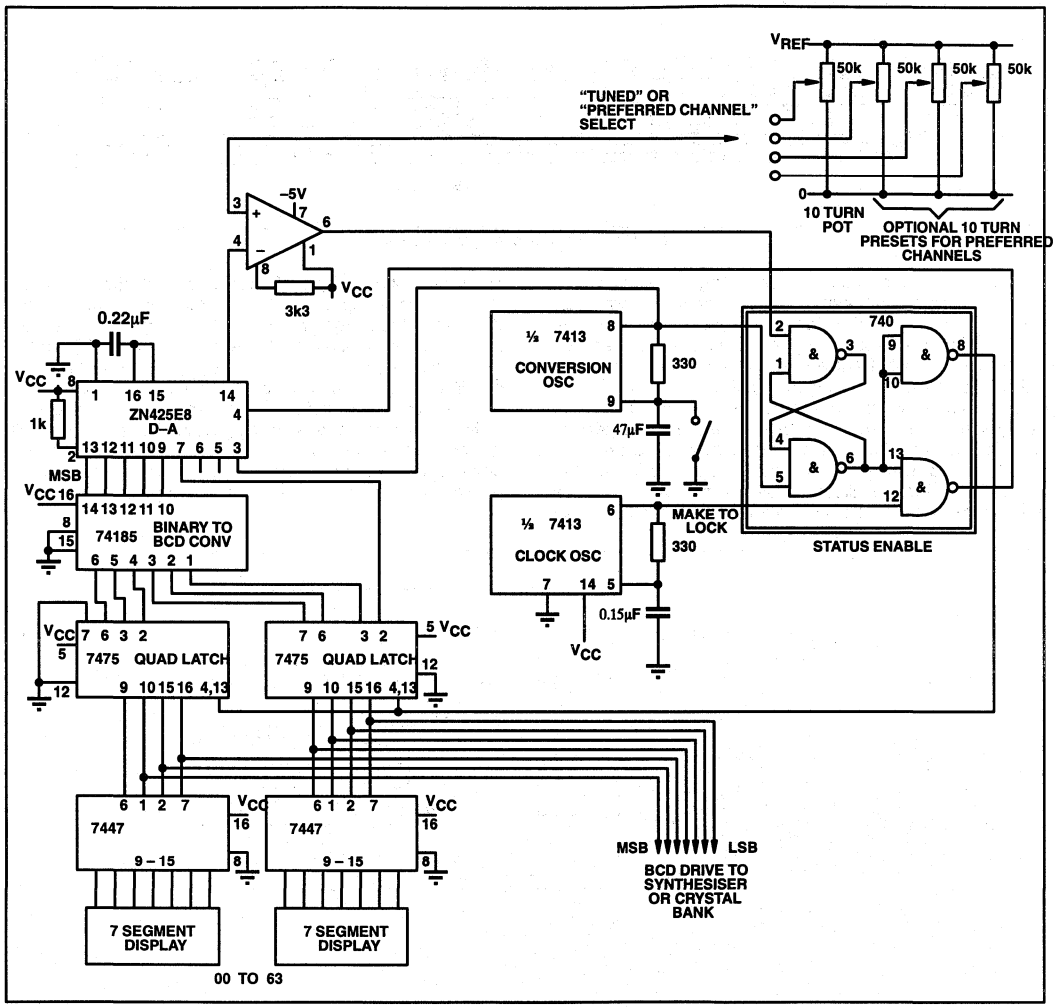


Fig. 14 Channel selector, 64 way

3.6 Bargraph display drive system

The ZN425E8 may be used in its continuous ramp mode very advantageously in conjunction with linear light emitting diode (LED) displays, e.g. Bar–graphs. This is because the LED displays lend themselves to being accessed in a matrix fashion using a time sharing or multiplexing technique. This allows a reduction in the number of connections required, to m+n in an array of m n diodes (Fig. 15a). This reduction in connections also allows a simplification of the drive system, as described below.

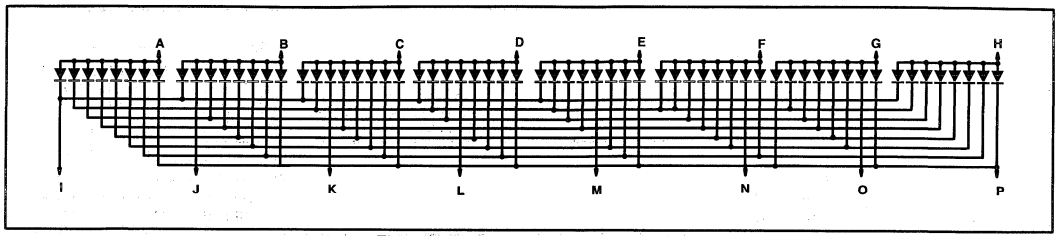


Fig. 15a Diode matrixing connections

The simplest techniques for providing for a bar output whose length is proportional to an analog input is shown in Fig. 15b. The ZN425E8 is driven in its continuous ramp mode. The six most significant digits from the counter are then decoded into two lots of 1 out of 8 drives. These drives then access the LEDs in a multiplexed fashion, so that the 64 LEDs are accessed once each in turn in a complete scan cycle. A high clock frequency is selected which ensures that the flicker rate is fast enough and thereby indistinguishable to the eye.

At the same time as the LED scan cycle is taking place, the ZN425E8 provides a staircase analog output, as shown. This is compared with the analog input in a comparator, whose output controls the display enable. Thus while the ramp is less than the analog input, the LEDs being scanned are enabled (the start of the Bargraph line), while once the ramp output is larger than the analog input, the drives to the LEDs further along the line are inhibited. This, therefore, provides an illuminated bar length proportional to the analog input.

This system as it stands suffers from a minor disadvantage, in that the duty cycle for accessing each LED is 1/m n, or 1/64 for the case of Fig. 15b. Although the LEDs become more efficient with pulsed operation, 1/64 duty cycle does not provide adequate brightness for some applications.

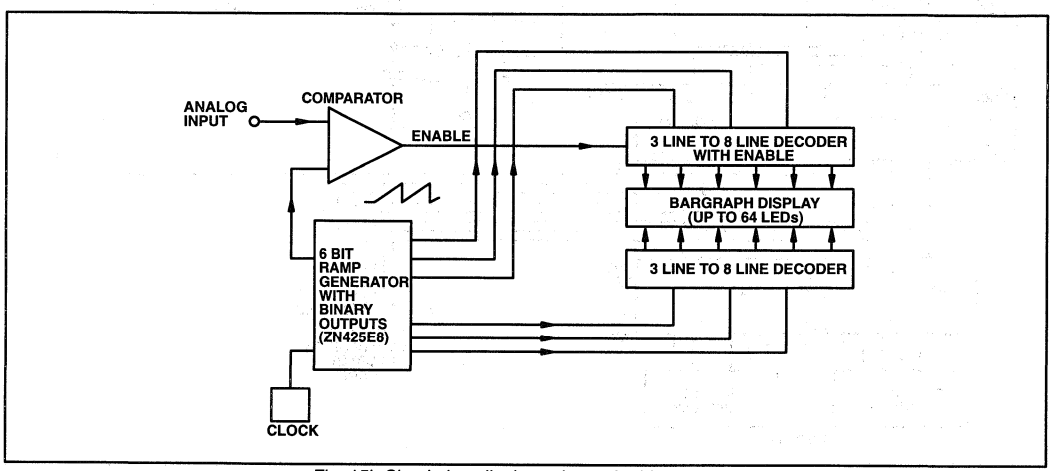


Fig. 15b Simple bar display schematic drive system

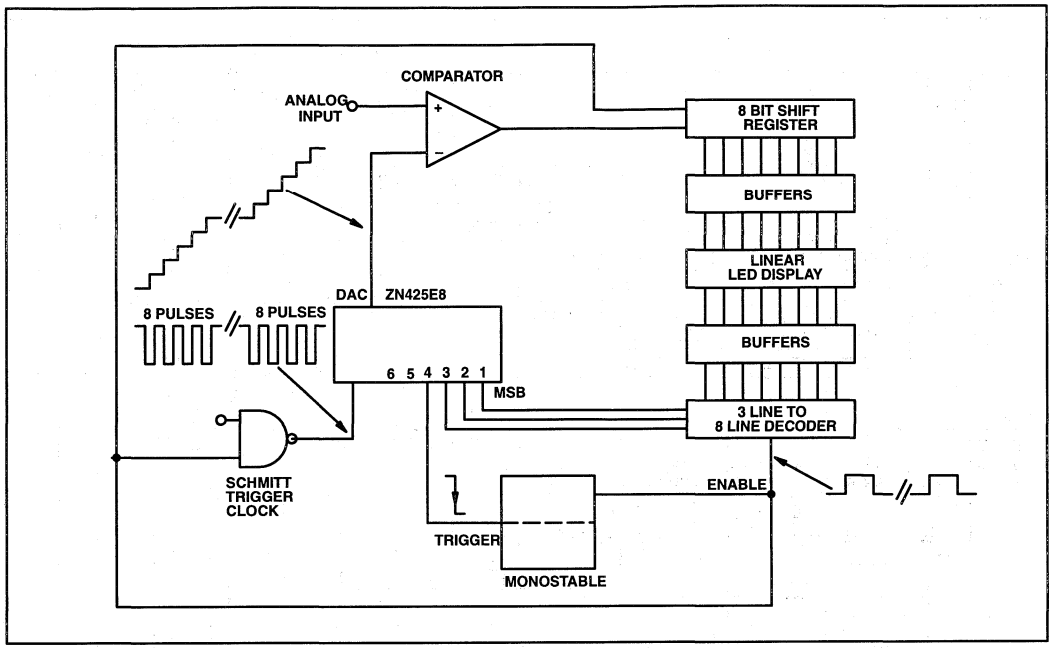


Fig. 15c Improved bar display schematic drive system

A technique to overcome this objection is shown in outline in Fig.15c. The technique used here is to load a shift register rapidly serially, and subsequently use this register to provide LED multiplex drives in parallel. This means that the duty cycle for accessing the LEDs is improved (for a 64 LED array) from 1/64 to just less than 1/8. This is quite sufficient for acceptable brightness in virtually all applications.

This system operates as follows. While the monostable is in its mode of loading the shift register, the ZN425E8 staircase output increases in 8 discrete steps. Simultaneously the shift register is loaded with the comparator output to provide serial to parallel conversion. The comparator output is thus effectively changed from serial access to parallel access of the linear LED array.

When the monostable changes over to its (longer period) display mode, the LED array is accessed, and the LEDs are driven or otherwise according to the enable or disable information stored in the shift register. The display is incidentally disabled while the mono is loading the register.

To provide an example of operation, suppose the bar is to have the first 37 LEDs displayed, with the rest blanked. Starting from the ZN425E8 being reset and the mono in its register load state, operation is as follows. The mono allows eight clock pulses through the gate to the ZN425E8 after which the ZN425E8 count pulse retriggers the mono. These eight pulses generate the first eight steps from the analog output, which produce from the comparator a continuous display enable (say logic 1). These are loaded into the shift register which thus finishes with 11111111 in parallel to the LED display.

At this point the mono is tripped into its display mode, and the counter has reached 8 (or 001000). However the decoder must access the first eight LEDs, so that the second decoder output is connected to the first set of LEDs. These are all illuminated.

During the second register load period, the cycle is repeated, with again all ones being loaded into the register which subsequently brightens up the second eight LEDs (9–16). The same occurs during the third and fourth mono cycles, lighting up the first 32 LEDs

During the fifth register load period, the analog output goes up a further eight steps. However after the fifth step the comparator changes over to load zero for the remainder of this period into the shift register. If loaded from the left the register will then finish up as 00011111. Subsequently during the mono display period LEDs 33 to 37 inclusive will be lit, but 38 to 40 will be blanked off. The sixth to eighth mono cycles will load zeros into the shift register, blanking off LEDs 41 to 64. The full LED scan cycle is therefore completed with the desired effect.

Typical system clock rates are 400kHz, and typical monostable periods 500µs for the values shown.

An actual circuit to achieve this is shown in Fig.16 and it may be seen that this is elegant and simple. The type of display which may be accessed in this way is the Bowmar Microstic R1M–053–66A, which is connected in eights on its common anodes. This has 64 red LEDs and a further two LEDs at the ends, one to show the display is working, and the other for over–range. Similar techniques may be used with the 106 LED version.

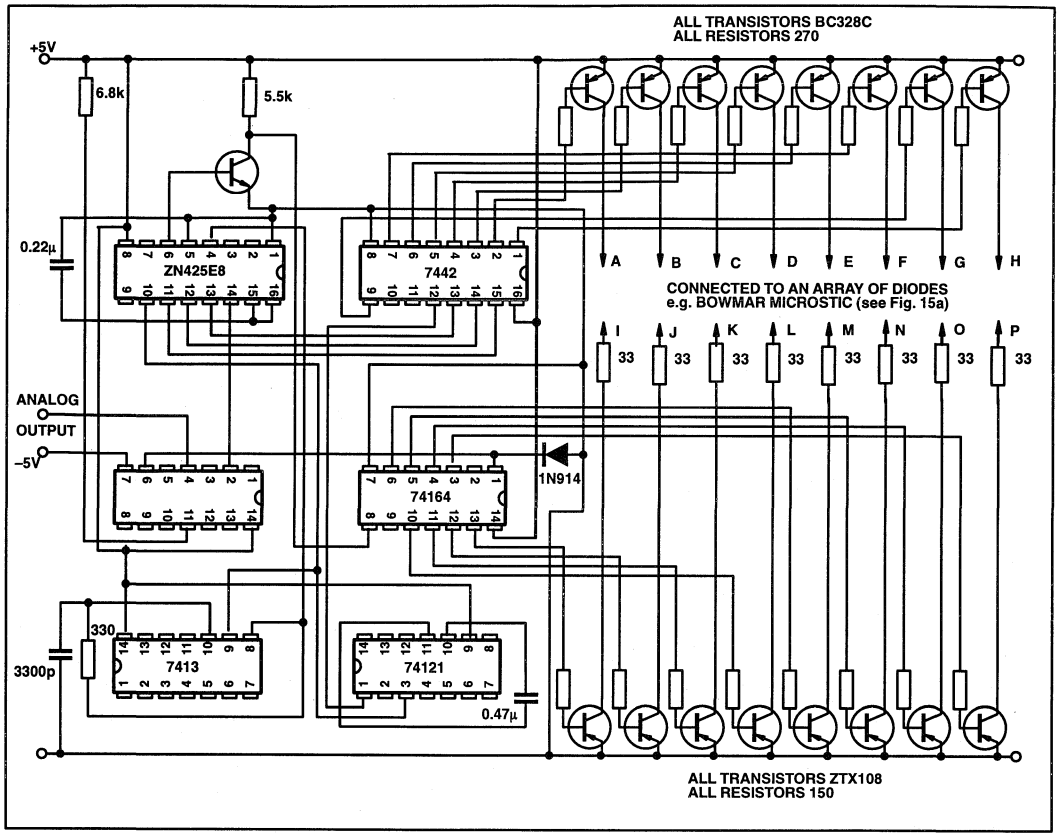


Fig. 16 Column display drive system

3.7 Up down or tracking

The counter on the ZN425E8 is only an up counter, and some systems, e.g. tracking converters or servos, may require an up/down counter. This conveniently provided externally, e.g. the 74193 using the ZN425E8 purely in its D–A converter mode and ignoring the counter (Fig. 17) While this may appear to be inelegant it is nevertheless economically sound.

4.MULTIPLY/DIVIDE

4.1 Multiplier

The rererence supply to the D–A section of the ZN425E8 has been purposely left on an uncommitted terminal, so as to allow connection either from its own reference or from an external reference. The point about an external reference is that it allows a multiplying effect, in that the analog output is proportional both to the binary code and the reference voltage. For this reason this type of DAC is called a multiplying DAC.

Practical limits in multipling voltages are 0 and 3V.

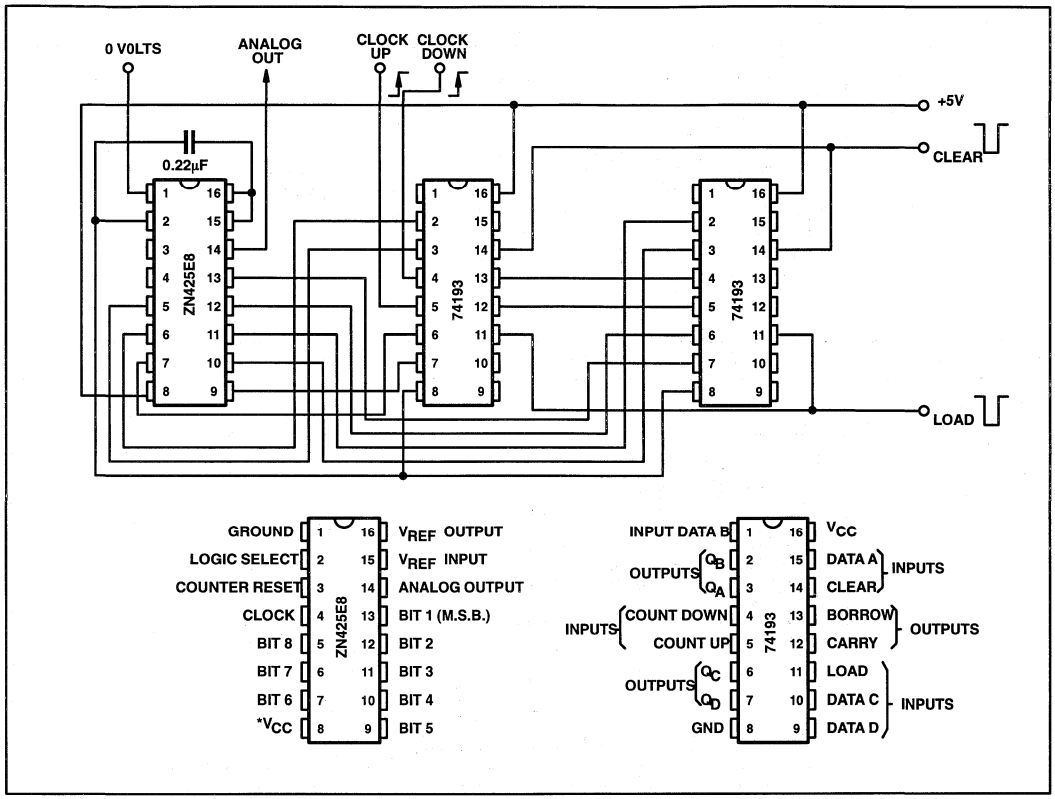


Fig. 17 Up/down counter or tracking DAC circuit

4.2 Variable frequency divider

If a ZN425E8 is operated in its continuous ramp mode in conjunction with a comparator whose output is fed back to the counter reset, a variable frequency divider can be constructed as shown in Fig.18a. Here an analog voltage can be used to control the number of steps before reset is applied, the overall effect being to provide variable frequency division under the control of a potentiometer.

4.3 Voltage controlled oscillator

The schematic of Fig. 18a may also be used as a voltage control oscillator. However the frequency is the inverse of the applied voltage, though the period is, of course proportional. The corresponding circuit of Fig. 18b gives an output frequency or pulse rate which is inversely proportional to applied voltage as shown in Fig. 18c. It is, however, in some cases more desirable to produce an output frequency directly proportional to applied voltage. This is accomplished by the circuit depicted in Figs. 19a and 19b and involves the use of an inverse scaler described in the next section, for which a brief mention is necessary to understand the basic operation of the VCO.

By using a DAC in the feedback loop of an operational amplifier an output voltage is derived which is inversely proportional to a digital input number to the DAC. Clock pulses applied to the DAC counter will produce a repetitive output waveform which is a hyperbolic $\frac{1}{n}$ function.

This waveform is applied to the inverting input of a comparator whilst the analog input voltage to be frequency converted is applied to the non inverting input. At the instant they become equal the comparator changes state and operates the Schmitt trigger which resets the DAC counter. The result is a train of negative going pulses whose frequency is directly proportional to the applied input voltage. This follows simply because if F_{Clock} = clock frequency to the DAC counter and F_{out} = output frequency, then $F_{out} = \frac{F_{Clock}}{n}$

where n = digital input number and analog input voltage to the comparator $V_{in} \propto \frac{1}{n}$

Therefore, $F_{out} \propto V_{in}$ and the appropriate characteristic is shown in Fig.19c.

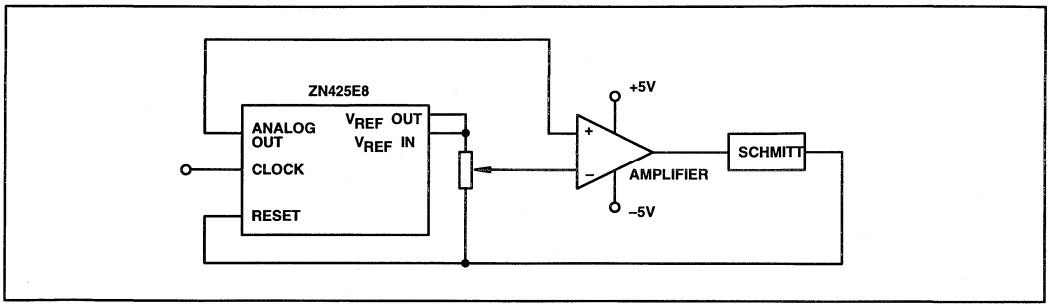


Fig. 18a Variable frequency divider or VCO schematic

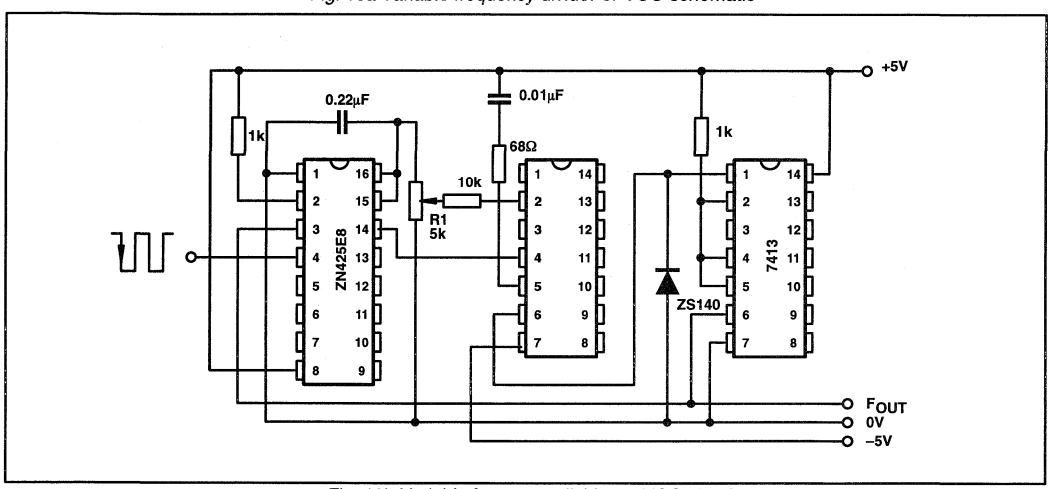


Fig. 18b Variable frequency divider or VCO circuit

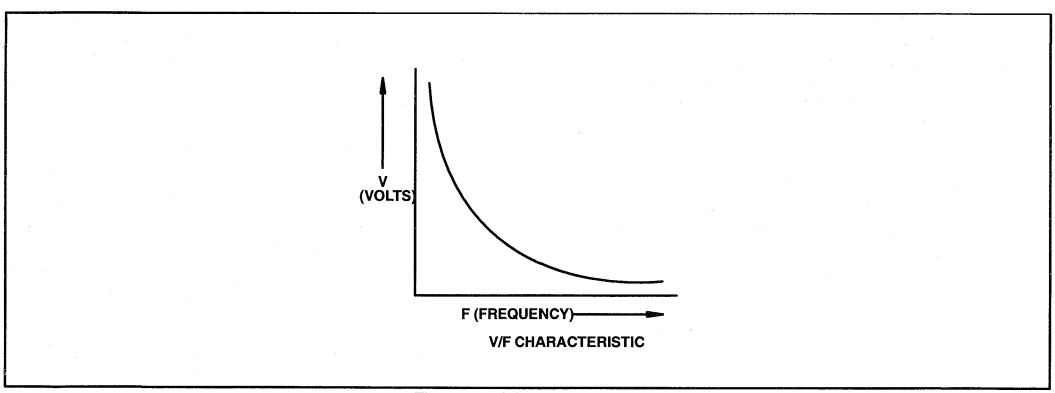


Fig. 18c VCO characteristics

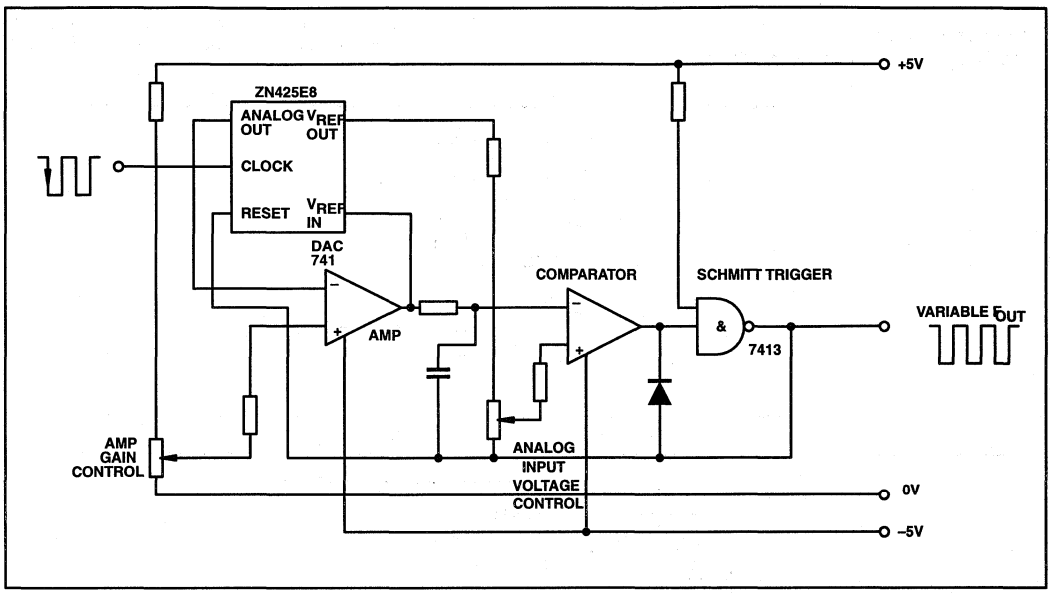


Fig.19a Schematic of VCO giving frequency proportional to voltage

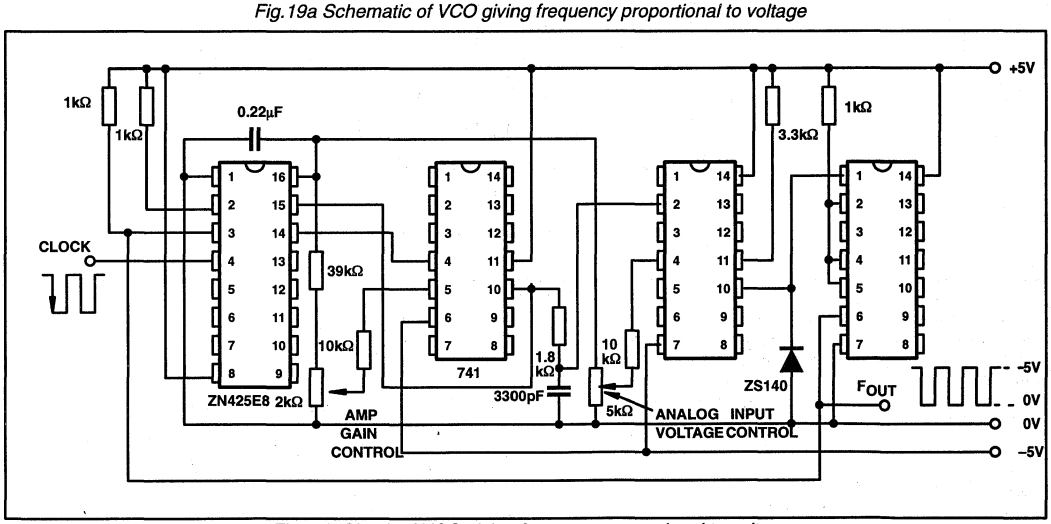


Fig.19b Circuit of VCO giving frequency proportional to voltage

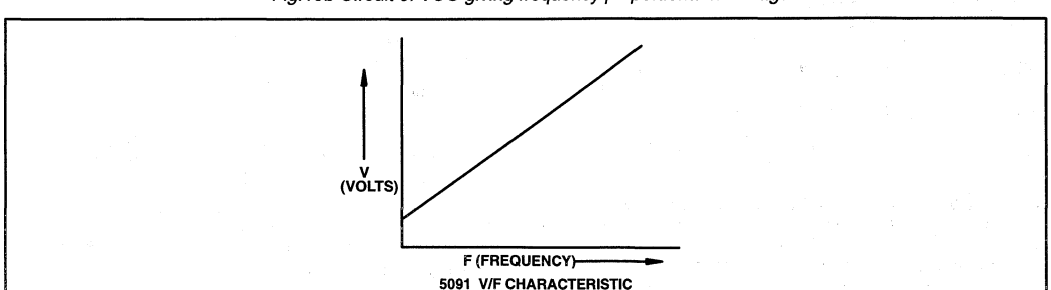


Fig.19c VCO characteristics

5. FUNCTION GENERATION

By virtue of the multiplying function, the ZN425E8 may also be used for function generation as described below.

5.1 Inverse scaler

If a DAC is operated in the feedback loop of an operational amplifier then the amplifier gain is inversely proportional to the input digital number or code to the DAC. The version giving scaling inversely proportional to positive voltage is shown in the schematic of Fig. 20a and the practical circuit of Fig. 20b.

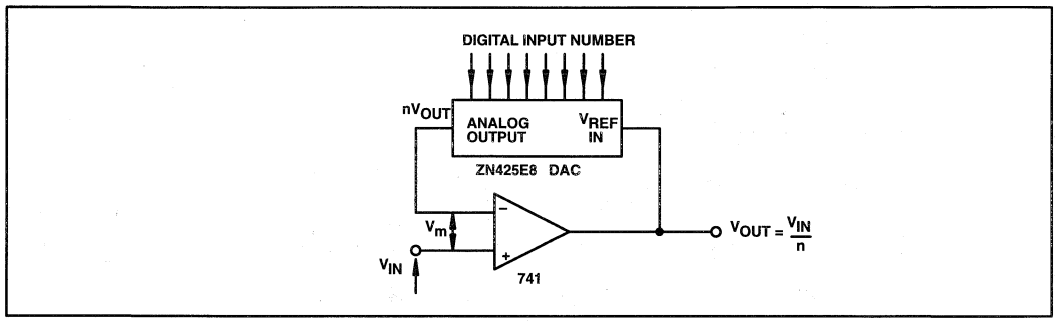


Fig. 20a Inverse scaler schematic

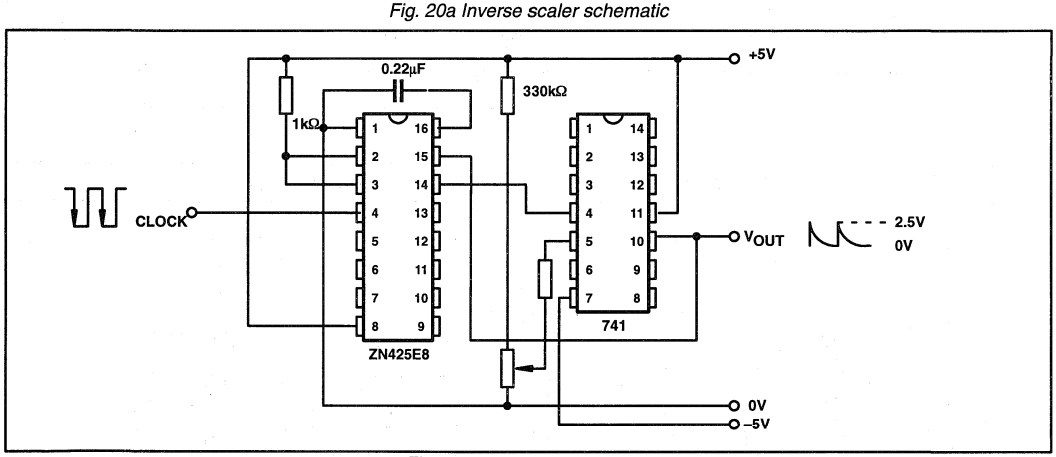


Fig. 20b Inverse scaler circuit

If A = open loop gain of the operational amplifier, and n is a fractional number representing any digital input (00000000 to 11111111 for 8 bits), that is a fractional number between 0 and 255/256 then from the diagram $V_{out} = AVm$, and $V_m = (V_{in} - nV_{out})$

$\therefore V_{out} = A(V_{in} - nV_{out})$ from which

$$V_{out}(1+An) = AV_{in} \quad \frac{V_{out}}{V_{in}} = \frac{A}{1+An}$$

Since $An \gg 1$, (A=100,000) then

$$\frac{V_{out}}{V_{in}} = Gain\ (G) = \frac{A}{AN} = \frac{1}{n}$$

For n = 1LSB = $\frac{1}{256}$ then the maximum allowable input voltage V_{in} to prevent saturation

$$(V_{sat} \simeq 4V) = \frac{4}{256} \simeq 15mV$$

If n = 0 then G = A and for a fixed input level the amplifier output will normally be equal to the saturation voltage since A = 100,000.

The complementary mode (scaling inversely proportional to negative voltage) is shown in Fig.20c (schematic) and Fig. 20d (practical circuit).

$$V_m = \left[V_{in} - \left(\frac{V_{in} - n\ V_{out}}{R_1 + R_F} \right) \right], \quad and\ V_{out} = -AV_m$$

If $\frac{R_1}{R_F} = F_1$ = inverting feedback return then

$$V_{out} = -A\left[V_{in} - \left(\frac{V_{in} - n\ V_{out}}{1 + F_I + nAF_I} \right) \right],$$

From which $V_{out} = -\left[\frac{AV_{in}}{I + F_I + nAF_I} \right]$

If the input voltage V_{in} is negative with respect to ground, then

$$Gain\ (G) = \left[\frac{A}{1 + F_I + nAF_I} \right]$$

If we make $F_I = 1$, i.e. $R_I = R_F$ then G $\left[\frac{A}{2 + nA} \right]$

But nA > 2 (since A ≃ 100,000)

and G = $\frac{A}{nA} = \frac{1}{n}$ as with the non inverting circuit.

Figs. 20a and 20c illustrate both types of inverse scalers, where a repetitive waveform of a $\frac{1}{n}$ function is generated by feeding clock pulses to the counter of the DAC.

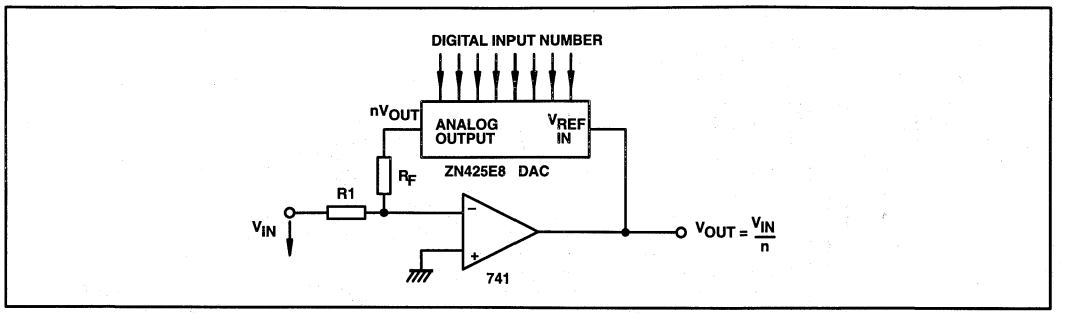


Fig. 20c Complementary inverse scaler schematic

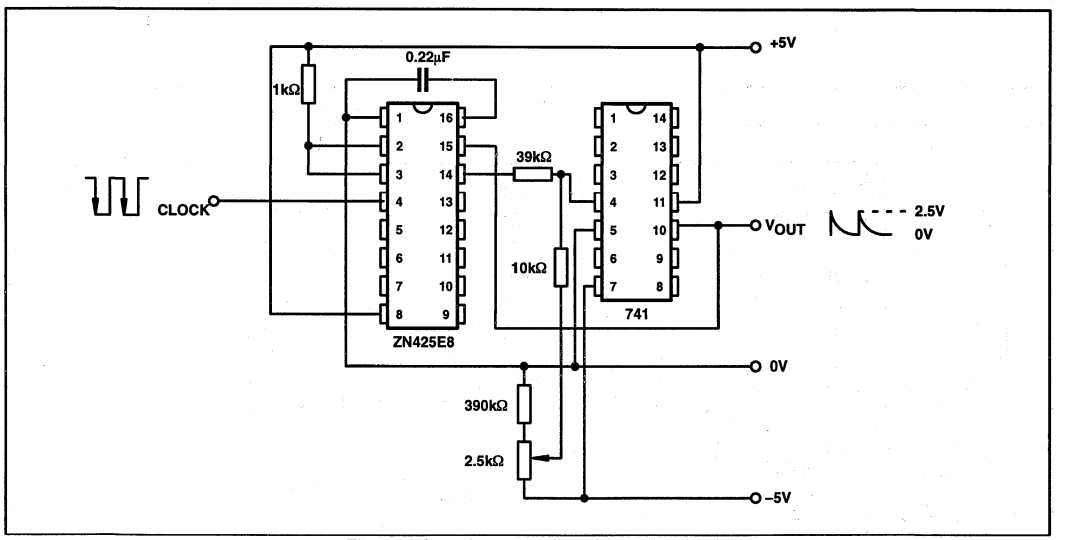


Fig. 20d Complementary inverse scaler circuit

5.2 Parabola

The multiplying action of the ZN425E8 may be used to generate a parabolic waveform shown schematically in Fig.21a and a practical circuit Fig. 21b.

Basically the circuit operates as follows;

A continuous ramp output is generated by feeding clock pulses to the counter of a ZN425E8 DAC using its internal reference which is buffered, level shifted, and finally inverted using two operational amplifiers, so that the inverted ramp starts at a peak amplitude ($V_{1\ REF}$ =2.5V) and decreases linearly to zero. This is then used as an external reference supply for a second ZN425E8 DAC whose bits are connected to the first DAC for synchronous clocked operation. The resulting analog output from the second DAC is a repetitive parabolic waveform whose

peak amplitude is equal to $\frac{V_{1\,REF}}{4} = \frac{2.5}{4} = 0.625V$

This follows because,

If N = a fractional number representing the digital input to both DACs then the analog output voltage from the first DAC = An (where A = $V_{1\ REF}$ =2.5V).

This is then inverted and level shifted to provide the reference voltage to the second DAC = (A–An) = $V_{2\ REF}$.

Therefore the analog output from the second DAC = n (A–An) =An–An^2 which is the equation of a parabola about the x axis of the form y=ax^2+bx+c.

Peak amplitude of the parabola occurs when n = $\frac{1}{2}$

for which $V_{out} = \frac{1}{2}\left(A - \frac{A}{2}\right) = \frac{A}{4} = \frac{V_{1REF}}{4}$ as stated

It should be noted the the ramp output from the non inverting buffer amplifier will inherently have a gain greater than unity, and therefore its peak amplitude will be some factor in excess of $V_{1\ REF}$. However the ramp invertor and level shifter introduces corresponding attenuation to compensate this so that gain and level shift controls provide adequate adjustment in obtaining the desired inverted ramp output of peak amplitude.

$$A = V_{1REF} = 2.5V$$

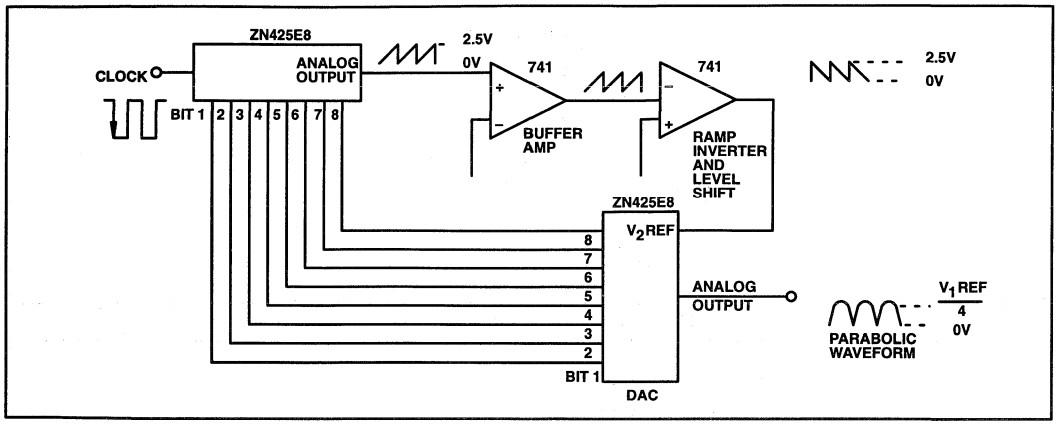


Fig. 21a Parabolic waveform generator schematic

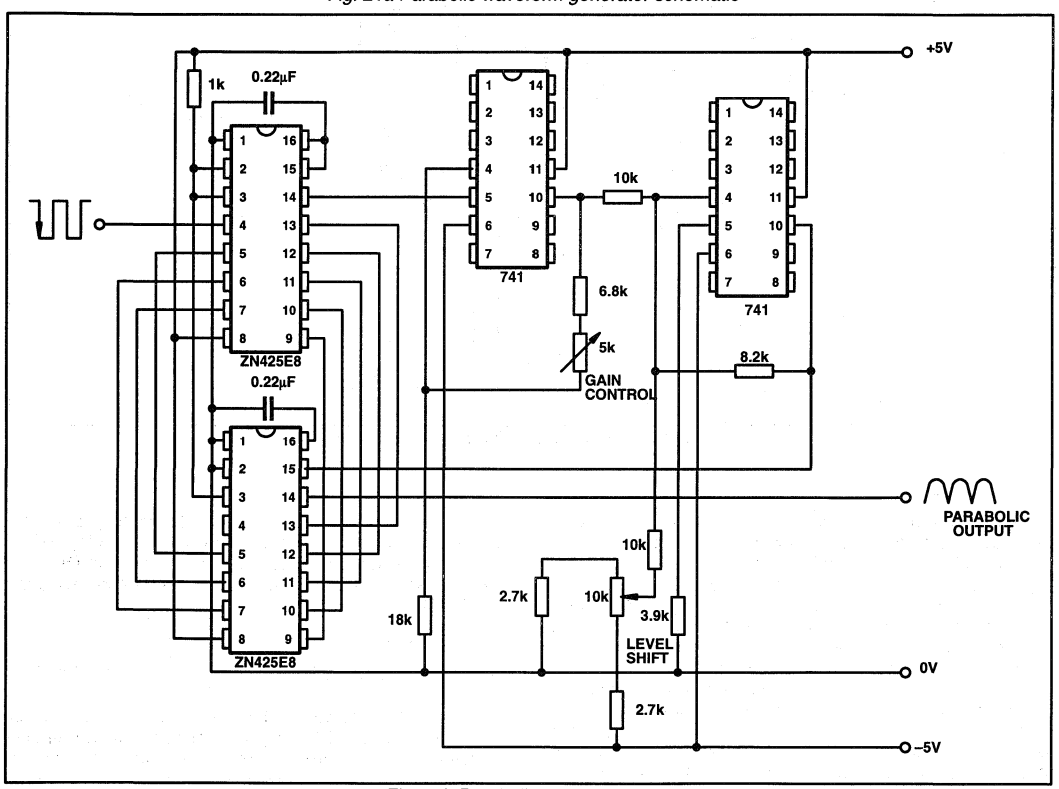


Fig. 21b Parabolic generator circuit

5.3 Log approximation

A more complex function y = log n can be performed with the aid of previously described building blocks. A schematic arrangement as shown in Fig.22a and the corresponding practical circuit of Fig. 22b provides a repetitive logarithmic relationship. The basic method is as follows.

An inverse scaler is used to generate an output voltage which is inversly proportional to a digital input number n to a ZN425E8 DAC. This voltage is then converted to a frequency or pulse rate using a VCO whose output frequency is proportional to an applied voltage. The derived train of pulses of varying mark to space ratio are then fed into the counter of

a final ZN425E8 DAC, these are integrated and a logarithmic output

$$\left(\frac{1}{n}dn = log\ n\right)$$ is obtained

The period of the analog $\frac{1}{n}$ function is dependent upon the input frequency to the inverse scaler. To rapidly convert this function to a pulse train and to generate a sufficient number of pulses for integration during this period, the clock frequency to the VCO derived from the Schmitt trigger must be high. The lower input frequency to the inverse scaler in synchronism with this clock frequency is obtained by using two 7493 dividers and equals the clock frequency divided by 256. For the CR values indicated in the Schmitt trigger F_{clock} = 512kHz therefore the input frequency

to the inverse scaler $= \frac{512x10^3}{256} Hz = 2000Hz$

And the output repetition frequency of the $\frac{1}{n}$

function $= \frac{2000}{256} Hz$ for which the period = $\frac{256s}{2000} = 128ms$

Some means must be incorporated of resetting the counter on the final ZN425E8 DAC and thereby the logarithmic analog output to zero at the completion of a full cycle of input pulses. Otherwise the analog output would continue to increase with each cycle of pulses until it equalled the internal reference voltage, resulting in a 3 cycle logarithmic waveform. This is accomplished by using the negative going edge from the 4th significant bit which in fact resets the counter on the final DAC the completion of a full cycle of input pulses. Whereas to be strictly correct resetting should be effected from the MSB; bit 4 having been selected purely for convenience as it allow the logarithmic characteristic to be more easily displayed on the oscilloscope, since it accounts for a greater proportion of the output waveform, with negligible loss in amplitude.

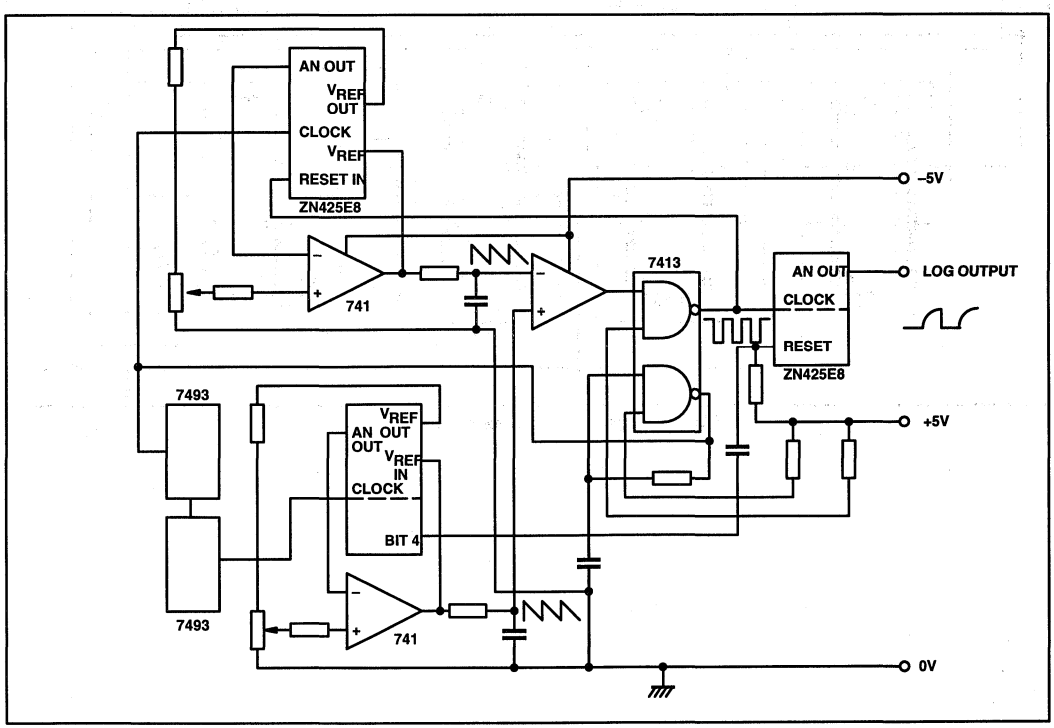


Fig. 22a Logarithmic waveform generator schematic

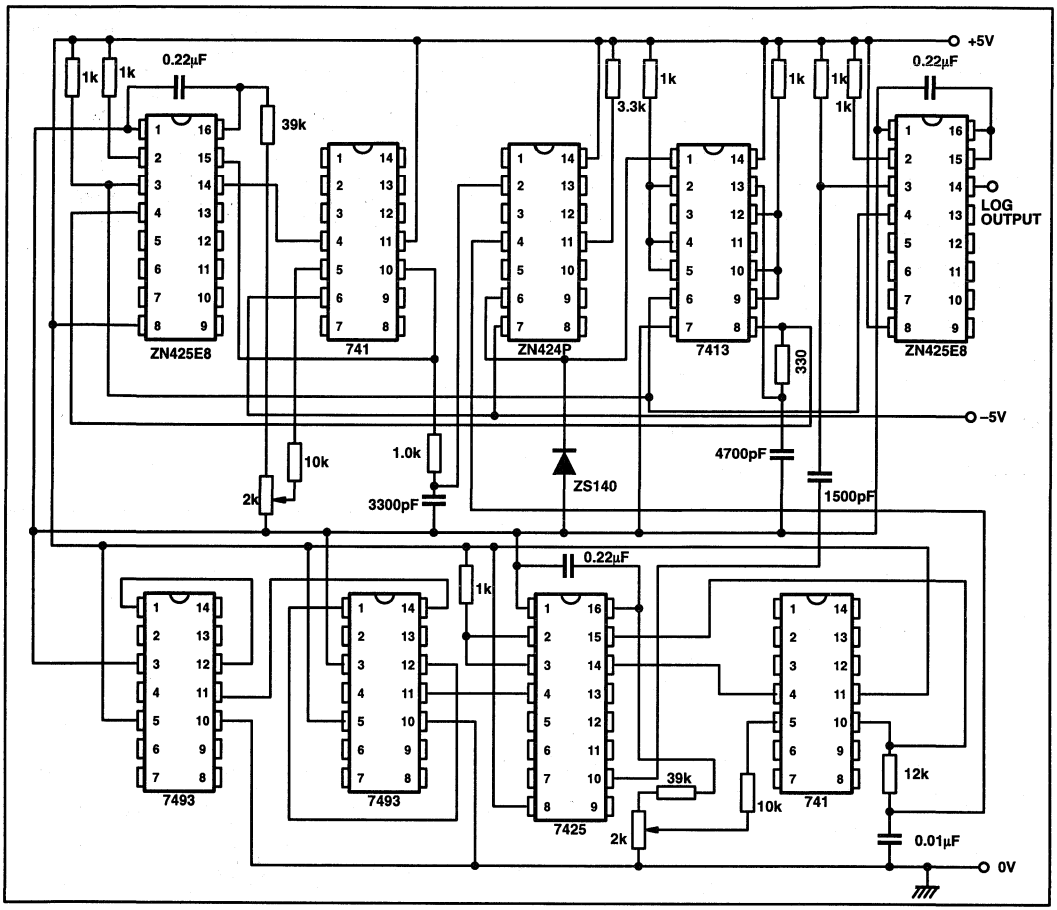


Fig. 22b Logarithmic waveform generator circuit

Direct Bus Interfacing using the ZN427/ZN428 Data Converters

This application note introduces two converters and describes how they can easily be interfaced directly to most of the popular types of microprocessor with particular reference to the 6800 and 8085A.

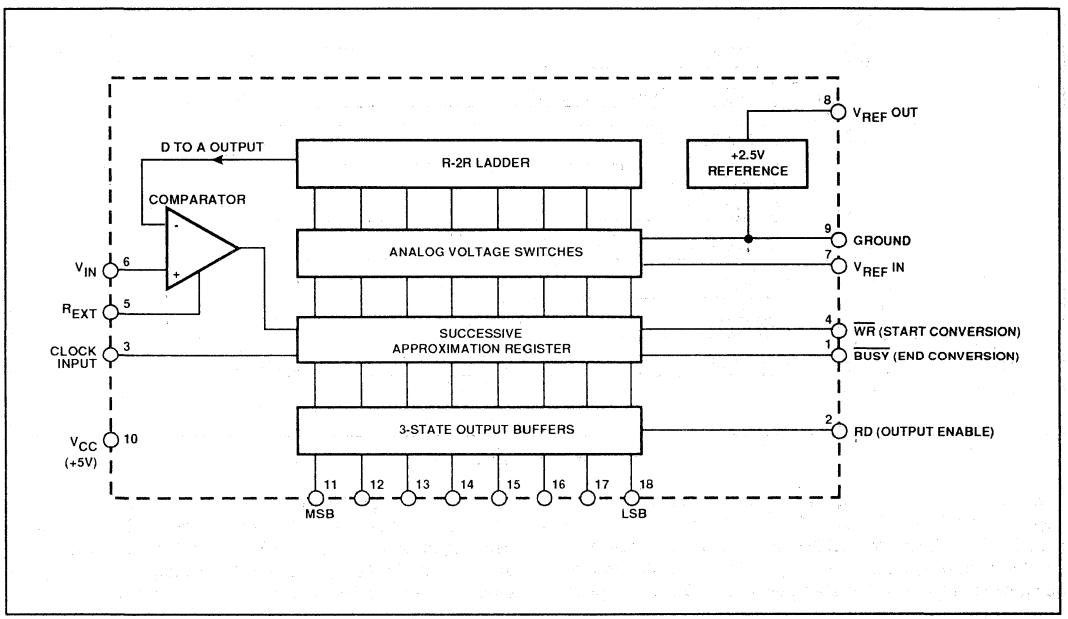


Fig.1 ZN427 logic diagram

The ZN427 A-D converter

The ZN427 is an 8-bit, successive approximation A-D converter (ADC).

It features three-state output buffers to permit bussing on to common data lines, fast 15µs conversion time and no missing codes over its full operating temperature range. The ZN427 contains a voltage switching D-A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5 volt precision bandgap reference.

The use of the on-chip reference is pin optional to retain flexibility, an external fixed or varying reference for ratiometric operation may, therefore, be substituted. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a resistor from the R_{EXT} pin 5 to the negative supply rail.

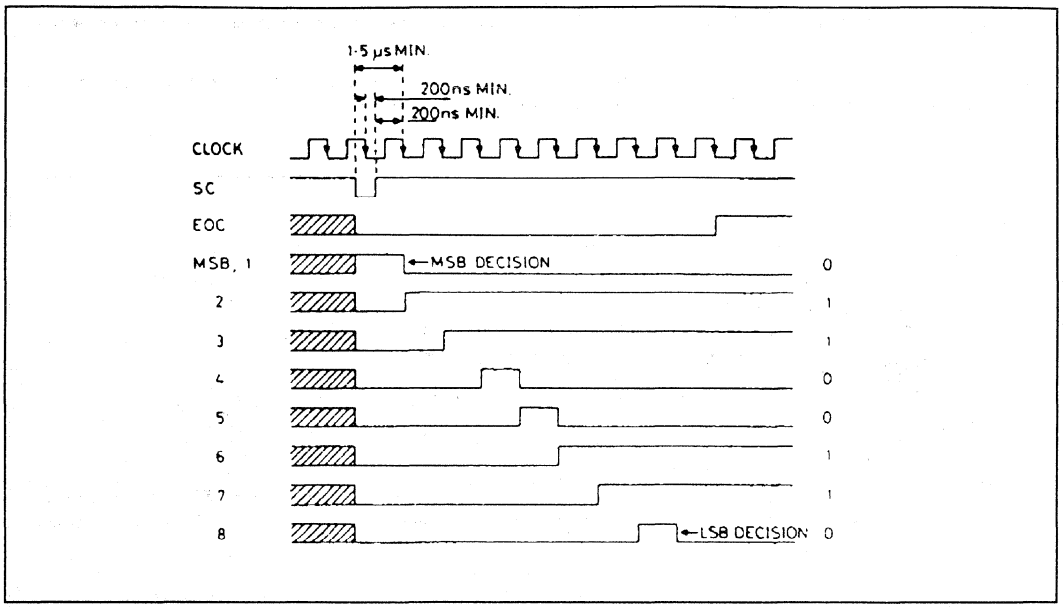


Fig.2 ZN427 timing diagram

The conversion cycle is initiated by a negative going pulse applied to the START CONVERSION (SC) input, this sets the END OF CONVERSION (EOC) output to a logic '0' indicating that the converter is busy, see Fig.2. On the ninth negative going clock edge after the start pulse the EOC output goes back to logic '1' signalling that the cycle is complete. The binary output data is latched until the next start pulse. The three-state data outputs are switched OFF (high impedance state) when the OUTPUT ENABLE (OE) input is at a logic '0' and they are enabled when the OE input is taken to a logic '1'.

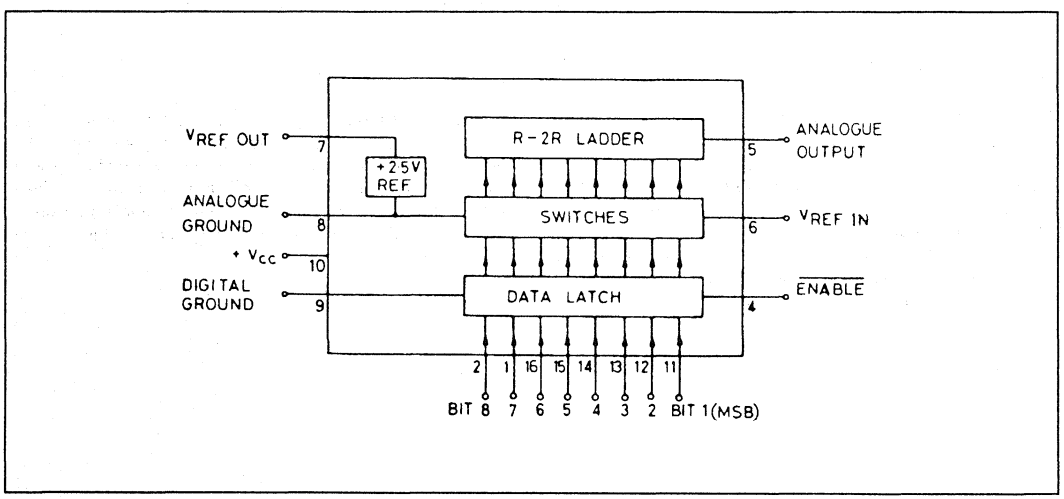


Fig.3 ZN428 logic diagram

The ZN428 D-A converter

The ZN428 is a monolithic 8-bit D-A converter (DAC), with input latches to facilitate updating from a microprocessor data bus. The latch is transparent when the ENABLE ($\overline{EN}$) input is at a logic '0' and the data is held when EN is taken to a logic '1'.

The ZN428 features single + 5V supply requirements, fast 800ns settling time and is guaranteed monotonic over its full temperature range. It contains a pin optional 2. 5V precision bandgap reference identical to the ZN427. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\,IN}$ by transistor logic switches especially designed for low offset voltage (< 1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network, the nominal range being 0-$V_{REF\,IN}$ volts with a 4kΩ resistance. Other output ranges can readily be obtained by the use of an external amplifier allowing complete versatility in its application.

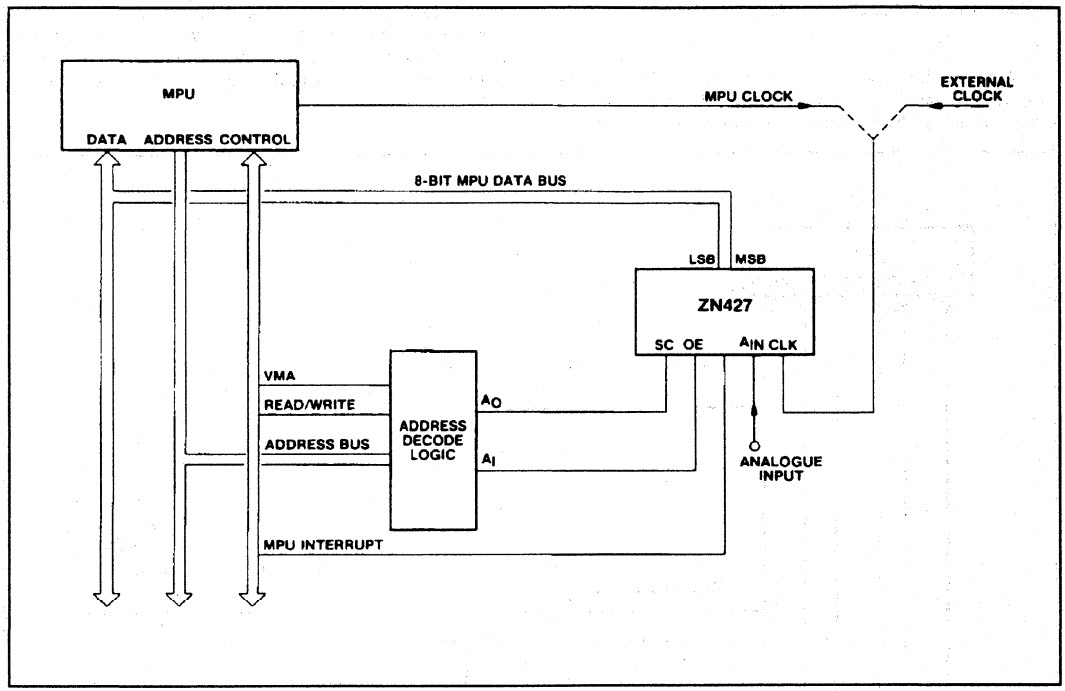


Fig.4 ZN427 microprocessor bus interface

The ZN427 microprocessor bus interface

Peripheral devices can be connected to a microprocessor system by two basic methods. The first and usually the simplest from the point of view of design effort required is to use a peripheral interface I/O device usually found as a support IC in most of the MPU families. With this method the peripheral device is simply connected to the I/O lines of the peripheral interface device and generally no considerations have to be made in terms of bus buffering, bus timing or address decoding.

The second method is to connect the peripheral device directly to the microprocessor data bus. This method is termed 'memory mapped I/O' which as its name implies is to make each peripheral I/O function appear to the MPU as a normal memory location, in which case the MPU cannot tell whether it is addressing memory or I/O. This allows the full set of memory reference instructions to be used for I/O data transfer, but it does imply that the peripheral device must be capable of responding at least as fast as the MPU memory and hence it should be compatible with the bus timing characteristics. The disadvantages of memory mapped I/O are that it usually requires additional address decoding logic, and also, since the I/O device will be addressed as memory, then there will consequently be fewer addresses available for actual memory.

It is with this second method of interfacing that this application note is primarily concerned.

A variation of memory mapped I/O, sometimes known as "I/O mapped I/O" is available on some MPUs which overcomes the last disadvantage referred to. This allows a defined range of memory address also to be used for I/O by means of separate I/O instructions. A special control line is required to inform the memory and I/O device whether the address of the current READ or WRITE cycle refers to memory or to I/O. This technique however does restrict the freedom of the programmer to the use of these I/O instructions which normally only operate on data in the microprocessor accumulator.

Fig. 4 shows the basic memory mapped interface for the ZN427 where the 8 binary outputs of the ADC are connected directly to the MPU data bus. The control inputs, START CONVERSION and OUTPUT ENABLE are shown driven from address decoder logic, the function of which is to drive the appropriate input when the address which has been allocated to that particular input is present on the address bus and the control bus signals indicate a valid memory read or write operation. Note that the level of address decode logic used must ensure that the three-state data outputs of the ZN427 are disabled at all times except when the actual ADC data is required on the data bus, otherwise bus contention problems may occur with other devices using the bus. The END OF CONVERSION output can be connected directly to an MPU interrupt to signal the completion of the conversion cycle by the ADC. The ZN427 clock can be driven either from the MPU clock or from an external source. If however the former method is employed, it may simplify the design of the interface with regard to the timing criteria of SC input. (This is covered in more detail later.)

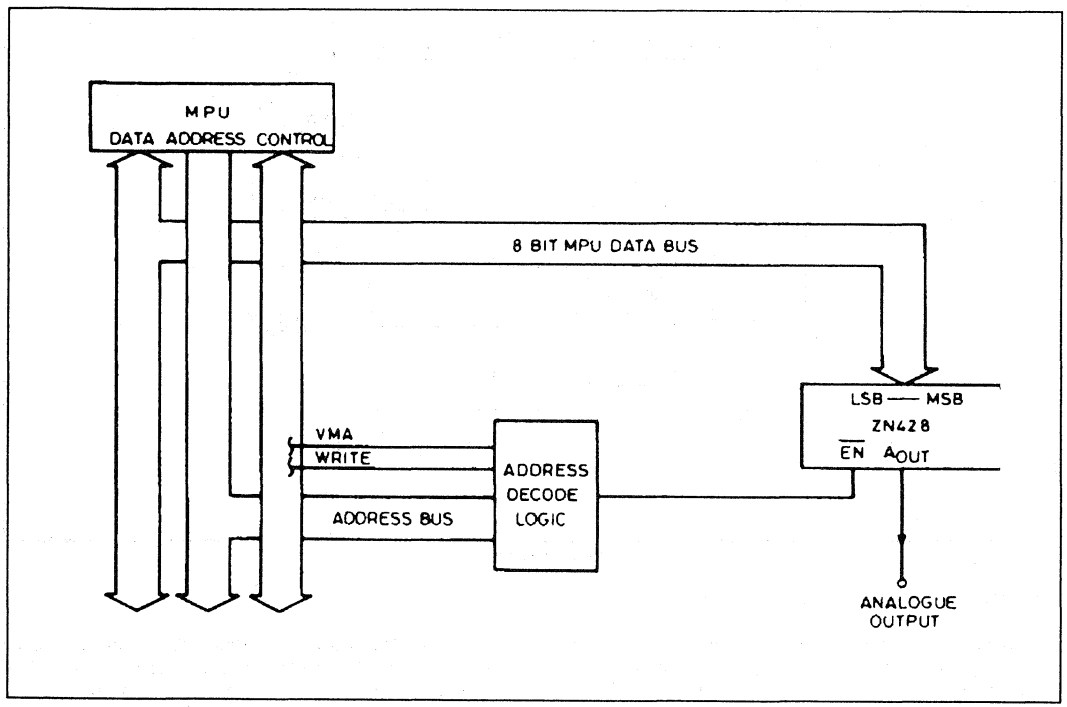


Fig.5 ZN428 microprocessor bus interface

The ZN428 data inputs can be directly connected to an MPU data bus when in the memory mapped configuration, this is illustrated in Fig. 5. For this application the address decode logic has only to generate the $\overline{\text{ENABLE}}$ signal for the DAC. This is accomplished by gating the MPU WRITE signal with the decoded address signal in order that when a memory write instruction to the DAC address location is executed, then a negative going pulse is applied to the EN input which will transfer the binary code from the data bus to the ZN428 input latches.

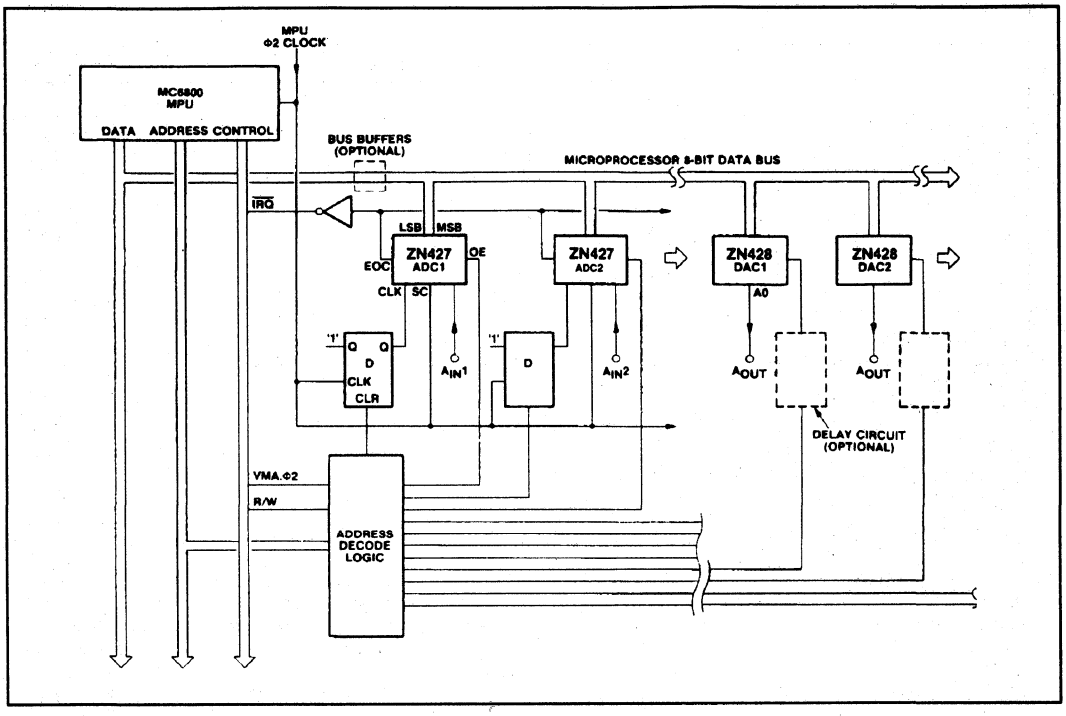


Fig.6 ZN427/ZN428 to 6800 bus interface

Interfacing to the 6800 bus

With the ability of the ZN427 and ZN428 to be bus compatible it is possible to produce a complete analog I/O system, specifically configured to the designer's own requirements with the converters connected directly to the MPU data bus. Such a system is illustrated in Fig. 6 built around a 6800 MPU.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL logic the 6800 requires only a single + 5 volt power supply, it features a set of 72 instructions with 7 addressing modes and full 65K byte memory addressing capability. The microprocessor communicates with its external memory and all I/O peripherals over an 8-bit bi-directional data bus and a 16-bit address bus. (Full data on the 6800 microprocessor is readily available from its manufacturers and their distributors).

The number of ZN427s and ZN428s which can be hung on the data bus is not limited, the only restrictions being the total load presented to the data bus and the number of decoded address lines available. The loading and drive characteristics of the converters are summarised in Table 1. Optional bi-directional bus buffers are shown in the diagram. these can be used to expand the system. Use of these will be dependent on the total number of converters used, other peripheral and memory devices on the data bus, and other loading factors such as physical length of bus required.

ZN427		ZN428	
Parameter	Specification	Parameter	Specification
I_{IL}	-5μA max.	I_{IL}	-5μA max.
I_{IH}	15μA max.	I_{IH}	20μA max.
I_{IH} (Clock)	30μA max.		
I_{OL}	1.6mA min.		
I_{OH}	-100μA min.		
I_{OHX} (Off state leakage)	2μA max.		

(NOTE: Current specified at 0.4V and 2.4V).

Table.1 Loading characteristics of the ZN427 and ZN428

The level of address decoding will depend on the overall MPU system design. This can range from merely using the upper address lines directly with no hardware decoding to provide the control lines for the converters - which rapidly depletes the number of address locations available for memory, through to full address decoding where all 65K addresses can be utilised. The address decode hardware can usually be produced from a few TTL gates in association with an address decoder I/C such as the 74154. In order to avoid addressing problems it is necessary on the 6800 to qualify the decoded address with the Valid Memory Address (VMA) and ø2 clock signals. The READ/WRITE control line can also be utilised to permit a single decoded address to control each ZN427, i.e. WRITE instruction to the specific address would generate the SC signal and a READ instruction of the same address would enable the converter outputs and read the data. The function of the 'D' type flip-flops shown in the diagram is to ensure that the timing criteria of the SC pulse are met. The requirements for this are that the SC pulse should start at least 1.5μs before the first active (negative going) clock edge after the SC pulse, and that the trailing edge of the SC pulse must not occur within ±200ns of a negative going clock edge, see Fig. 2. By careful design of the address decode logic when deriving the converter clock from the MPU it is possible to produce the correct timing for the SC pulse and to dispense with the 'D' type flip-flops.

The other advantages of using the MPU clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of the MPU machine cycles. Again with reference to Fig.2 it can be seen that the conversion cycle always takes less than 10 clock cycles after the end of the SC pulse. Hence instead of using the EOC output to drive MPU $\overline{IRQ}$ input a simple programme delay loop can be substituted. Note that the EOC outputs of up to five ZN427s can be 'wire-anded' together to form a common interrupt line.

The clock frequency of the standard 6800 is 1MHz which can be used directly to drive the ZN427s if a small loss of accuracy can be tolerated. The 6871B MPU clock generator is produced in a version with a 614.4kHz clock signal. This is only marginally higher than the specified ZN427 clock rate of 600 kHz and the ø2 TTL output of this can be used directly for the converter clock if full accuracy is essential.

With the 6800 it may be necessary to delay the decoded address enable signal to the ZN428 converters if glitch free operation is desired. This is due to the fact that during a write operation on the 6800 the address and address qualifying control signals become valid before the data bus signals are valid, thereby enabling the DAC before the data is established on the data bus.

The analog output can be taken directly from the ZN428 output pin which provides a nominal output range from zero volts to $V_{REF\ IN}$ with a 4kΩ output resistance. For most applications higher output ranges or drive will be required. This can easily be accomplished on the ZN428 by the addition of an external buffer amplifier which can be chosen for the specific characteristics required. The ZN428 is provided with separate analog and digital ground pins which should normally be connected together close to the I.C. For noisy systems or environments an improvement may be obtained, in some cases, by running the two ground pins to supply ground separately, taking the analog ground of each ZN428 to a single common earth point in the system away from the sources of high noise such as clock oscillators, digital buses, etc. Note that the maximum voltage between the analog and digital ground pins should not be allowed to exceed 200mA.

Both the ZN427 and ZN428 contain a nominal 2.5V internal bandgap voltage reference. Use of this on chip reference is pin optional to retain flexibility and an external reference can be substituted which allows ratiometric operation over the range of typically 1.5 to 3V. The on-chip reference is capable of supplying the reference voltage for up to five ZN427s and ZN428s. This useful feature saves power, discrete components and gives excellent gain tracking between the converters in a system. The tail current for the comparator on the ZN427 is derived via an external resistor from a negative supply. By suitable choice any negative supply of between - 3 and - 30 volts may be used. Since the negative current is only of the order of 65 microamps per converter then for applications where only a positive supply is available a simple diode pump circuit can be used .

With a memory mapped interface the full range of memory reference instructions are available to the programmer in order to control the converters, and programming becomes a relatively simple matter of reading and writing data to the addresses allocated to the converters. For example, for the ADCs a conversion cycle could be initiated by a store accumulator command (STA A) to address location ALOC 1, where ALOC 1 is the address of the ADC to be accessed. The contents of the MPU accumulator 'A' at this time are irrelevant since we only want to generate a memory write cycle to produce a pulse at the SC input. Now one can either enable the MPU interrupt and wait for the EOC output to generate an interrupt signal if this is the method used or alternatively a simple programme delay loop can be entered to produce a delay of ≥9 converter clock cycles (i.e. ≥15µs if a 600kHz clock is used). Upon receipt of an interrupt or completion of the delay a load accumulator command (LDA A) can be performed on address ALOC 1. This will read the binary data from the converter into the MPU accumulator 'A'. It is even simpler to programme the DACs. All one needs to do is to load the value to be outputted to say accumulator 'A' in binary format. A store accumulator command (STA A) is then programmed to address location ALOC 2, where ALOC 2 is the address allocated to the DAC. Upon execution of this the data will be transferred from the accumulator via the data bus to the DAC input latches and be present at the DAC output in analog form within 1.25 microseconds of the enable pulse.

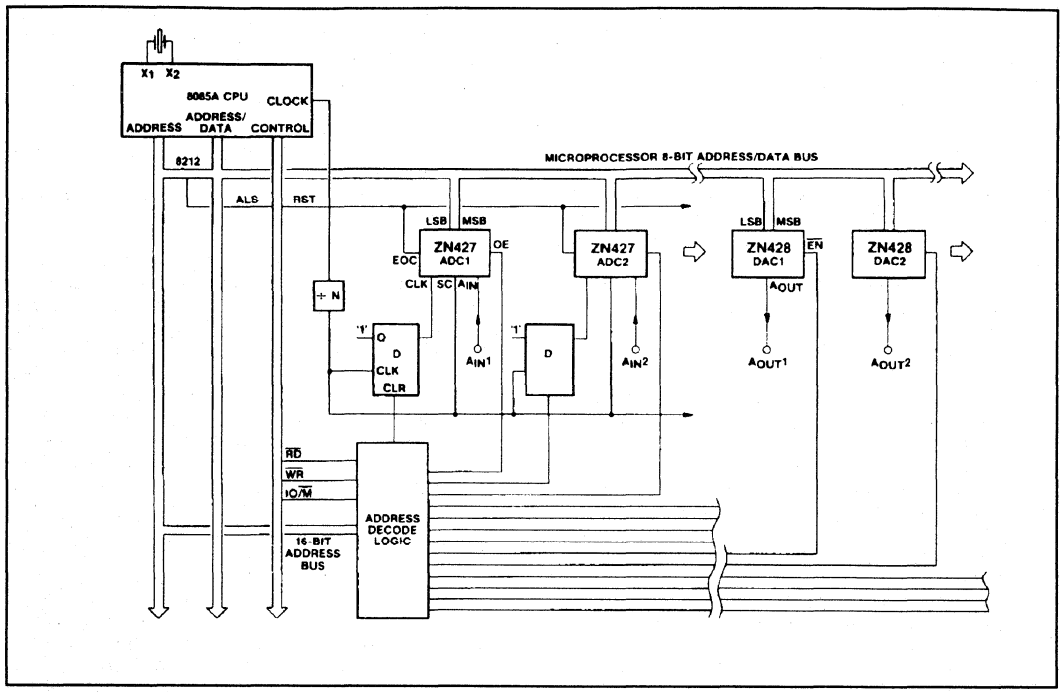


Fig.7 ZN427/ZN428 to 8085 bus interface

Interfacing to the 8085 bus

An analog I/O system for the 8085A microprocessor is shown in Fig.7. This is similar to the 6800 system but the following exceptions should be noted.

The 8085A is another popular 8-bit microprocessor. However, unlike the 6800 this MPU uses a multiplexed data bus whereby the lower 8 address bits AO-A7 are time shared with the 8 data bits. The address bus contains the upper 8 bits A8-A15. If the lower 8 address bits are to be used for address decoding then it is preferable to de-multiplex the bus using an 8 bit latch, such as the 8212, strobed with the address latch enable (ALE) signal from the MPU. The 8085A offers either memory mapped I/O or I/O mapped I/O by means of a separate control line (IO/$\overline{M}$). This allows use of the 'IN' and 'OUT' instructions to control I/O data transfers and the retention of the full 65K memory locations. If using this method then it is unnecessary to de-multiplex the address/data bus, since only the lower 256 addresses are used for I/O transfers, and the address in the lower 8 bits is mirrored into the upper 8 address bits during this operation.

The standard 8085 clock frequency is 3MHz.

Hence it is necessary to divide the output from the 8085A CLK output pin down by a factor of at least 4 to produce an acceptable ZN427 clock. Because of this it is more difficult to synchronise the decoded address signals with the ZN427 clock in order to meet the start pulse timing criteria, and one will usually have to incorporate the 'D' type flip-flops as indicated to generate the SC pulse.

Note that with the 8085A the common EOC line can be used directly to generate an interrupt via one of the 3 restart interrupt inputs. The decoded address input to the ZN428's EN input can also be used without any additional delay since, with this MPU the bus data is valid during the time that the WRITE signal is established.

Again programming is very straightforward. With a memory mapped I/O configuration the data transfer commands - move (MOV), load (LDA) and store (STA) can be used to control data transfers between the converters and the MPU. If an I/O mapped I/O configuration is adopted then the input (IN) and output (OUT) commands are used to transfer data between MPU accumulator and the converters.

Summary

The analog I/O systems described in this report are intended only as a guide to illustrate to design engineers the ease and versatility with which these two converters can be used to produce analog I/O channels for popular 8-bit microprocessors. As a result of the low cost, low external component count and flexibility of these converters, designs based on the 'one converter per channel concept' will be both a practical and economical solution to microprocessor data acquisition problems. This approach should find many new applications in areas which have previously been limited by the necessary usage of traditional data acquisition methods involving a single high cost hybrid ADC utilising sample and hold and multichannel multiplexing techniques .

Microprocessor Interfacing using the ZN427/ZN428 Data Converters

AN192 - 2.2

Conventional analog I/O systems for Microprocessors are generally high accuracy, high cost, hybrid module/PC board assemblies, available in only one fixed configuration ot I/O channels (i.e.16 Input and 2 Output channels). This applicatlon note describes how a low cost analog I/O system may be produced for the 6800 microprocessor using GEC Plessey Semiconductors ZN427 A-D and ZN428 D-A converters with the 6820/6821 peripheral interface adaptor (PIA) IC. This combination produces a versatile system which can be configured to the designer s particular I/O requirements and which can also be expanded without major modifications to the hardware. The advantages of interfacing to the microprocessor via the PIA are that It provides a simple easily expandable system without additional address decoding and line bufferlng hardware, and it also simplifies timing problems associated with a direct bus interface.

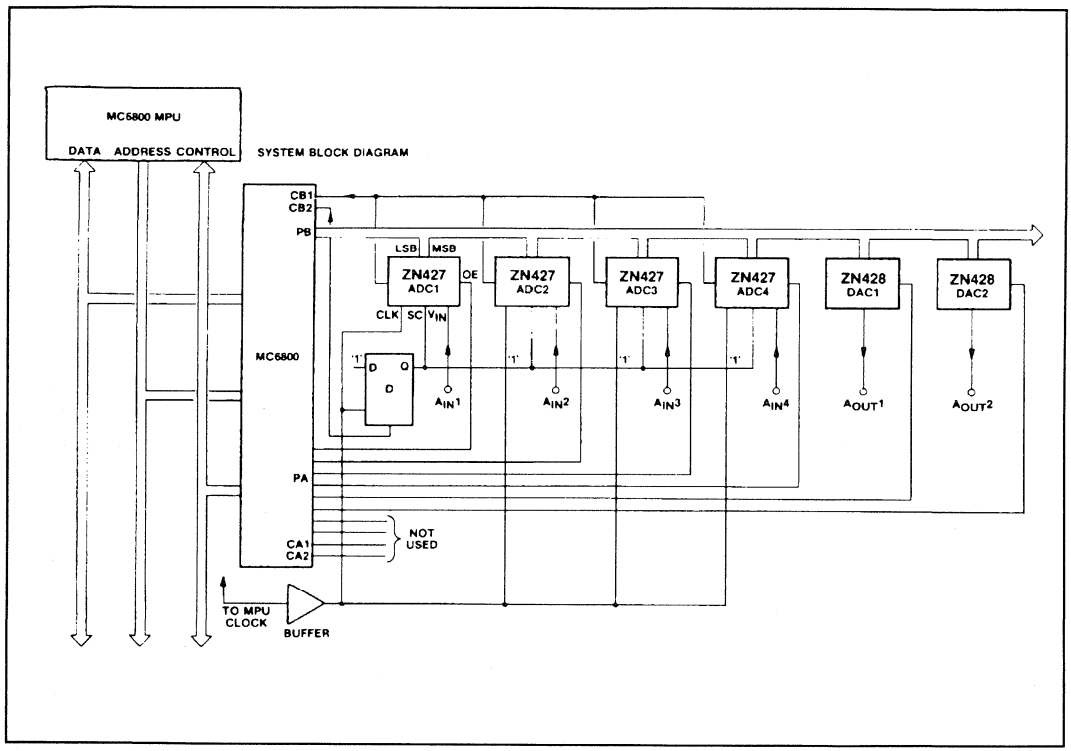


Fig.1 System block diagram

The ZN427 A-D converter

The ZN427 is an 8-bit, successive approximation A-D converter. It features fast 15µs conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D-A converter, a 2. 5V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.

Operation of the ZN427 is best described with reference to the timing diagram, Fig.3. Conversion is initiated by a START CONVERT (SC) pulse which can be applied asynchronously with respect to the ZN427 clock, providing the following criteria are met.

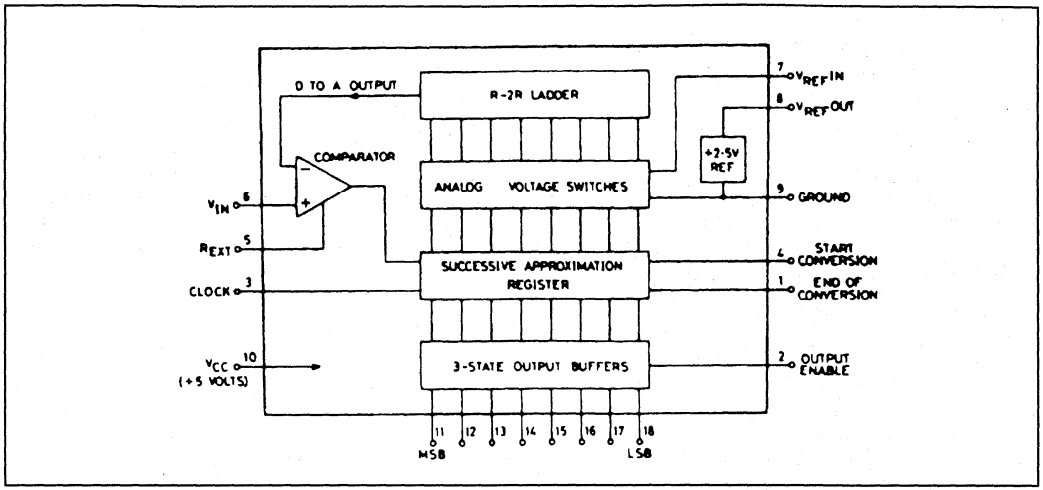


Fig.2 ZN427 logic diagram

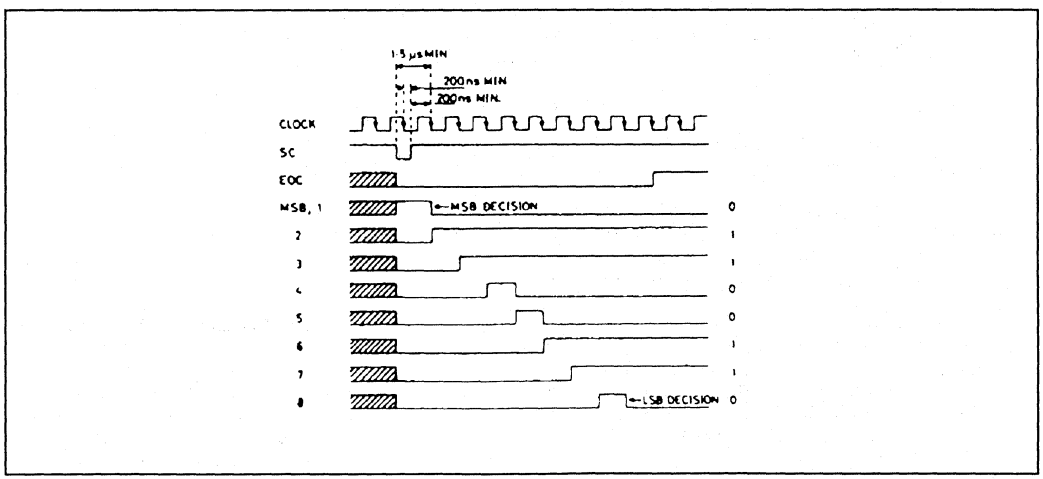


Fig.3 Timing diagram

1. The leading edge of the SC-pulse should precede the first active (negative going) edge of the clock (after the trailing edge of the SC pulse) by at least 1.5µs to allow for MSB setting.

2. The trailing edge of the SC pulse must not occur within ±200ns of a negative going edge of the clock.

3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse. Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D-A converter of $V_{REF\ IN/2}$.

This value is compared with the input voltage V_{IN}, and a decision is made on the first negative clock edge to set the MSB to 0 if $V_{REF\ IN/2} > V_{IN}$, or else to keep it at '1', Bit 2 is switched to '1' on the same clock edge, and on the next edge a decision is made about Bit 2, again by comparing the D-A output with V_{IN}. This process is repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is a valid representation of V_{IN}. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is an '0' and are enabled when the OE input is taken to '1'.

The ZN428 D-A ocnverter

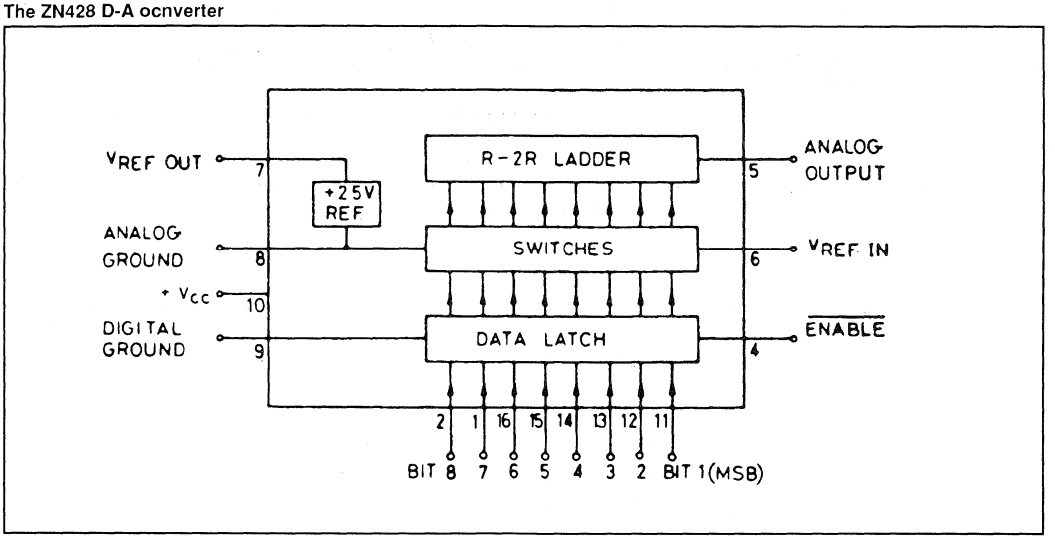


Fig.4 Logic diagram

The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when $\overline{\text{ENABLE}}$ is at logic '0' and the data is held when $\overline{\text{ENABLE}}$ is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800ns settling time and is guaranteed monotonic over the full operating range. It also contains a 2. 5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0V to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The 6800 microprocessor system

It is assumed that the reader is fully conversant with the 6800 microprocessor family, information on which can be found in the Motorola M6800 microprocessor applications manual, so only a brief description is given here.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL the 6800 requires only a single + 5 volt power supply, it features an instruction set of 72 instructions with 7 addressing modes and full 65k byte memory addressing capability. The microprocessor communications with its external memory and all I/O devices via an 8-bit bi-directional data bus and a 16-bit address bus.

The 6820/21 peripheral interface adaption (PIA) provides a flexible means of interfacing byte-orientated peripherals to the microprocessor, through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed to act either as an input or output, and each of the four control/ interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface .

The analog I/O interface

The system described in this application note provides 4 analog input and 2 analog output channels - see the system block diagram Fig. 1 and the detailed circuit diagram Fig. 5. Other configurations can easily be produced-these are discussed later in this note.

The peripheral data lines PB0-PB7 of the PIA are connected to the binary data outputs of the ZN427s and the data inputs of the ZN428s to produce a common 8-bit data bus for the converters. Peripheral lines PA0-PA5 are programmed as OUTPUTS and provide individual OUTPUT ENABLE AND $\overline{\text{ENABLE}}$ signals for the ZN427 and ZN428 respectively. A common, simultaneous START CONVERT signal for the ZN427s is produced from the CB2 control line program in the SET/ RESET output mode and used in conjunction with a 'D' type flip-flop. The END OF CONVERT outputs from the ZN427s are commoned together and drive the CB1 input of the PIA which can be programmed to generate a microprocessor interrupt signal. In this system configuration, the peripheral lines PA6, PA7 and the control lines CA1, CA2 are not used.

The ZN427 clock signal can be generated either asynchronously from an external source or from the microprocessor clock. If using the MC6871 B microprocessor clock device (as supplied with the Motorola MEK6800D2 evaluation kit), which produces a 614.4kHz clock signal, then the Ø2 TTL output of this can be used directly. Note that the maximum lock frequency of the ZN427 is specified as 600kHz, although the device will function up to greater than 1 MHz, but at reduced accuracy due mainly to the response time of the comparator. Therefore, if using a microprocessor with a clock frequency greater than 600kHz. then this can either be divided down to less than 600kHz, or it may be used directly up to approximately IMHz if some loss of accuracy can be tolerated. The advantage of using the microprocessor clock over an external clock is that it allows an accurate calculation of the conversion time to be made in terms of the microprocessor machine cycles eliminating the need to use microprocessor interrupts.

The START CONVERT pulse is generated using a 'D' type flip-flop (1/2 SN74L74) in order to meet the timing requirements discussed earlier. A conversion cycle is initiated by outputting a logic '0' followed by a logic '1' from the CB2 line of the PIA. This drives the CLEAR input of the 'D' type and sets the START CONVERT (SC) input of each 427 to a logic '0' via the Q output. The first positive going clock edge after the CLEAR input is returned to a logic '1 ' will clock the 'D' type and set the SC input of each ZN427 at a '1 ' allowing the conversion cycle to proceed. Note that while the SC input of the ZN427 is at a logic '0' level the MSB output will be driven to a logic '1 ' and all other data outputs to a logic '0' and the conversion cycle will be held. On the 9th negative clock edge after the START pulse the END OF CONVERSION outputs will go to a logic '1' signifying the end of the conversion cycle. This can be detected by programming the PIA to set the microprocessor interrupt input on the positive going edge of the CBI control line. The EOC outputs of up to four

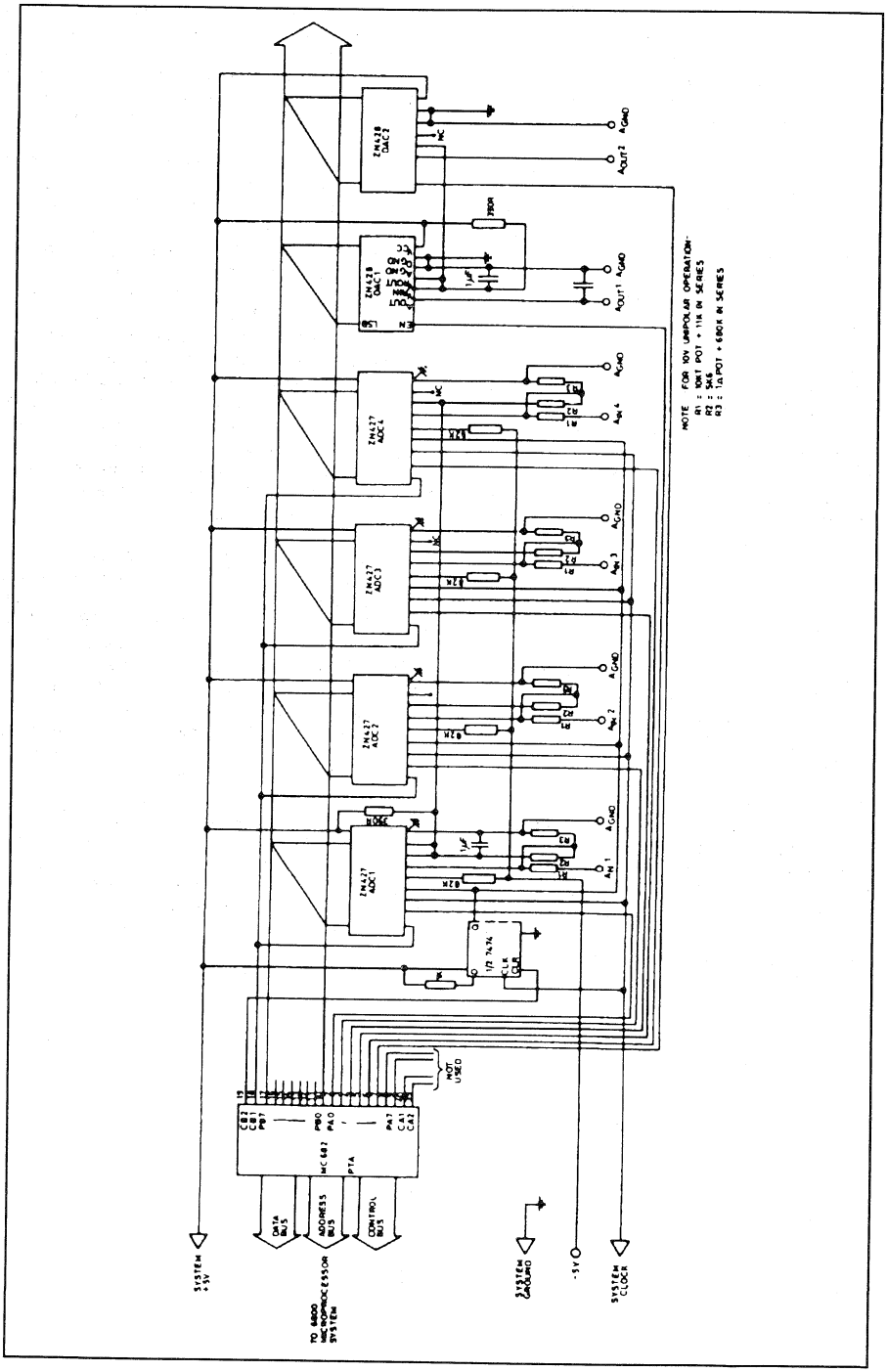

ZN438 DAC2
ZN438 DAC1
ZN427 ADC4
ZN427 ADC3
ZN427 ADC2
ZN427 ADC1
1/2 74LS74
MC 6821
SYSTEM +5V
TO 6800 MICROPROCESSOR SYSTEM
DATA BUS
ADDRESS BUS
CONTROL BUS
SYSTEM GROUND
-5V
SYSTEM CLOCK
NOTE: FOR 10V UNIPOLAR OPERATION:
R1 = 50KT POT + 11K IN SERIES
R2 = 5KT POT
R3 = 10 POT + 680R IN SERIES

Fig.5

ZN427s can be 'wire-or'd' together to produce a common interrupt line as shown in Fig. 5. Alternatively, if using the microprocessor clock (at up to 1MHz), then the EOC output will always occur within 10 microprocessor machine cycles after the instruction setting the CB2 control line back to a logic '1'. A suitable fixed delay can therefore be built into the program to allow for the conversion time.

The binary output data of each ADC can be read by programming the peripheral lines PB0-PB7 as INPUTS and loading the data onto the converter bus by outputting a logic '1 ' on the appropriate PA peripheral line in order to enable the 3-state output buffers of the ADC. A microprocessor read instruction on the PIA peripheral register 'B' will then transfer the data to the microprocessor. Obviously the program should be so arranged that, in order to avoid bus connection problems, only one ADC is enabled at any one time.

The circuit diagram Fig. 5 shows the ZN427s connected for a unipolar input range of 0 to + 10 volts. Other ranges, e.g. ±5V, ±10V and ±5V, can readily be obtained by using a simple resistor network as shown in the ZN427 data sheet.

The negative supply shown for the ZN427 is from - 5 volts through an 82kΩ resistor. By suitable choice of resistor value any negative supply between -3 and -30 volts may be used. For applications where only a single + 5 volt supply is available, a simple diode pump circuit can be used to generate the negative supply. Further information on the negative supply and a diode pump circuit suitable for up to 5 ZN427s is shown in the data sheet.

Data is output from the system by programming the peripheral data lines PB0-PB7 as OUTPUTS and wiring the binary data from the microprocessor into the PIA peripheral register 'B'. The ENABLE input of the relevant ZN428 is driven to a logic '0' and back to logic '1' via the appropriate PA peripheral line, which will transfer the data from the converter bus to the input data latches of the ZN428. Again the programmer must ensure during an output data transfer that all the ZN427s and the other ZN428 are disabled.

The analog outputs of the ZN428 are shown, taken directly from pins 5 and 8 which will provide an output range from 0 volts to $V_{REF\ IN}$ through a 4kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any "glitches" which may be present. The value of this capacitor depends on the system noise and the response time required, however for the minimum specified settling time it should not be greater than 100pF. An output buffer amplifier was omitted from the ZN428 design in order to allow optimum settling time, flexibility and lowest cost. Both unipolar and bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate analog and digital ground pins. These can normally be connected together close to the device and taken to signal ground. However for noisy systems or environments it may be advisable to keep the analog ground pins for each individual ZN428 separate from the digital ground pin, and to connect each analog ground to a single common earth point in the system away from sources of digital noise such as clock oscillators, digital buses. etc. The analog output ground line or terminal should also be taken direct to this common earth point. (Note: The maximum voltage between analog and digital grounds is limited to 200mV.)

Common reference voltage can be provided by connecting the $V_{REF\ OUT}$ pin of one converter to the $V_{REF\ IN}$ pins of up to five converters (i.e. either ZN427s or ZN428s). This useful feature saves power and gives excellent gain tracking between converters. Fig. 5 shows the four ZN427s driven from one internal reference and the two ZN428s from another.

Note that in this application the dynamic characteristic of the ZN427/428 (i.e. enable/ disable delay times, etc.) should not present any problems since they are much less than the microprocessor instruction execution times and need not be considered in the programming.

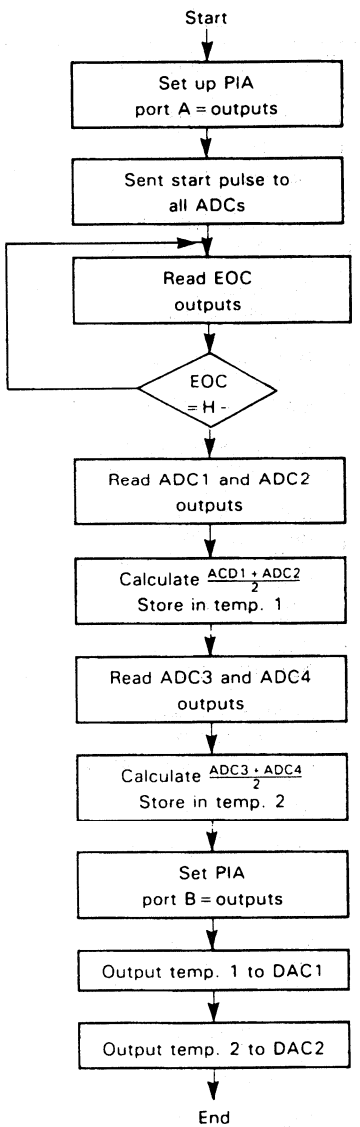
Program example

A simple program which illustrates the ease of controlling the ZN427/ZN428 with the PIA is shown with the flow diagram, Fig. 6. The object of the program is to read the analog voltage inputs to ADCs 1 and 2, calculate the mean value and output this on DAC1. A similar operation is performed on the inputs of ADCs 3 and 4 and output on DAC2.

It is assumed that the PIA has been reset which has the effect of zeroing all the PIA registers. This sets all the peripheral and control lines as INPUTS and disables the interrupts. Initially the index register is loaded with the PIA base address in order that the indexed addressing mode can be used throughout the program to address the PIA. The peripheral lines PAO-PA7 are programmed as OUTPUTS and the control registers set so that control line CB2 operates in the SET/RESET output mode and the interrupt flag bit CRB-7 is set with a positive going edge on control line CB1. All the converters are disabled by outputting 30H and the PIA lines which sets the OUTPUT ENABLE inputs of the ZN427s to a logic '0' and the $\overline{\text{ENABLE}}$ inputs of the ZN428s to a logic '1'. A dummy read is made of the B data register to clear the interrupt flag bit CRB-7.

A START signal is then generated via control line CB2 by toggling bit CRB-3 in control register B. The end of the conversion cycle is detected by testing the interrupt flag bit CRB-7 and looping at this point in the program until it goes to a '1'. (Note: The microprocessor interrupt request lines IRQA, IRQB are disabled.) The output of ADC1 is now read by driving peripheral line PAO to a logic '1', and the data is stored in the microprocessor accumulator B, ADC2 is read in a similar way by setting PA1 line to a logic '1 ' and storing the data in accumulator A. The mean value of the readings is found by adding the accumulators and rotating the result right one bit through carry, this is equivalent to dividing by 2. The result is saved in the memory location labelled 'TEMP 1'. The process is repeated on ADC3 and ADC4, enabling the ADC outputs by setting lines PA2 and PA3 in turn to a logic '1', and storing the computed result in location 'TEMP 2'.

The data direction register B is now accessed and the peripheral line PBO-PB7 changed to OUTPUTS. The data stored in 'TEMP 1 ' is outputted onto the converter bus and DAC 1 enabled by toggling line PA4 in a logic 1-0-1 sequence, which will transfer the binary data from the bus to the DAC input latches and hence to the analog output. A similar sequence is performed on DAC2 with the data from 'TEMP 2', using PA5 line to drive the $\overline{\text{ENABLE}}$ input. The program is terminated with a software interrupt SWI, returning to the monitor program.



PIA PORT ALLOCATIONS

PORT A

PA0	ADC1 OE input
PA1	ADC2 OE input
PA2	ADC3 OE input
PA3	ADC4 OE input
PA4	DAC1 $\overline{EN}$ input
PA5	DAC2 $\overline{EN}$ input
PA6	NOT USED
PA7	NOT USED

PORT B

PB0	BINARY DATA LSB
PB1	BINARY DATA LSB + 1
PB2	BINARY DATA LSB + 2
PB3	BINARY DATA LSB + 3
PB4	BINARY DATA LSB + 4
PB5	BINARY DATA LSB + 5
PB6	BINARY DATA LSB + 6
PB7	BINARY DATA MSB

CONTROL

CA1	NOT USED
CA2	NOT USED
CB1	COMMON EOC OUTPUT
CB2	COMMON START LINE

PIA ADDRESSES

8004	PERIPHERAL/DATA DIRECTION REG. A
8005	CONTROL REG. A
8006	PERIPHERAL/DATA DIRECTION REG. B
8007	CONTROL REG. B

Fig.6 Program flow diagram

6800/6820 I/O INTERFACE - PROGRAM EXAMPLE

Location	Object		Comment	Source statement
000	CE004		LDX 8804	Load PIA address to IX
3	86FF		LDA A FF	
5	A700		STA A 0, X	Set port A as outputs
7	863E		LDA A 3E	
9	A701		STA A 1, X	Set control reg. A
B	A703		STA A 3, X	Set control reg. B
D	8630		LDA A 30	
F	A700		STA A 0, X	Disable converters
11	A602		LDA A 2, X	Dummy read to clear flag
13	8636		LDA A 36	
15	A703		STA A 3, X	Set CB2 low to
17	863E		LDA A 3E	generate start pulse
19	A703		STA A 3, X	Set CB2 high
1B	A603	TEST	LDA A 3, X	Read control reg. B
1D	8580		BIT A 80	Test for CRB-7 high
1F	27FA		BEQ TEST	ie End of Conversion
21	8631		LDA A 3, 31	
23	A700		STA A 0, X	Enable ADC1 O/Ps
25	E602		LDA B 2, X	Read ADC1 O/P
27	8632		LDA A 32	
29	A700		STA A 0, X	Enable ADC2 O/Ps
2B	A602		LDA A 2, X	Read ADC2 O/P
2D	1B		ABS	Add ADC1 + ADC2 readings
2E	46		RORA	Divide by 2
2F	976E		STA A Temp. 1	Save in temp. 1
31	8634		LDA A 34	
33	A700		STA A 0, X	Enable ADC3 O/Ps
35	E602		LDA B 2, X	Read ADC3 O/P
37	8638		LDA A 38	
39	A700		STA A 0, X	Enable ADC4 O/Ps
3B	A602		LDA A 2, X	Read ADC4 O/P
3D	1B		ABA	Add ADC1 + ADC2 readings
3E	46		RORA	Divide by 2
3F	976F		STA A Temp. 2	Save in temp. 2
41	8630		LDA A 30	
43	A700		STA A 0, X	Disable ADC O/Ps
45	863A		LDA A 3A	
47	A703		STA A 3, X	
49	86FF		LDA A FF	
4B	A702		STA A 2, X	Set port B as output
4D	863E		LDA A 3E	
4F	A703		STA A 3, X	
51	966E		LDA A temp. 1	
53	A703		STA A 2, X	Put x Data on bus
55	8620		LDA A 20	
57	A700		STA A 0, X	Enable DAC1 I/Ps
59	C630		LDA B 30	
5B	E700		STA B 0, X	Disable DAC1 I/Ps
5D	966F		LDA A temp. 2	
5F	A702		STA A 2, X	Put y data on bus
61	8610		LDA A 10	
63	A700		STA A 0, X	Enable DAC2 I/Ps
65	E700		STA B 0, X	Disable DAC2 I/Ps
67	3F		SWI	End
006E	00		Temp. 1	x data
006F	00		Temp. 2	y data

Summary

The system described in this report is by no means restricted to the configuration shown. Provided that the drive capability of the system components is not exceeded, the number and configuration of ZN427s and ZN428s which can be employed is limited only by the I/O lines available from the PIA, hence providing the design engineer with a wide degree of freedom in producing the system that best fulfils his requirements.

The major loading and drive characteristics of the various system components are shown in Table 1. Buffer gates can be employed where necessary to expand the drive capability of the components such as when utilising a long bus with high capacitive loading. Note that the peripheral lines from side B are used for the converter bus since these present a high impedance when programmed as inputs. Also the 6821 PIA is preferred to the 6820 because this has a 2-TTL drive capability on both A and B side peripheral lines. As stated previously up to 4 ZN427 EOC outputs can be 'wire-or'd' together if using more than 4, then each group can be ANDed together using an SN7409 TTL gate to produce a single interrupt line.

If required separate START signals can be generated for each ZN427 hence allowing a microprocessor read of one ADC to be in progress while the other(s) are in a conversion cycle. However this configuration does require one peripheral line and one 'D' type flip-flop per START signal line. Since only one ZN427 or ZN428 should be enabled at any one time, then it is possible to incorporate one or more decoder types of IC such as the SN74154, 4 line to 16 line demultiplexer/ decoder in order to expand the system. This device could be connected with the 4 data inputs connected to 4 PA peripheral lines and the decoder enable input driven by CA2 line. Use of two such ICs would provide 32 output lines allowing an analog I/O system with a combination of up to 32 analog input and output channels to be produced.

As a result of the low converter cost, low external component count and flexibility of this type of system, designs based on using one converter per analog channel will be both a practical and economical solution to microprocessor data acquisition problems. This approach should find many new applications in areas which have previously been limited by the necessity of having to use the traditional data acquisition methods involving a single, high cost hybrid A-D converter utilising a sample/hold and multichannel multiplexing techniques.

MC6820	PA0 - PA7/CA2	PB0 - PB7/CB2	CA1/CB1
I_{IL} I_{IH} I_{OL} I_{OH}	-1.6mA max -100µA min 1.6mA min -100µA min	10µA max. 1.6mA min -100µA min	2.5µA max. (at V_{IN} = 0 to 5.25V)
MC6821			
I_{IL} I_{IH} I_{OL} I_{OH}	-2.4mA max -200µA min 3.2mA min -200µA min	10µA max. 3.2mA min -200µA min	2.5µA max. (at V_{IN} = 0 to 5.25V)
ZN427			
I_{IL} I_{IH} $I_{IH\ (Clock)}$ I_{OL} I_{OH} I_{OHX} (Off state leakage)	-5µA max 15µA max 30µA max 1.6mA min -100µA min 2µA max		
ZN428	All inputs		
I_{IL} I_{IH}	-5µA max 20µA max		

NOTE Currents specified at 0.4 and 2.4V unless otherwise stated

Table.1

A Serial Interface for the ZN427 A-D Converter

In many data acquisition applications it is advantageous to situate the A-D converter close to the transducer and to transmit the digital data in serial form back to the data collection centre of the system. The serial data link uses less conductors and provides better noise immunity than a parallel data bus. This application note describes a RS-232C compatible serial data interface for the ZN427 8-bit A-D converter using an industry standard 6402 UART. A simplified block diagram is shown in Fig. 1.

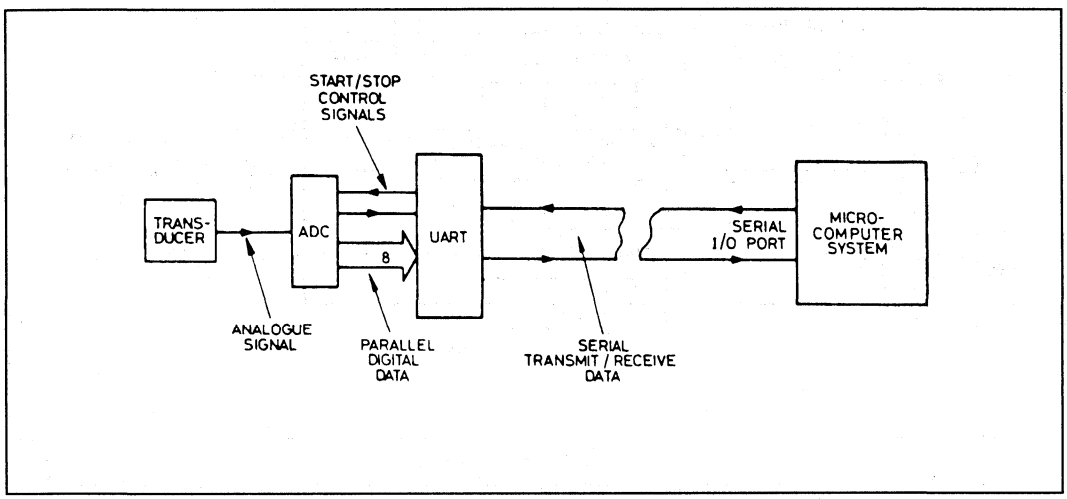


Fig.1 Serial data interface

In order to initiate a conversion cycle a character is transmitted by the microcomputer. Upon receipt of this character by the UART its DR (data received) output goes to a high level which generates a start pulse for the A-D converter triggering a conversion cycle. At the end of the cycle the EOC (lend of convert) output is used to load the converted data into the UART which performs a parallel to serial conversion and transmits the data back to the microcomputer.

The ZN427 is an 8 bit successive approximation A-D converter. It features three-state output buffers to permit bussing onto common data lines, fast 10μS conversion time and no missing codes over the full operating temperature range.

The ZN427 contains a voltage switching D-A converter, a fast comparator, successive approximation logic, three state output buffers and a 2.5V precision bandgap reference. A logic diagram of the converter is shown in Fig. 2. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a limiting resistor for the negative supply current. This will provide a nominal input voltage range of 0 to V_{REF}IN. Other input ranges both unipolar and bipolar can be obtained by connecting a simple resistor network to V_{IN} (pin 6) as illustrated in Figs. 3a and 3b. Further information on the ZN427 can be found in the data sheet

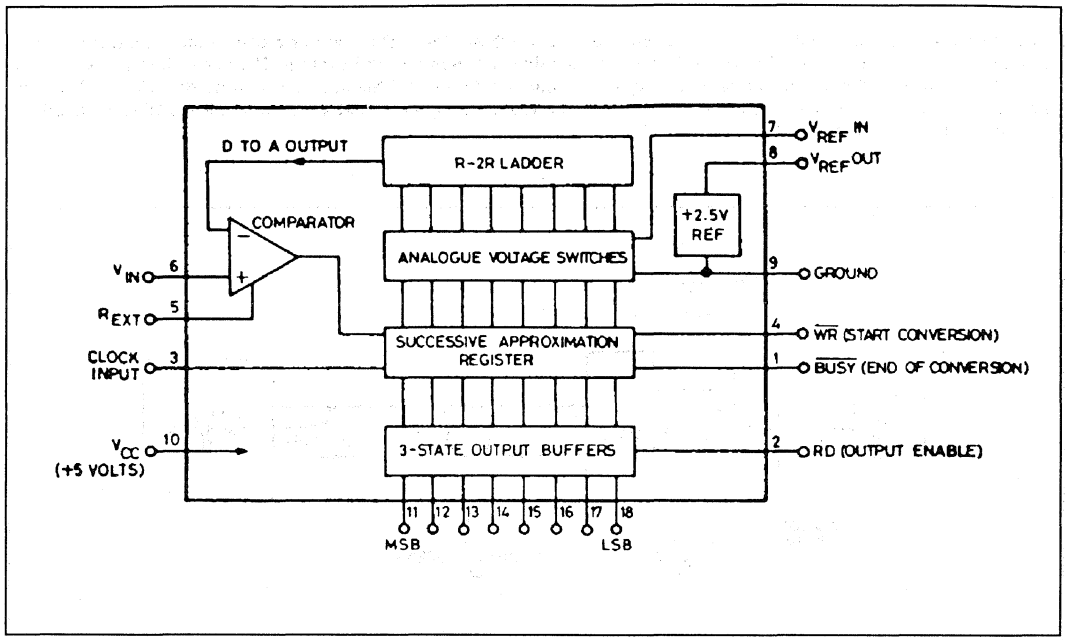


Fig.2 System diagram

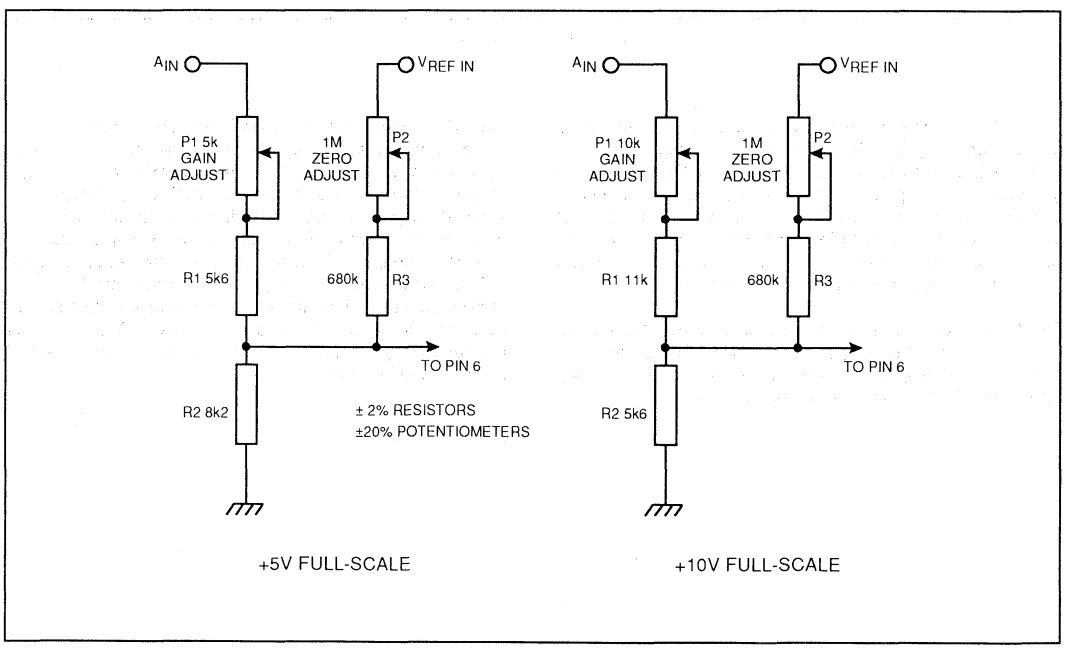


Fig.3a Unipolar operation - component values

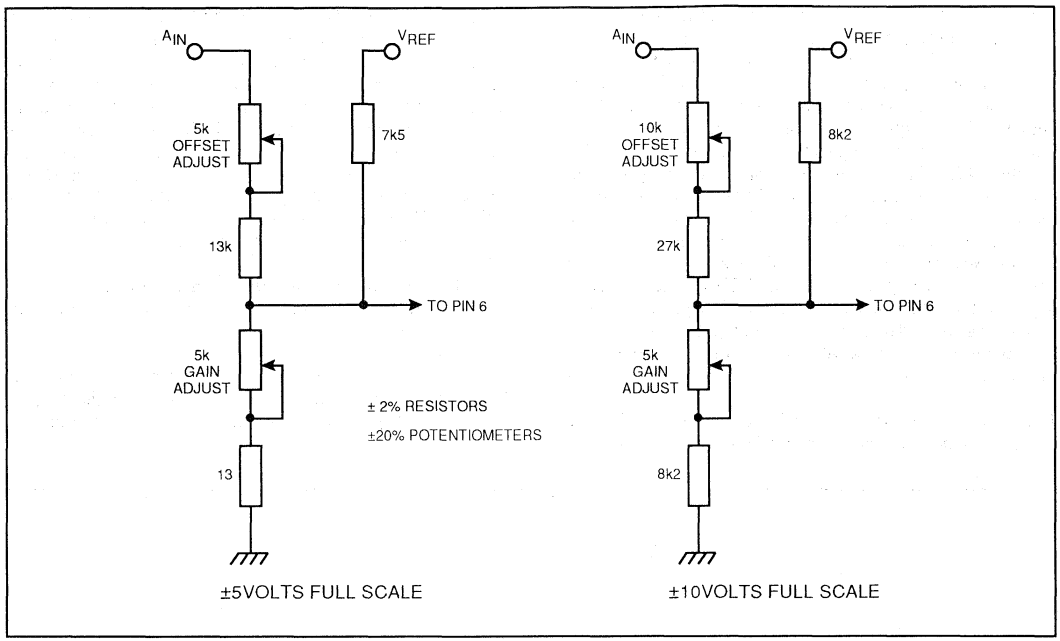


Fig.3b Bipolar operation - component values

A detailed circuit diagram of the converter interface is shown in Fig.4.

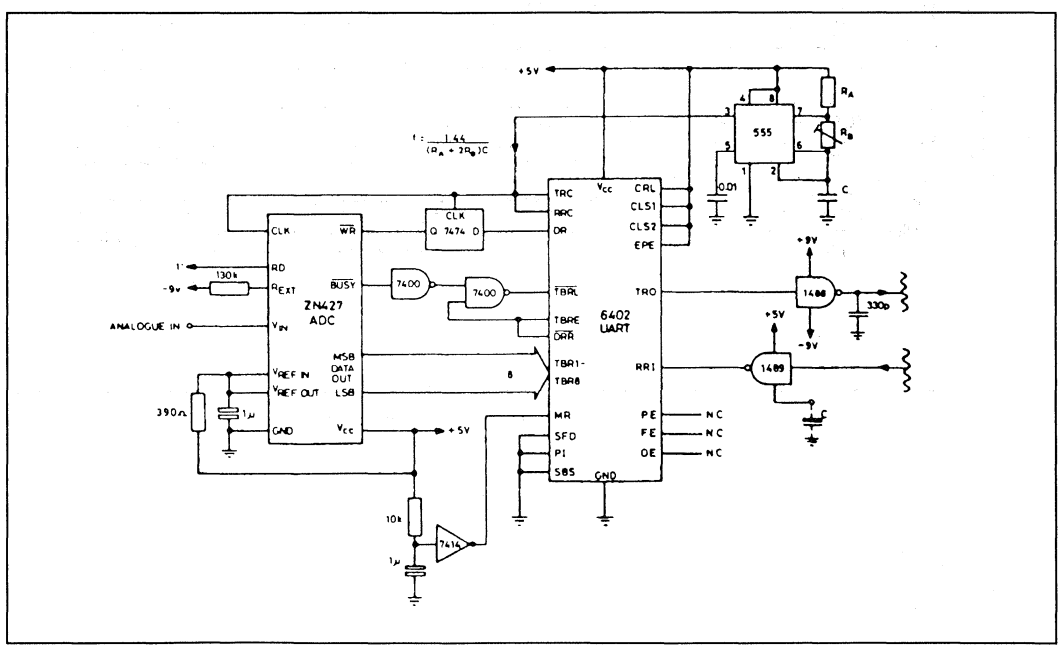


Fig.4 ZN427 UART interface

The DR output of the UART is connected to the 'D' input of the 7474 latch, the 'Q' output of which drives the $\overline{WR}$ (start convert) input of the ADC. The use of this ensures that the timing of the $\overline{WR}$ pulse with respect to the converter clock input is correct. On the ninth negative clock edge after the $\overline{WR}$ pulse the $\overline{BUSY}$ output goes to a high level signalling that the conversion cycle is complete. This low to high transition is used to load the data into the UART via the TBRL (transmitter buffer register load input). The signal is gated with the TBRE (transmitter buffer register empty) signal which holds the TBRL input high until the UART transfers the data to its transmitter register. If TBRL were allowed to return low before TBRE went high the converter data would be overwritten since the TBR (transmitter buffer register) is a transparent latch. The TBRE signal is also used to drive the DRR (data received reset) input which clears the DR output to a low level allowing another character to be received.

The waveforms associated with this operation are shown in Fig. 5. A simple oscillator using a 555 I.C. is shown which generates both the ADC clock and the transmit/receive clocks for the UART. The external clock is 16 times the data rate, the signal being divided internally by the UART. If a more stable data rate is an important factor then the 6403 UART, which is functionally similar but which uses a crystal oscillator as the timing source. may be substituted. In this case the ADC clock would still be generated by the 555 since it is not necessary for the converter and UART clocks to be synchronised. The UART control inputs CLS1, CLS2 (character length select); PI (parity inhibit); EPE (even parity enable); SBS (stop bit select) are hard wired for whatever data format is wanted.

The MR (master reset) input is driven via a 7414 Schmitt trigger I.C. from a R-C delay circuit to generate the recommended reset pulse after power up.

The 1488 and 1489 I.C's shown buffering the UART TRO (transmitter register output) and RRI (receive register input) pins are RS-232C compatible line drivers and receivers.

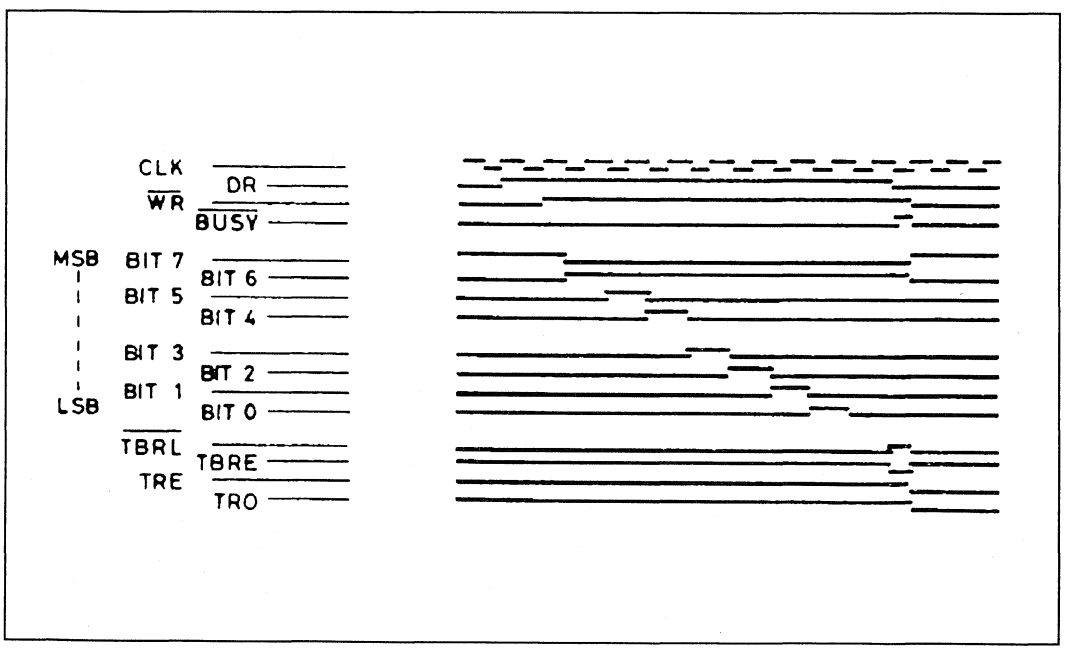


Fig.5 ZN427 UART interface waveforms

In some applications incorporating microcomputers with RS-232S serial I/O ports no additional interfacing at the data collection centre end will be necessary. However if only a parallel I/O port is provided than another UART to convert the serial data back to parallel will be needed. An interface for the PET microcomputer which connects to the Parallel User Port on connector J2 is shown in Fig. 6. This uses the eight I/O data lines. PAO-PA7 and two control lines CA1 and CB2 which originate from a 6522 versatile interface adaptor I.C. The data lines PAO-PA7 are connected to the RBR (receive buffer register) outputs of the UART. The CA1 input is driven by the UART DR output and is operated in the latched mode which stores the received data within the VIA on a positive transistion of this pin. In order to initiate a new reading from the ADC the remaining control pin CB2 is used. This is connected to the UART inputs DRR and TBRL. When programmed to produce a negative pulse the DR output is reset and a character is transmitted to the converter UART to start a new conversion cycle.

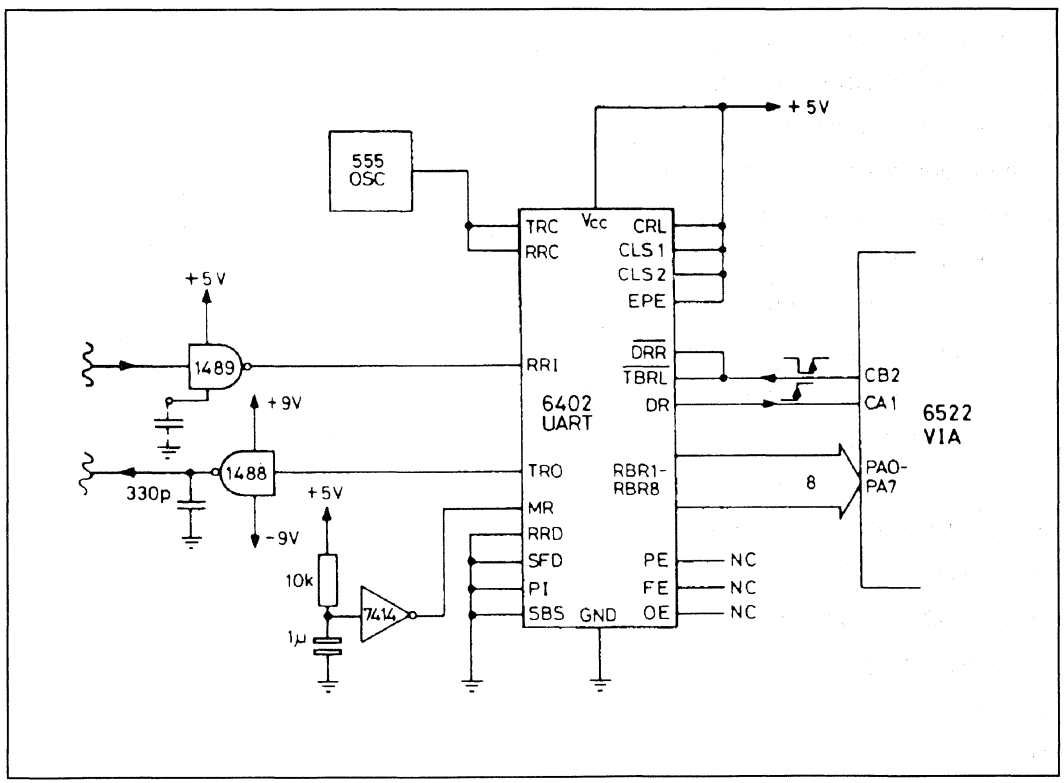


Fig.6 6522 VIA UART interface

A simple program example in PET basic is shown in the next page.

PROGRAM EXAMPLE

```
10  REM UART INTERFACE REV. 3
20  REM SET PORT A TO INPUTS
30  POKE 59459, 0
40  REM DISABLE CA1 INTERRUPT
50  POKE 59470, 2
60  REM SET PCR TO 111 XXXX 1
70  POKE 59468, PEEK (59468) OR 225
80  REM SET ACR TO XXX000X1
90  POKE 59467, PEEK (59467) AND 227 OR 1
100 REM CLEAR CA1 FLAG IN IFR
110 A = PEEK (59457)
120 REM PULSE CB2 LOW-HIGH
130 POKE 59468, PEEK (59468) AND 31 OR 192
140 POKE 59468, PEEK (59468• OR 225
150 REM WAIT FOR +TRAN ON CA1
160 REM TEST CA1 FLAG IN IFR
170 IF (PEEK (59469) AND 2) THEN 190
180 GOTO 170
190 REM READ IRA AND CLEAR CA1 FLAG
200 A = PEEK (59457)
210 PRINT A
220 GOTO 120
```

Initially the appropriate VIA internal registers are set up then a negative going pulse is produced on the CB2 pin. This starts a conversion sequence and when the new data is received the CA1 input goes high, latching the data in the VIA, and setting the CA1 flag bit in the interrupt flag register. This flag is tested by the program and when set the data is read and printed out. CB2 is again pulsed low and the sequence repeated.

For 6502 based microcomputer systems where all I/O lines of a 6522 VIA are available the CA2 pin can be used in the read handshake mode in place of the CB2 pin, simplifying the program. Also the status flag of the UART can be monitored by other I/O port lines for erro
checking purposes.

Interfacing the ZN427 A-D Converter with the 8085A

The growth of microprocessors has led to a demand for low cost, fast 8-bit A-D and D-A converters to interface between the real world of analog values and the digital world of the microprocessor. Converter systems have, until recently, been mainly high cost, multiplexed, sample and hold systems usually built around a 12-bit A-D converter. The system described in this report is a low cost, expandable, one converter per channel system, based on the ZN427 8-bit A-D converter interfaced directly to the I/O Ports of the 8155 2K bit static 'RAM', which forms part of the basic 8085A microprocessor system.

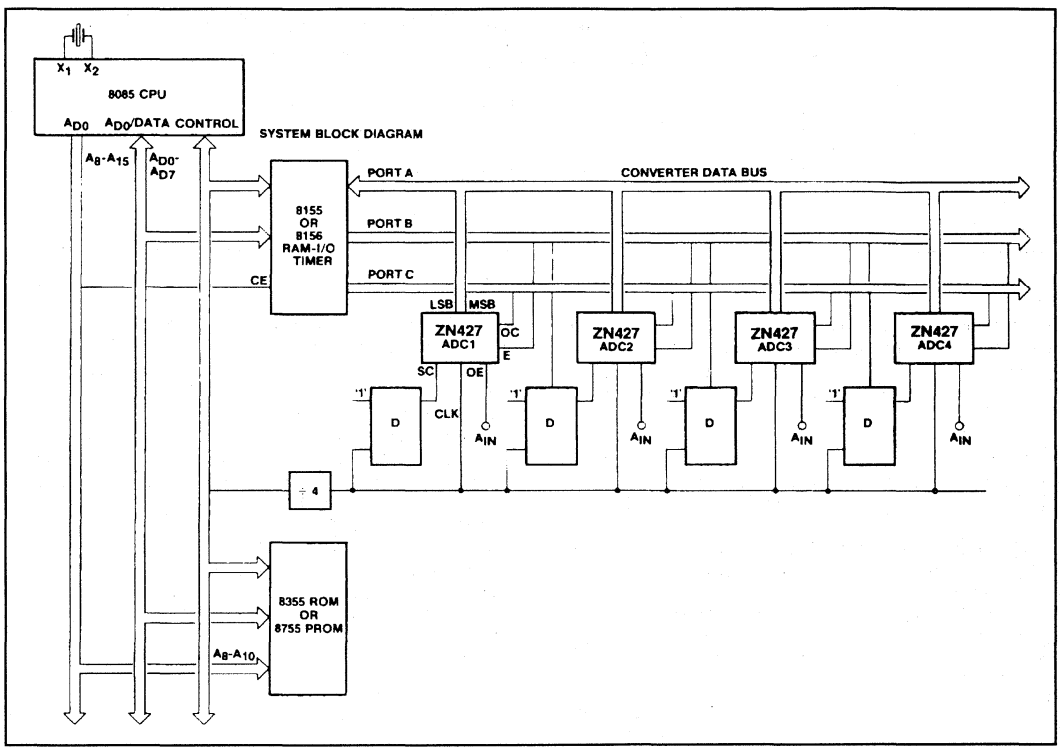


Fig.1 System block diagram

The ZN427 A-D converter

The ZN427 is a monolithic 8-bit, successive approximation A-D converter designed for microprocessor compability. It features fast 15µs conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D-A converter, a 2.5V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.

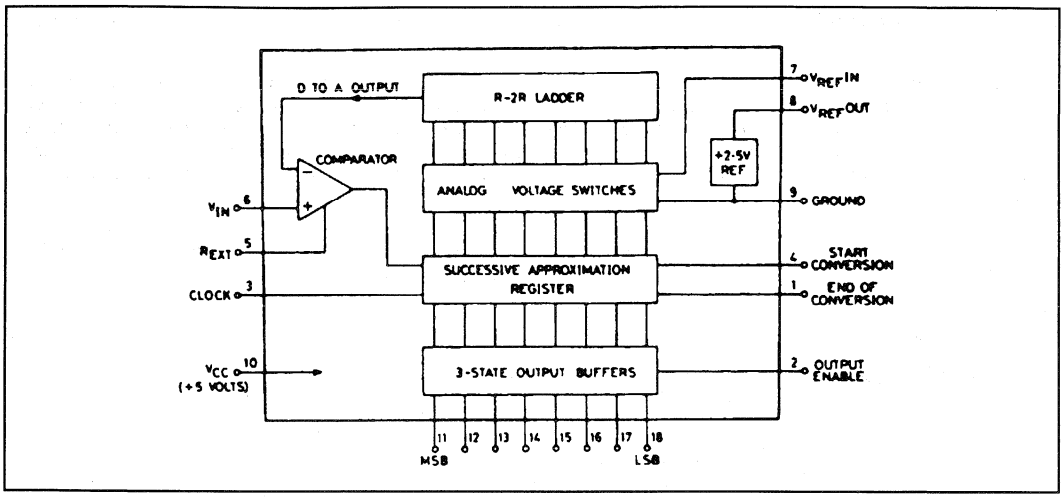


Fig.2 ZN427 logic diagram

Operation of the ZN427 is best described with reference to the timing diagram - Fig. 3. Conversion is initiated by a start convert (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

1. The leading edge of the SC-pulse should precede the first active (negative going) edge of the clock (after trailing edge of the SC pulse) by at least 1.5µs to allow for MSB setting.

2. The trailing edge of the SC pulse must not occur within ±200ns of a negative going edge of the clock.

3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse. Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D to A converter of $V_{REFIN/2}$. This value is compared with the input voltage V_{IN}, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REFIN/2} > V_{IN}$, or else to keep it at 1. Bit 2 is switched to a '1' on the same clock edge, and on the next edge a decision is made about bit 2, again by comparing the D/A output with V_{IN}. This process is repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is valid representation of V_{IN}. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is a '0' and are enabled when the OE input is taken to a '1'.

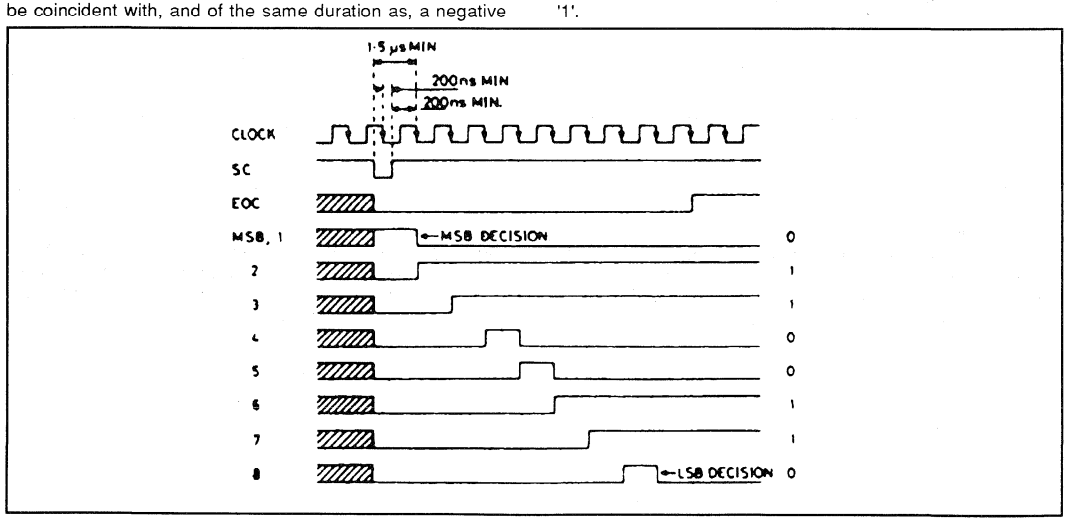


Fig.3 Timing diagram

The 8085A microprocessor system

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 users manual, so only a brief description is given here.

The 8085A is a complete 8-bit parallel central processing unit. A minimum component 8085 microcomputer system can be built from just three chips - the 8085A CPU, an 8355 or 8755 ROM or PROM, and an 8155 or 8156 RAM/TIMER/I-O chip. The 8155/8156 provides, in addition to 2k bits of Static RAM, two programmable 8-bit I/O Ports, one programmable 6-bit I/O Port and a programmable 14-bit binary timer counter. (The difference between the 8155 and the 8156 is that on the 8155 the CHIP ENABLE is active LOW, and on the 8156 it is active HIGH).

The ZN427 interface

This application note describes how up to 4, ZN427 ADCs can be connected to the I/O ports of one 8155 RAM to provide 4 analog input channels to the microprocessor system. Since most 8055 based systems include the SDK-85 system design kit will incorporate one or more 8155s, then the addition of analog input channels would involve minimum additional hardware and design effort. An advantage of using the 8155 I/O ports is that no additional address decoding or bus demultiplexing and buffering hardware is necessary.

For existing systems, if spare I/O ports are available then analog inputs can easily be added without any major modifications to the hardware. Also the expansion of the number of input channels to a system by addition of extra 8155s should be easily implemented since this device is directly bus compatible with the 8085A .

The 8155 I/O ports are allocated as shown in the logic diagram, Fig.1. Port A is programmed as INPUTS and provides an 8-bit data bus which connects to the three-state binary data outputs of each ZN427. Port B is programmed as OUTPUTS, the lower 4-bits provide the start convert and the upper 4-bits provide the output enable signals to each ZN427. The END OF CONVERT output of each ZN427 is connected to a port C pin, which are programmed as INPUTS to provide the individual BUSY FLAGS for each ZN427. Note that only 4- of the 6-bits available from port C are used.

The ZN427 clock can be supplied either from an external source or from the 8085A CLOCK OUTPUT. Since the 8085A clock will normally be at 3MHz, it will be necessary to divide this down by at least a factor of 4. This is achieved in the circuit, see Fig.6, by means of a dual JK flip-flop (7473) connected as a 2-bit binary counter. (Note: This will provide a clock frequency of 750kHz which is a little higher than the ZN427 clock frequency spec. minimum of 600kHz. However, for most practical applications the loss in accuracy due to this will be minimal.) An external clock could be used for the ZN427 but the advantage of using the microprocessor clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of the microprocessor CLOCK CYCLES (or 'T' states).

(Note: To avoid confusion, future reference to clock will mean the ZN427 clock signal unless specifically stated otherwise.)

The START CONVERT pulse is generated using a 'D' type flip-flop ($^1/_2$ 7474) in order to meet the timing requirements discussed earlier. A conversion cycle is started by outputting a '0' followed by a '1' from the appropriate port B output to the CLEAR input of the 'D' type which sets the SC input of the ZN427 to '0'. The first positive going clock edge after the CLEAR input is returned to a '1' clocks the 'D' type and sets the SC input to '1'. This sequence is illustrated in the start pulse timing diagram, Fig.4.

On the 9th negative clock edge after the start pulse the END OF CONVERT output goes to a '1' signifying the end of the conversion process, this can be detected by an I/O read on port C. However, when generating the ZN427 clock from the microprocessor clock as shown, the EOC output will always occur within 35 microprocessor clock cycles after the OUT instruction returning the SC to a '1'. In this case it is not necessary to poll the EOC outputs, the ZN427 data outputs can be read after a suitable fixed delay in the program. For application where process time is at a premium or if immediate response is required to an EOC output, a microprocessor interrupt can be generated by connecting the EOC output direct to one of the 8085A restart inputs. The EOC outputs of two 4-ZN427s can be 'wire-OR'd' to produce a common interrupt line. Usually, however, the fast conversion time of the ZN427 (15μs) will make it not worth-while to employ microprocessor interrupts since the conversion time takes less than 6/7 typical microprocessor instructions .

The binary output data is applied via the converter data bus to port A of the 8155 by driving the OE output to a '1' from the appropriate port B bit. Obviously the program should be arranged so that the outputs of only one ZN427 are enabled at any one time, in order to avoid bus contention problems. Note that in this application the output enable and disable switching times (which are specified at 250ns max.), need not be considered since they are much less than the instruction execution times.

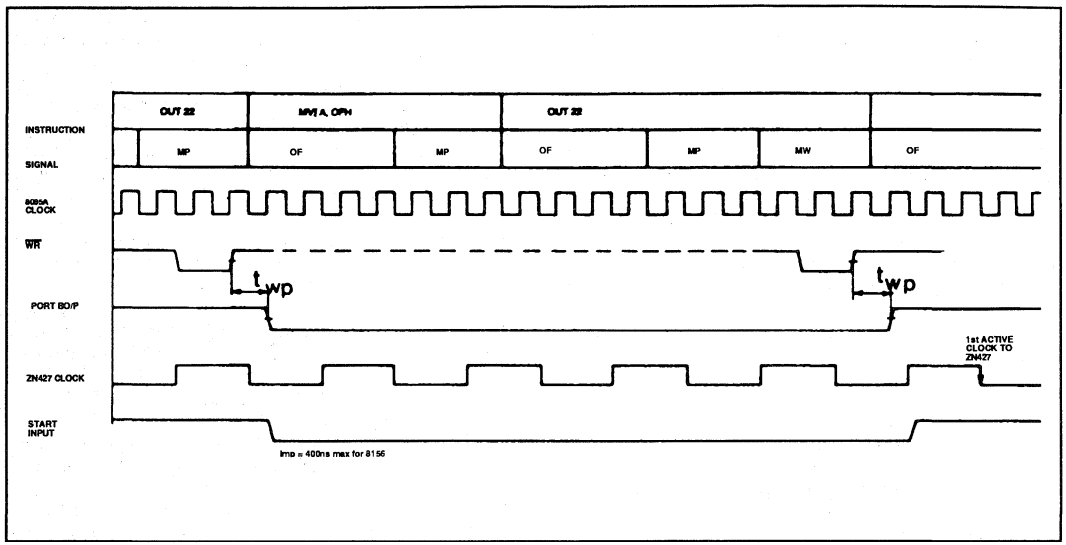


Fig.4 Start pulse timing diagram

The circuit diagram, Fig. 6 shows the ZN427s connected for a unipolar input range of 0 to +10V. Other ranges, e.g. +5V, ±10V, and ±5V can be readily obtained by using the appropriate resistors as shown in the ZN427 data sheet. Note also that the reference, $V_{REF\,IN}$, of up to five ZN427s may be driven from one internal reference. This useful feature saves power, discrete components, and gives excellent gain tracking between the converters.

In the circuit the negative supply to the ZN427s is through an 82k resistor from -5V. By suitable choice of resistor any negative supply of -3 to -30 volts may be used. For applications where only a positive 5 volt supply is available, a simple diode pump circuit suitable for up to 5-ZN427s is shown in the ZN427 data sheet.

Program example

A simple program is given together with the flow diagram in Fig. 5, which illustrates the ease of controlling and reading the ZN427 with the 8155 I/O ports.

Following the flow diagram it is seen that after initialisation of the stack pointer the I/O ports of the 8155 are defined - ports A and C as INPUTS, port B as OUTPUTS. A simultaneous START CONVERT pulse is sent to all the ADCs by outputting logic 'O' followed by logic '1' to the lower 4-bits of port B. The EOC outputs of the ADCs are then read via port C and tested for a logic '1' to check if the conversion process has finished. The microprocessor will loop on this part of the program until the EOC output of all the ADCs go to '1'. When this occurs the program proceeds by enabling the outputs of each ADC in turn and reading the binary data via port A. The ADC outputs are enabled in turn by outputting a logic '1' to each of the upper 4-bits of port B (keeping the other 3-bits at '0' and the lower 4-bits at a '1'). The data from each ADC is stored in consecutive memory locations, starting at the address labelled 'DATA'. The H and L register pair hold the memory address at which data is to be saved; these are incremented for each read of the ADC.

This program could easily be modified to act as a sub-routine for another main program. As mentioned previously a fixed delay could be substituted for the program loop which tests the EOC outputs. Also instead of generating a simultaneous START pulse separate START signals may be sent to each ADC at different times in a control cycle.

Summary

The system described in this report should be suitable for most applications since it allows complete control of each individual ADC. However, the configuration can easily be changed for particular requirements, - a few ideas are briefly described below.

1. If a simultaneous START pulse is adequate, then the START CONVERT inputs of the ZN427s can be commoned together and driven via one 'D' type from one port output.

2. The EOC outputs of up to 4-ZN427s can be commoned and either taken to one port input or used as a microprocessor interrupt signal.

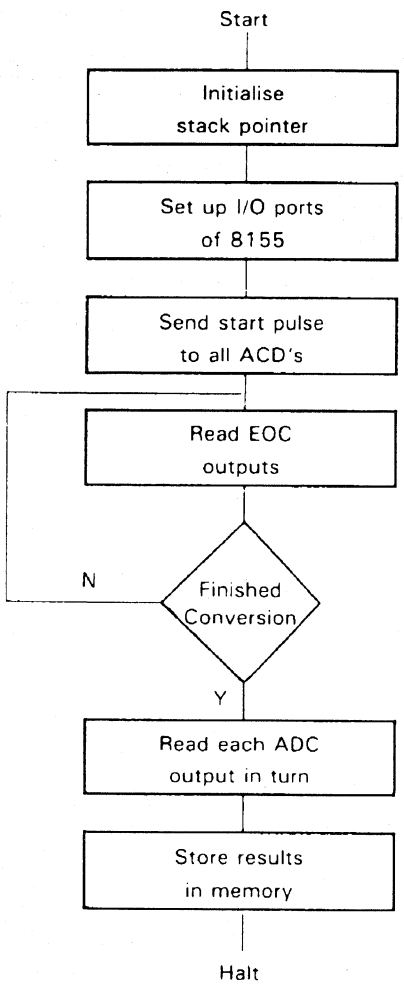
3. Adoption of methods 1 and/or 2 above would use 8155 Port bits and hence allow more ZN427s to be connected to each 8155.

4. Instead of generating the START pulse from the 8155 it could be asynchronously produced externally by a process timer, photo transistor or proximity detector circuit etc., the only timing requirement being that the pulse width fed to the CLEAR input of the 'D' type is at least half a clock period, (i.e. 640ns with a 320ns microprocessor clock) or 1.5µs, whichever is smaller.

5. If D-A channels as well as A-D are required in one system then ZN428,8-bit D-A converters can be mixed on the same converter data bus as the ZN427. This will allow a designer to tailor a system to his specific A-D and D-A requirements .

It is hoped that after reading this application note, the reader will have a much better insight into the operation and versatility of the ZN427, and into how it can easily be interfaced to a microprocessor system.

In order to avoid duplication only the relevant ZN427 characteristics were discussed in this report. For a full description and specification of the ZN427 please refer to the data sheet.



8155 PORT ALLOCATIONS

PORT A

PA0	BINARY DATA LSB
PA1	BINARY DATA LSB + 1
PA6	BINARY DATA MSB – 1
PA7	BINARY DATA MSB

PORT B

PB0	ADC1 SC INPUT
PB1	ADC2 SC INPUT
PB2	ADC3 SC INPUT
PB3	ADC4 SC INPUT
PB4	ADC1 OE INPUT
PB5	ADC2 OE INPUT
PB6	ADC3 OE INPUT
PB7	ADC4 OE INPUT

PORT C

PC0	ADC1 EOC OUTPUT
PC1	ADC2 EOC OUTPUT
PC2	ADC3 EOC OUTPUT
PC3	ADC4 EOC OUTPUT

I/P PORT ADDRESSES

20	COMMAND/STATUS REG
21	RAM PORT A
22	RAM PORT B
23	RAM PORT C

Fig.5 Program flow diagram

ZN427 - 8085A PROGRAM EXAMPLE

Location	Object		Source statement	Comment
2000	31C8204		LXI SP. 20C8	Intialise Stack pointer
2003	3E02		MVI A, 02H	Define I/O ports
2005	D320		OUT 20	
2007	3E00		MVI A, 00H	
2009	D322		OUT 22	Send start to ALL ADC's
200B	3EOF		MVI A, 0FH	
200D	D322		OUT 22	
200F	060F		MVI B, 0FH	
2011	DB23	LOOP:	IN 23	Read EOC s
2013	AO		ANA B	Strip upper 4 bits
2014	B8		CMP B	Test if ALL EOC s
2015	C21720		JNZ LOOP	are A '1'
2018	213B20		LXI H, DATA	
201B	3EIF		MVI A, 1FH	
201D	D322		OUT 22	Enable ADC 1
201F	DB21		IN 21	Read ADC 1
2021	77		MOV M, A	Save in Loc., DATA
2022	23		INX H	Increment pointer
2023	3E2F		MVI A 2FH	
2025	D322		OUT 22	
2027	DB21		IN21	Read ADC 2
2029	77		MOV M, A	Save in Loc. DATA + 1
202A	23		INX H	
202B	3E4F		MVI A 4FH	
202D	D322		OUT 22	
202F	DB21		IN 21	Read ADC 3
2031	77		MOV M, A	Save in Loc. DATA + 2
2032	23		INX H	
2033	3E8F		MVI A 8 FH	
2035	D322		OUT 22	
2037	DB21		IN 21	Read ADC 4
2039	77		MOV M, A	Save in Loc. DATA + 4
203A	76		HLT	
203B		DATA:		
203C				
203D				
203E				

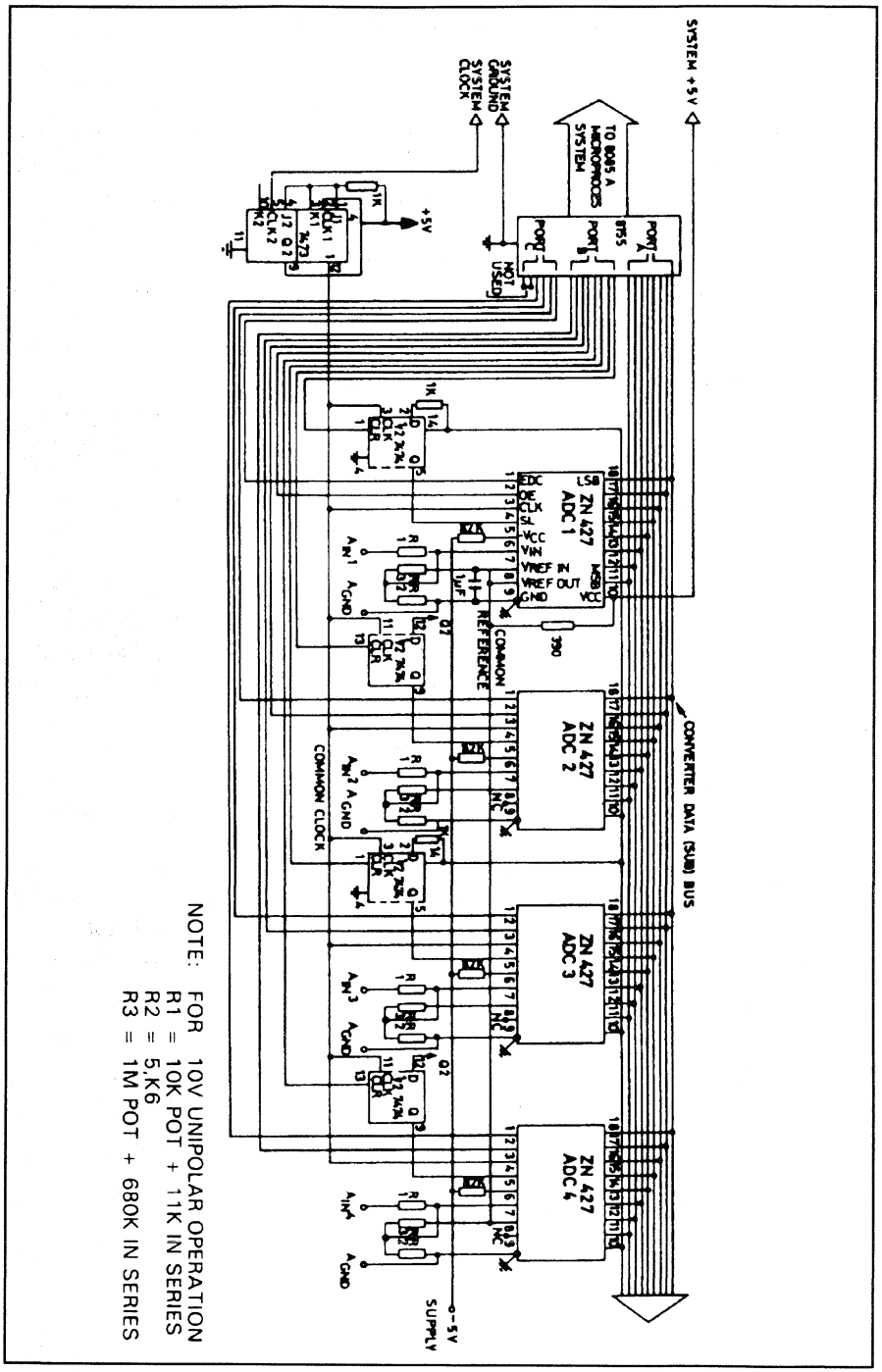

SYSTEM +5V
TO 8085 A MICROPROCES SYSTEM
SYSTEM GROUND
SYSTEM CLOCK
PORT A
PORT B
PORT C
8255
NOT USED
+5V
1K
ZN 427 ADC 1
ZN 427 ADC 2
ZN 427 ADC 3
ZN 427 ADC 4
REFERENCE
COMMON
COMMON CLOCK
CONVERTER DATA (SUBD) BUS
SUPPLY
0-5V
NOTE: FOR 10V UNIPOLAR OPERATION
R1 = 10K POT + 11K IN SERIES
R2 = 5.K6
R3 = 1M POT + 680K IN SERIES

Fig.6

Interfacing the ZN428 D-A Converter with the 8085A

This report describes a simple, low cost, expandable multichannel D-A system based on the ZN428, 8-bit D-A converter interfaced directly to the I/O ports of the 8155, 2K bit static RAM, which forms part of the basic 8085 microprocessor system.

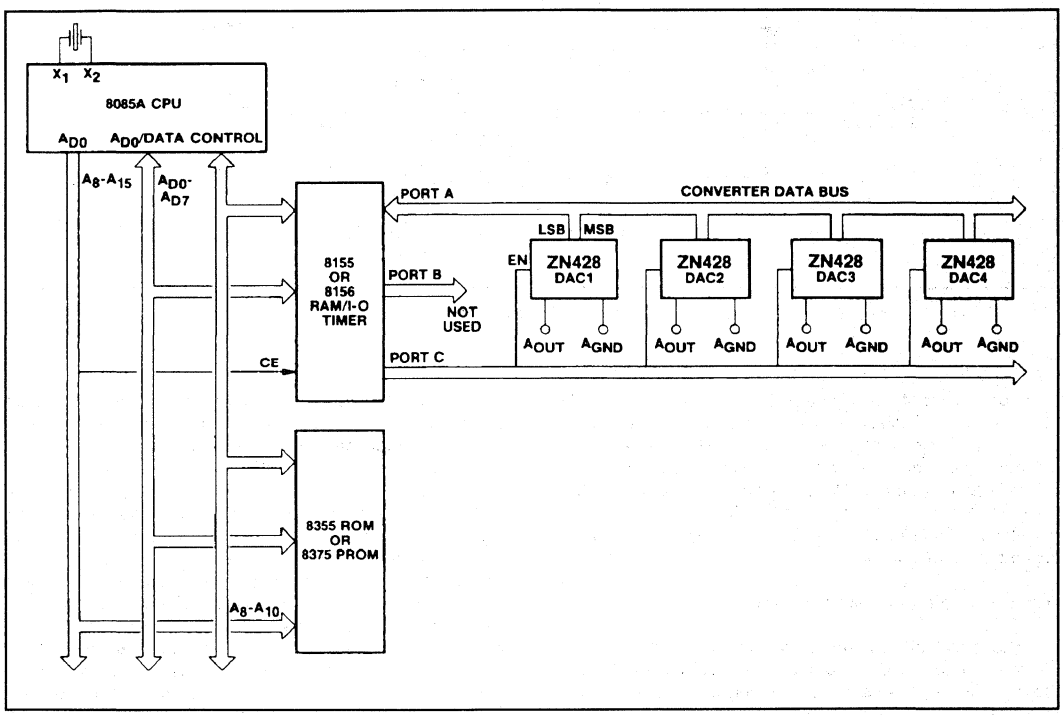


Fig.1 System block diagram

The ZN428 D-A converter

The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when $\overline{\text{ENABLE}}$ is at logic '0' and the data is held when $\overline{\text{ENABLE}}$ is taken to logic '1'. The ZN428 features single +5 volt supply requirements, fast 800ns setting time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

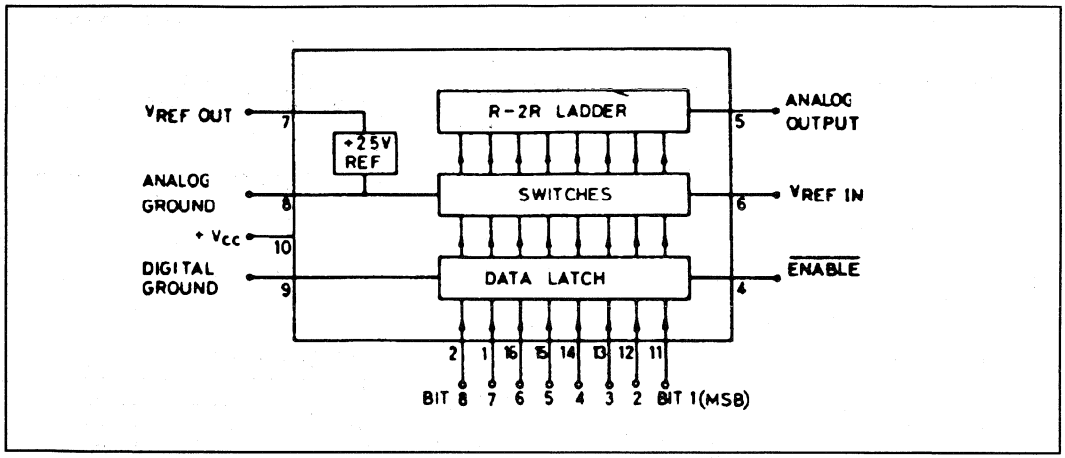


Fig.2 ZN428 logic diagram

The converter is of the voltage switching type and used R-2R ladder network. Each 2R element is connected to the 0 volt or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0 volt to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The 8085A microprocessor system

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 users manual, so only a brief description is given here.

The 8085A is a complete 8-bit parallel central processing unit. A minimum component 8085A microcomputer system can be built from just three ICs - the 8085A CPU, an 8355 or 8755 ROM or PROM, and an 8155 or 8156 RAM/TIMER/I-O IC. The 8155/8156 in addition to 2K Bits of Static RAM, provides two programmable 8-bit I/O ports, one programmable 6-bit I/O port and a programmable 14-bit binary timer counter. (The difference between the 8155 and the 8156 is that on the 8155 the CHIP ENABLE is active LOW, and on the 8156 it is active HIGH.)

The ZN428 interface

This application note describes how one or more ZN428 DACs can be connected directly to the I/O ports of an 8155 RAM to provide analog output channels from the microprocessor system.

Since most 8085 based systems, including the SDK-85 system design kit, will incorporate one or more 8155s then the addition of analog output channels can be made with the minimum of extra hardware and design effort. An advantage of using the 8155 I/O ports is that no additional address decoding or bus multiplexing and buffering hardware is necessary. For existing systems, if spare I/O ports are available then analog outputs can easily be added without major modifications to the hardware. Also expanding the number of output channels by means of addition of extra 8155s should be easy to implement, since the 8155 is directly bus compatible with the 8085A. Fig. 3 shows 4-ZN428s connected to the I/O ports of one 8155. Port A is programmed as OUTPUTS and provides a common 8-bit data bus which is connected to the binary data inputs of each ZN428. The $\overline{\text{ENABLE}}$ inputs of each of the ZN428s are connected to separate pins on port C which is also programmed as OUTPUTS. Note that in this configuration only 4 of the 6 port C pins are used and port B is also unused.

The reference voltage of all converters, is provided by connecting the $V_{REF\ OUT}$ pin of one ZN428 to the $V_{REF\ IN}$ pins of all the ZN428s as shown. This useful feature saves power, components and gives excellent gain tracking between converters. Up to five ZN428s may be driven from one internal reference in this way.

The circuit, Fig. 3, shows the outputs of the ZN428s taken directly from pins 5 and 8. This will provide an output range of 0V to $V_{REF\,IN}$ through a 4kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any 'glitches' which may be present. The value of this capacitor depends on the noise in the system and the response time required, however, for the minimum settling time it should not be greater than 100pF. The output buffer amplifier was omitted from the ZN428 in order to allow greater system speed, flexibility and lowest cost. Both unipolar and bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate analog and digital ground pins. These can be connected together close to the IC pins. However, for noisy systems or environments it may be better to keep the analog ground pins for each individual ZN428 separate from the digital ground, and to connect each analog ground to a single common earth point in the system, away from sources of digital noise such as clock oscillators, digital buses etc. The analog ground output line or terminals should also be taken direct to this common earth point. (Note: The maximum voltage between analog and digital grounds is limited to 200mV.)

Data is fed to a converter simply by outputting the binary data onto the common bus from port A of the 8155. The appropriate output from port C is then driven to a logic '0' level then back to a logic '1'. This will transfer the binary data on the bus into the input latches of the ZN428. The $\overline{\text{ENABLE}}$ inputs of converters which are not being updated are held at logic '1'. The data from port A can now be changed and the next converter updated as and when required as determined by the controlling program of the microprocessor. Note that in this application the data set-up and data hold times and enable pulse widths need not be considered since they are much less than the microprocessor instruction execution times.

Program example

A simple program is given together with the flow diagram in Fig.4, which illustrates the ease of controlling the ZN428 in conjunction with the 8155 I/O ports.

The object of the program is to read the binary data from four successive memory locations and to output this data sequentially to each of the four DACs. In practice this program would probably act as a sub-routine outputting data derived from some external source and operated on by the main program.

With reference to the flow diagram Fig. 4 it is seen that after initialisation of the stack pointer the I/O ports A and C are defined as OUTPUTS. The H and L register pair are loaded with the starting address in memory of where the data to be outputted is stored. Register B determines which ADC is to be enabled, this is set initially to 1 1 1 1 1 1 10; while register C, which acts as a loop counter is set to 4. Data is then read from memory into the accumulator using the H and L registers in the register indirect addressing mode. This data is outputted onto the converter data bus via port A by sending the contents of the accumulator directly to the 8155 with the 'OUT' instruction. DAC 1 is now enabled by transferring the contents of register B to the accumulator and outputting this via port C. The accumulator contents are rotated one bit left before being transferred back to register B, ready to enable the next DAC. Next $\overline{\text{ENABLE}}$ is removed by outputting all 1 's via port C, H and L are incremented to address the next data byte and register C is decremented and tested for zero. In this case register C will contain 03 and the program will branch back to the address labelled 'LOOP' via a conditional jump instruction, and the data byte will be read into the accumulator. Since register B was shifted one bit left the new data will be loaded into DAC 2 on this cycle of the loop. The program cycles round the loop 4 times, reading the data from memory and outputting it to each DAC in turn until register C is decremented to zero, at which point the program halts.

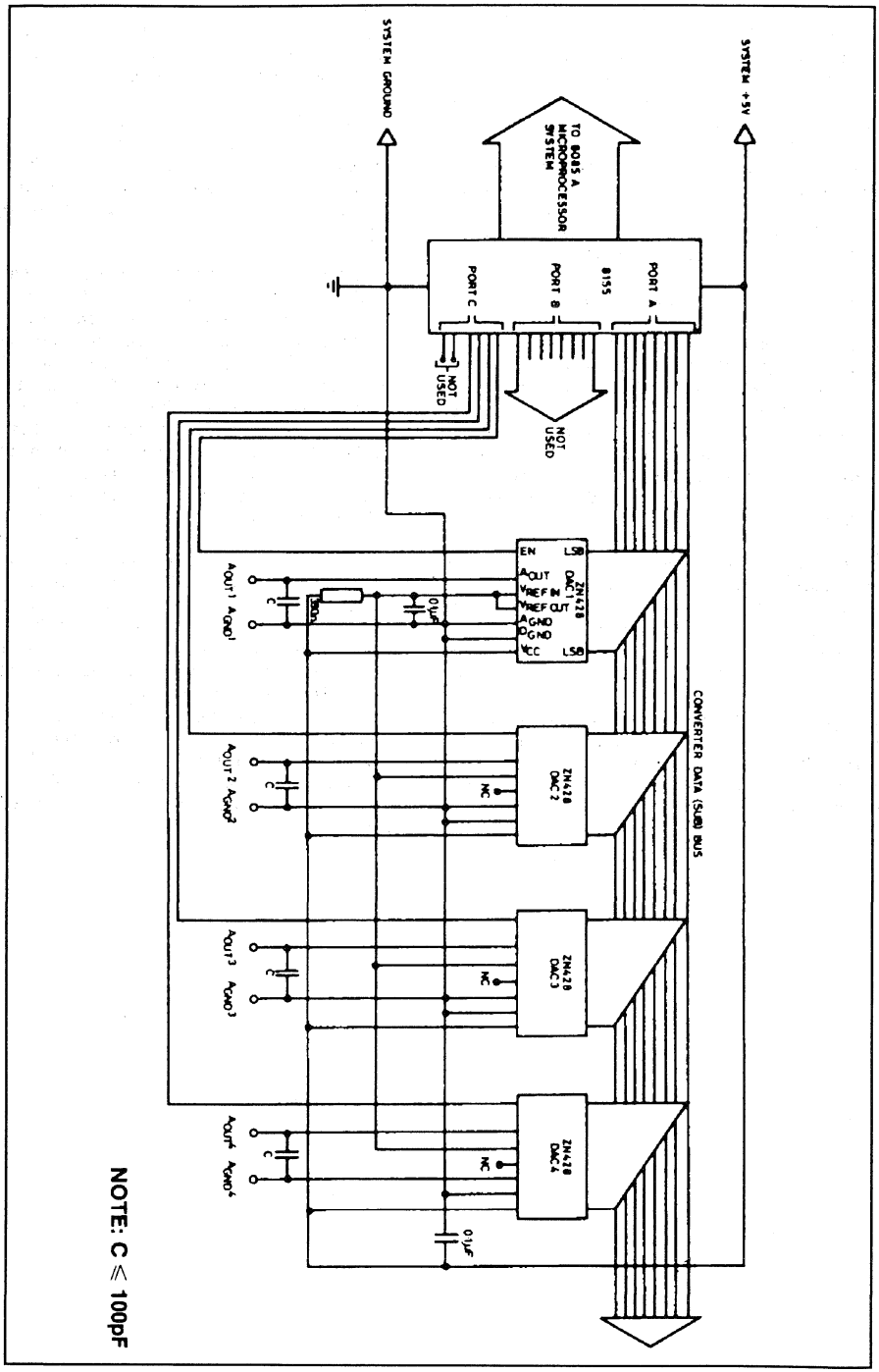

SYSTEM GROUND
SYSTEM +5V
TO 8085 A MICROPROCESSOR SYSTEM
PORT C
8155
PORT B
PORT A
NOT USED
NOT USED
EN
LSB
AOUT
VREF IN
VREF OUT
AGND
DGND
VCC
LSB
ZN428 DAC 1
AOUT1 AGND1
C
150Ω
0.1μF
ZN428 DAC 2
AOUT2 AGND2
ZN428 DAC 3
AOUT3 AGND3
ZN428 DAC 4
AOUT4 AGND4
NC
0.1μF
CONVERTER DATA (SLSB) BUS
NOTE: C ≤ 100pF

Fig.3

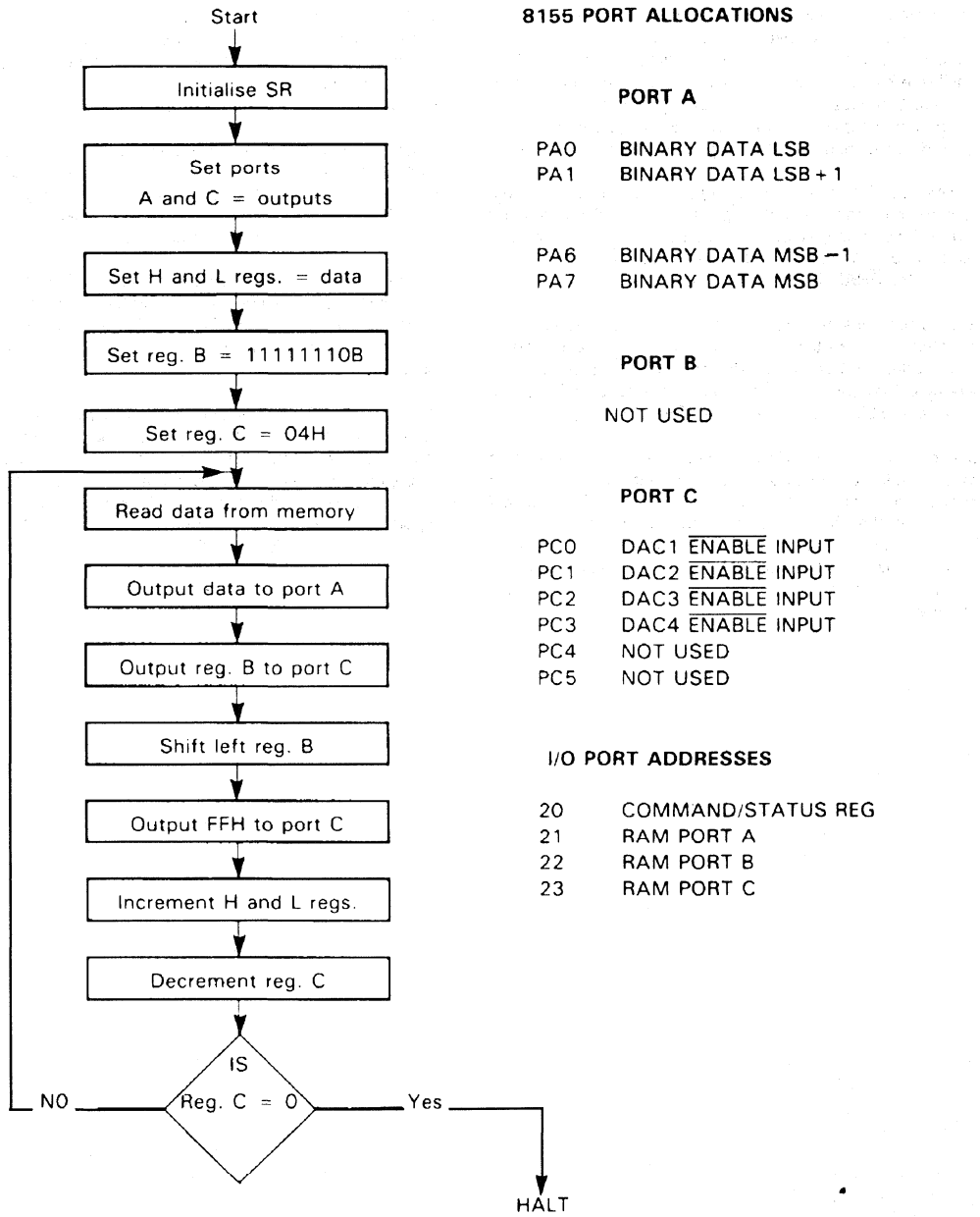


Fig.4 Program flow diagram

Summary
The system described in this report should be satisfactory for most applications, however, this configuration is by no means rigid, but is only intended as one example to demonstrate how easily the ZN428 can be used with the 8085A microprocessor system. A few ideas and notes are briefly described below, and it is hoped that these will help the design engineer to produce the most efficient system for his particular requirements.

1. The 8155 I/0 ports can be allocated as dictated by system requirements and availability. In the example all of port A and four of the six port C I/0 pins are used. Port B could have been used equally as well either for the converter data bus or to provide the $\overline{\text{ENABLE}}$ signals.

2. If I/0 port pins are limited and only one DAC needs to be enabled at any one time, then a decoder IC (i.e. 8205, 1 out of 8 binarv decoder) can be used to drive the $\overline{\text{ENABLE}}$ inputs. For example 4 I/0 port pins, 3 for the address code and 1 for the decoder enable would drive 8 DAC ENABLE inputs.

3. In order to update 2 DACs simultaneously but with different data, then the binary inputs of one (or more) DACs could be connected to port A and the other DAC to port B. The relevant data could then be output on Ports A and B and then the ENABLE inputs of both DACs driven to logic '0' together, either by commoning the two inputs to one port C or by using separate I/0 pins from port C but programming both bits to go low together.

4. The number of ZN428s which can be connected to a common data bus is limited only by the bus capacitance and the drive capability of the 8155 I/0 Ports. Note the low inputs currents of the ZN428-
IIH = 20μ1A at 2.4V, IIL = -5μ1A at 400mV.

5. When the ZN428 $\overline{\text{ENABLE}}$ input is held at logic '0' the input latches are held open and the data is transferred directly to the ladder switches. Therefore, if repeatedly updating only one DAC the $\overline{\text{ENABLE}}$ input can be held at logic '0' instead of returning to logic '1' after each update.

6. If A-D channels as well as D-A are required in one system, then ZN427, 8-bit A-D converters can be mixed on the same converter data bus as the ZN428. This will allow the design engineer to tailor a system to his specific A-D and D-A requirements.

It is hoped that after reading this application note the reader will have a much better insight into the operation and versatility of the ZN428, and into how it can easily be interfaced to a microprocessor system. In order to avoid duplication only the relevant characteristics of the ZN428 were discussed in this report. For a full description and specification of the ZN428 please refer to the data sheet.

ZN428 - 8085A PROGRAM EXAMPLE

Location	Object		Source statement	Comment
2000	31C8204		LXI SP. 20C8	Intialise SP
2003	3E0D		MVIA, 0D	Define I/O ports
2005	D320		OUT 20	
2007	212020		LXI H, DATA	Set H & L = data
200 A	06FE		MVI B, FEH	
200 C	0E0 4		MVI C, 04H	
200 E	7E	LOOP:	MOV A,M	Read data
200 F	D321		OUT 21	Put data on bus
2011	78		MOV A,B	
2012	D323		OUT 23	Set $\overline{\text{Enable}}$ low
2014	07		RLC	Rotate left for next DAC
2015	47		MOV B,A	
2016	3EFF		MVI A, FF	Set $\overline{\text{Enable}}$ high
2018	D323		OUT 23	
201A	23		INX H	
201B	0D		DCR C	
201C	C2 0E 20		JNZ Loop	Jump IF C = 0
201F	76		HLT	
2020			DATA	
2021				
2022				
2023				

Interfacing the ZN448/9 A-D Converters to the Z80μP via a Z80 PIO

AN191 - 2.2

This report illustrates how to interface one or more ZN448/9 A-D converters to a Z80 based microprocessor system using a Z80 PIO. Circuit diagrams and program examples are given to enable the user to get his interface system working. The following is also applicable to the faster versions ot the Z80μP and the Z80 PIO and also to the CMOS versions. Most of the principles described can also be applied when interfacing the ZN448/9 to other popular μPs.

In order to keep this report concise it is assumed that the reader is familiar with the Z80 system.

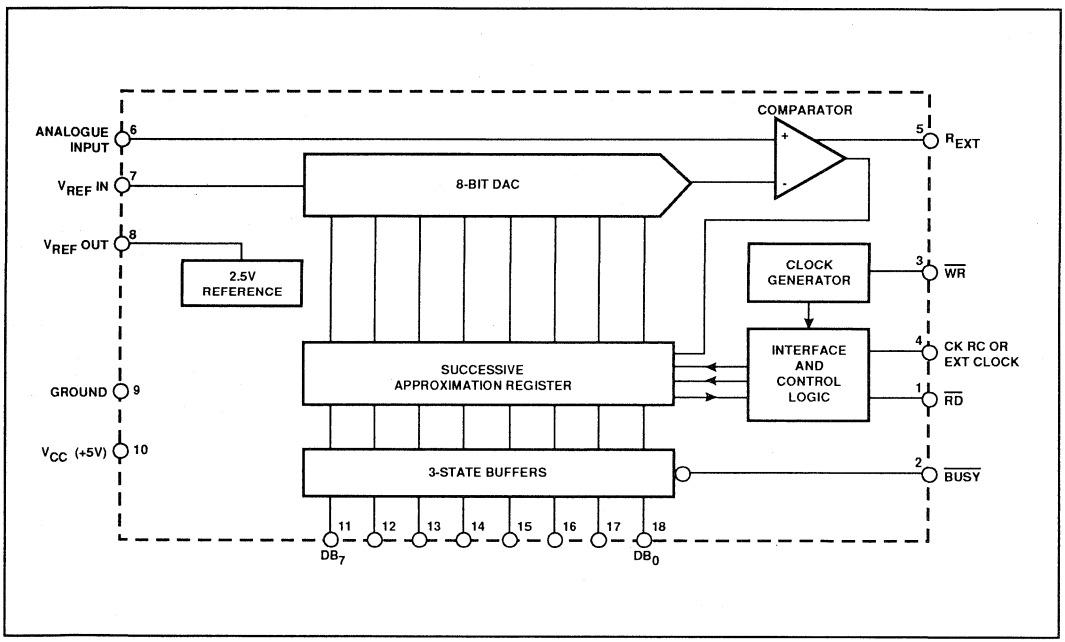


Fig.1 ZN448/9 system diagram

THE ZN428/9 A-D CONVERTERS

The ZN448/9 are 8-bit successive approximation A-D converters with linearity errors of $\pm^1/_2$ and 1 LSB respectively.

Hereafter any description relating to one of these devices is equally applicable to the other type.

All active circuitry is contained on-chip including three-state output buffers, 2.5V bandgap reference and a clock generator.

They are each capable of converting unipolar or bipolar input voltages with the only external components required for operation being a reference resistor and capacitor, clock capacitor, resistor to the negative supply and the analog input scaling resistor(s) (to accommodate the different input voltages).

A conversion is initiated by taking the $\overline{WR}$ input low and then high. The conversion then takes between $7^1/_2$ and $8^1/_2$ clock cycles after the $\overline{WR}$ positive edge. The $\overline{WR}$ input signal may be completely asynchronous to the chip clock. The falling edge of the $\overline{WR}$ signal sets the MSB high and the remaining bits low. This edge also sets the $\overline{BUSY}$ output low. Once started the converter cycles through a successive approximation routine to arrive at a result (see data sheet for explanation). When the conversion is finished, the $\overline{BUSY}$ output goes high indicating that valid data may now be read. A low at the $\overline{RD}$ input enables the data outputs and a high puts them into the high impedance state.

The devices will operate correctly with clock frequencies up to at least 900kHz. At 900kHz the conversion time is less than 9.5µs. (In fact the devices will typically operate above 900kHz but some loss in accuracy may result.)

The negative supply requirement is minimal (e.g. 75µA) and can easily be supplied from a simple diode pump circuit.

Further information including the input resistors required for various unipolar and bipolar input voltages and examples of diode pump circuits, can be obtained from the data sheet.

Z80 PIO

The Z80 PIO is a programmable two port device which provides a TTL compatible interface between peripheral devices and the Z80 CPU. It is capable of interfacing directly to the CPU without any external logic. The two 8-bit, bidirectional ports, each have two handshake lines (RDY and $\overline{STB}$) for use when transferring data to or from peripherals. Either port or indeed any port bit, can be programmed to act as an input or output.

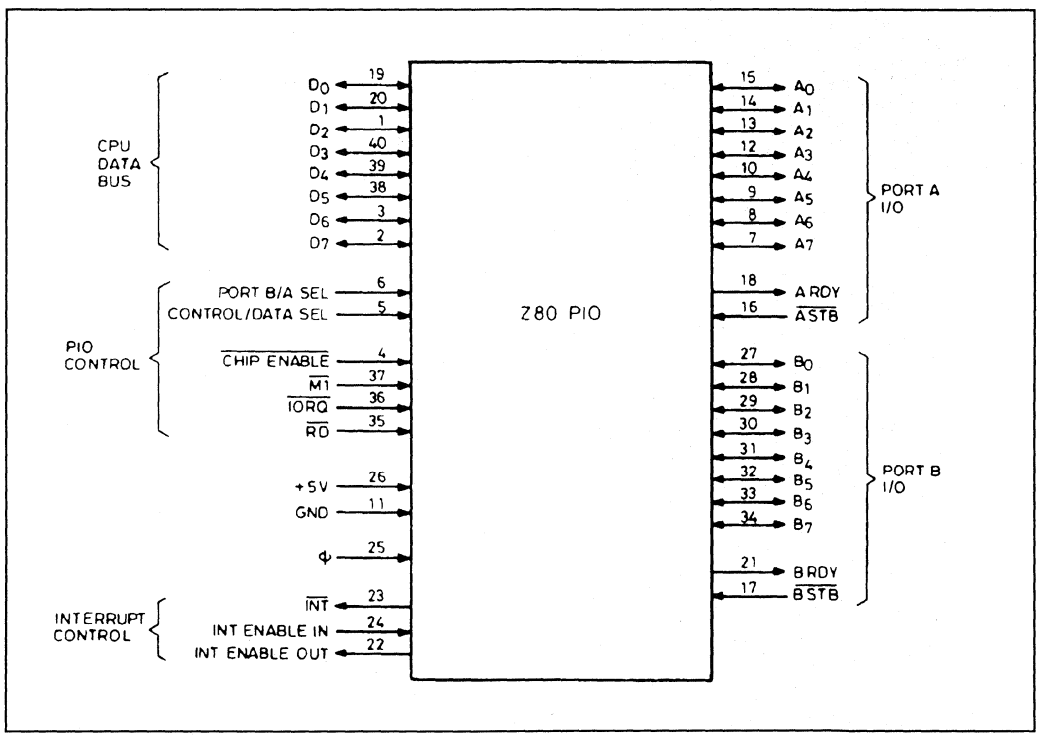


Fig.2 Z80 PIO

The PIO has 4 operating modes:
Mode 0 (Output mode) - All port bits are set to outputs .
Mode 1 (Input mode) - All port bits are set to inputs .
Mode 2 (Bidirectional mode) - Used for bidirectional data transfer - not considered in this report.
Mode 3 (Control mode) - Each bit can be programmed individually to act as an input or output. Useful for status and control applications .

We will utilise mode 1 for reading the result of the A-D conversion. With mode 3 we can configure some of the port bits as outputs, taking them low and high as desired (can be used for controlling the $\overline{RD}$ and $\overline{WR}$ input on the converters) and we can configure some of the port bits as inputs (for monitoring the $\overline{BUSY}$ outputs). If the $\overline{BUSY}$ outputs are not being monitored and the port bits are being used as outputs, mode 0 could instead be used for controlling the $\overline{RD}$ and $\overline{WR}$ inputs.

In the input mode, the $\overline{STB}$ input needs to be low to allow data into the port. A positive edge on the $\overline{STB}$ latches data into the port, causes RDY to go low and generates an interrupt if enabled. During a port read the RDY line will be forced low, if not already low, and then high.

This is a brief introduction to a complex device.

Further information can be obtained from the manufacturers data sheets.

INTERFACING A SINGLE ZN448/9 TO THE Z80 USING A SINGLE PORT

If it is required to interface only one ZN448 to the Z80 system, this can be achieved using only a single port ($^1/_2$ PIO). Here the $\overline{RD}$ input on the ZN448 is tied low and hence the data outputs are permanently enabled.

A conversion can be started with a $\overline{WR}$ pulse derived from the RDY signal or from some other logic. Valid data can then be read when the conversion is finished. In order to ensure this, either a program delay can be used ((i) below) or the $\overline{BUSY}$ output can be used to generate an interrupt via the port $\overline{STB}$ input ((ii) below).

(i) Data acquisition using a program delay

Here a dummy read is issued to the port to generate a positive transition on the RDY output. This edge then triggers a monostable which in turn supplies a $\overline{WR}$ pulse to the ZN448. This initiates a conversion. The program then cycles through a delay routine to give the conversion time to finish. After this a genuine read is issued to the port and the data then processed as required .

The circuit diagram is as follows:

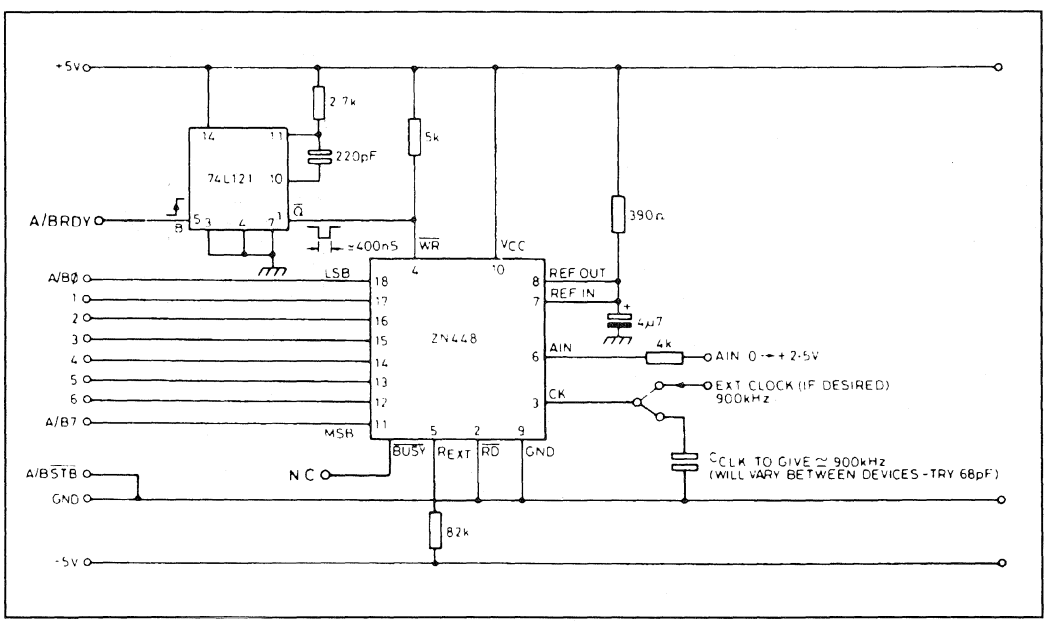


Fig.3 Interfacing a single ZN448 to a single port - program controlled

PROGRAM LISTING

PROGRAM 1

Address	Object code	Label	Source code	Comments
NN00	3E 4F		LD A, 4FH	} Sets port to input (Mode 1)
NN02	D3 PORTCO		OUT PORTCO, A	
NN04	DB PORT DA		IN A, PORTDA	Dummy read from port
NN06	3E DELAY		LD A, DELAY	Initialises A for delay
NN08	3D	(1)	DEC A	} Delay routine
NN09	20 FD		JR NZ, (1)	
NN0B	DB PORTDA		IN A, PORTDA	Reads result of conversion
NN0D	32 MEM		LD (MEM), A	Stores result
NN10	?		?	Return to monitor program (Command(s) system dependant)

KEY:
NN00 = Any Suitable starting address.
PORTCO = Port control address.
PORTDA = Port data address.
DELAY = Initialisation byte for delay (see comments).
MEM = 16-bit memory location nominated for storing data. (Needs assembling in the order Lo-byte, Hi-byte in the object code).

COMMENTS

The delay required depends on processor speed and the ZN448 clock frequency. With the ZN448 clock frequency at 900kHz, try working down from DELAY = 06H. For slower clocks the delay may need increasing accordingly.

When the processor reads the result of the conversion from the port, a further conversion is automatically initiated. This is of no consequence during normal operation. However if the data is being inspected manually for evaluation purposes, the data can appear incorrect at the first glance. This is because the valid data on the ZN448 outputs is one conversion behind the data read into the processor. Hence if the analogue input voltage is on the edge of a code transition, any noise present could possibly cause the result in memory and the data on the ZN448 outputs to differ slightly. If desired this can be overcome by examining the ZN448 outputs just before the conversion result is read (e.g. insert a break in the program), and then acquire the data for subsequent comparison.

The above arrangement is useful when there is only one spare port and it can be dedicated to this purpose.

(ii) Data acquisition under interrupt control

Interrupts are useful when interfacing to slow peripherals. However the ZN448 is not itself a slow peripheral as it can be operated to give a conversion time of less than 10μs. Hence it does not need to be interrupt driven.

However it may be required to call on the ZN448 relatively infrequently - as governed by some timing logic (e.g. a counter timer chip):

(a) this timing logic could vector to a subroutine which then starts a conversion and reads the result. In this case the subroutine might as well incorporate a delay - this has been covered in the previous section.

(b) alternatively this timing logic could initiate a conversion directly or, for example, via a monostable. This effectively makes the ZN448 appear slower and now makes interrupts more useful.

The second situation (b) above is now considered in this section. It is left to the user to configure this "timing logic" to best suit his particular requirements.

Remember that $\overline{\text{BUSY}}$ goes high to signal the end of conversion and also that the port $\overline{\text{STB}}$ input responds to positive transitions. Thus when $\overline{\text{BUSY}}$ is connected to $\overline{\text{STB}}$ and interrupts are enabled, an interrupt will be generated when $\overline{\text{BUSY}}$/$\overline{\text{STB}}$ goes high. This would then summon a service routine to read the result of the conversion.

PROGRAM EXAMPLE

This is a program to start a conversion. cycle through a delay routine (until conversion has finished) and then read the result. This data is then stored in memory.

PROGRAM STATEMENT

: Nominate memory location for storing the conversion results:
: Decide on delay required (see comments for suggestions).
: It is assumed that the port needs initialising.

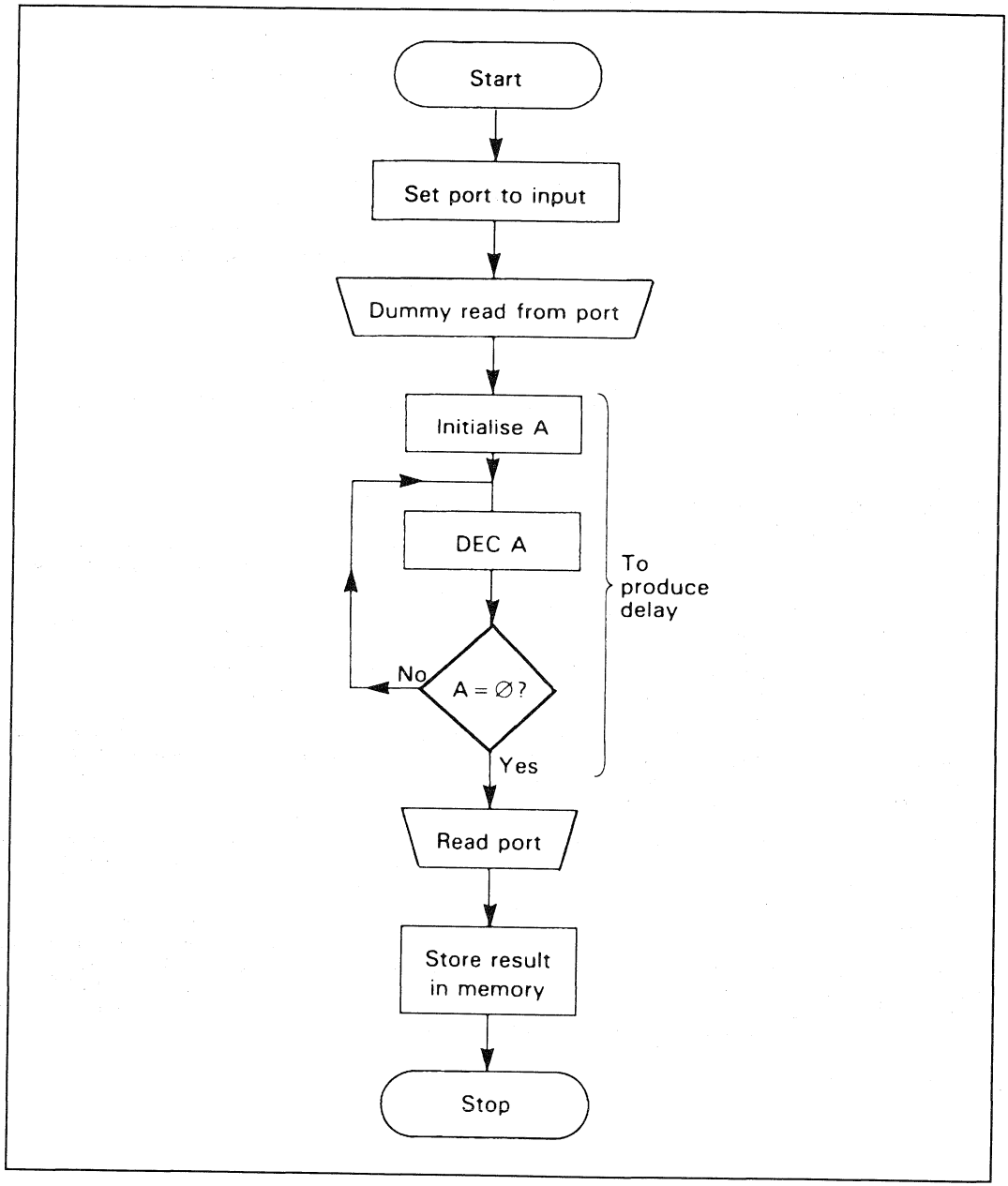


Fig.4 Flow chart 1

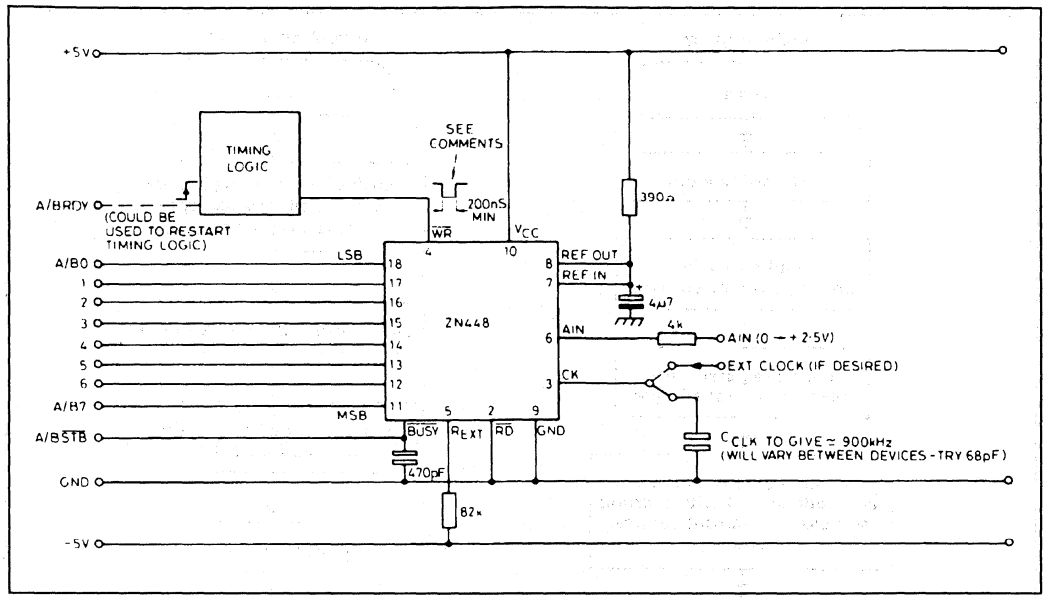


Fig.5 Interfacing a single ZN448 to a single port - interrupt driven

The capacitor on the $\overline{\text{BUSY}}$ O/P is to meet the port data to $\overline{\text{STB}}$ rising edge set up time.

PROGRAM EXAMPLE

Here, when an interrupt is generated via $\overline{\text{BUSY}}$, the µP is vectored to the service routine which then reads and stores the result of the conversion, the conversion having been previously initiated by the timing logic.

The µP is set to interrupt mode 2, as the ports are designed to be used in this mode. The contents of the I register and the port interrupt vector are combined by the µP to form a 16-bit vector. This is then used to look up the starting address of the interrupt service routine. The µP then loads the program counter with this address and continues program execution from this location.

PROGRAM STATEMENTS

: Nominate memory locations for the vectored address, the interrupt service routine and for storing the conversion result.

: It is assumed that the user initiates conversion correctly when required.

: It is assumed that the port needs initialising:

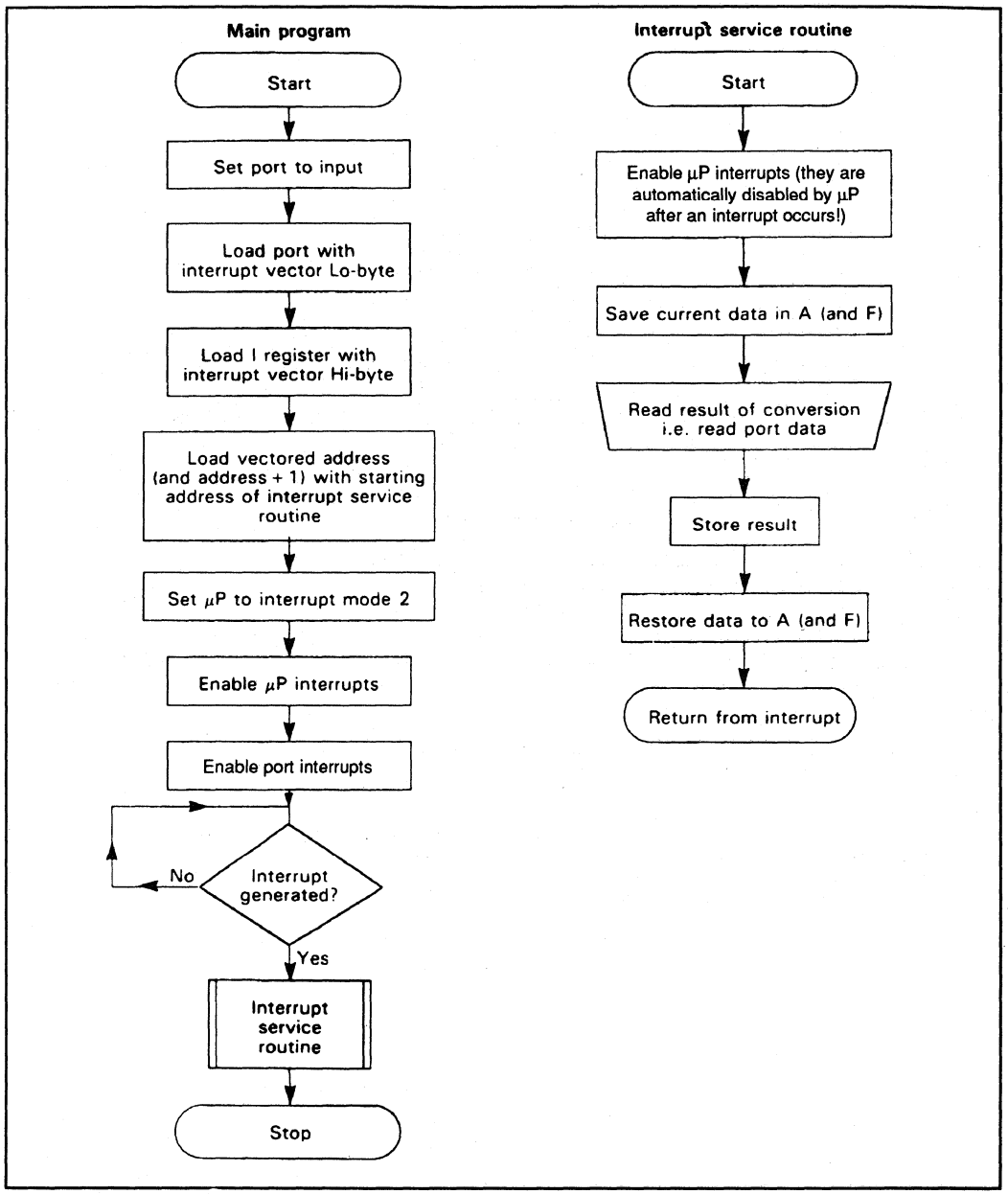


Fig.6 Flow chart 2

PROGRAM LISTING

PROGRAM 2

Address	Object code	Label	Source code	Comments
NN00	3E 4F		LD A, 4FH	Sets port to input (Mode 1)
NN02	D3 PORTCO		OUT PORTCO, A	
NN04	3E IVECL		LD A, IVECL	Loads port with interrupt vector Lo-byte
NN06	D3 PORTCO		OUT PORTCO, A	
NN08	3E IVECH		LD A, IVECH	Loads I register with interrupt vector Hi-byte
NN0A	ED 47		LD I, A	
NN0C	3E SERVL		LD A, SERVL	Loads vectored address (and consecutive address) with starting address of interrupt service routine
NN0E	32 IVEC		LD (IVEC), A	
NN11	3E SERVH		LD A, SERVH	
NN13	32 IVEC + 1		LD (IVEC + 1), A	
NN16	ED 5E		IM 2	set µP to interrupt mode 2
NN18	FB		EI	Enable µp interrupts
NN19	3E 83		LD A, 83H	Enable port interrupts
NN1B	D3 PORTCO		OUT PORTCO, A	
NN1D	76		HALT	Waits for interrupt (or reset!)
NN1E	?		?	Returns to monitor (command(s) system dependant)

INTERRUPT SERVICE ROUTINE

Address	Object code	Label	Source code	Comments
MM00	FB		EI	Re-enables µP interrupts
MM01	F5		PUSH AF	Stores current values of AF
MM02	DB PORTDA		IN A, PORTDA	Reads result of conversion
MM04	32 MEM		LD(MEM), A	Stores result in memory
MM07	F1		POP AF	Restores AF values
MM08	ED 4D		RETI	Returns from interrupt

KEY:
NN00 = Any Suitable starting address.
PORTCO = Port control address.
PORTDA = Port data address.
IVECL = Low-byte of 16-bit interrupt vector (in port).
IVECH = High-byte of 16-bit interrupt vector (in I register).
IVEC = 16-bit interrupt vector formed by IVECH and IVECL.
IVEC + 1 = 16-bit address one location higher up in memory than IVEC.
SERVL = Interrupt service routine starting address-low byte.
SERVH = Interrupt service routine starting address-high byte.
MM00 = 16-bit starting address for interrupt service routine formed by SERVH and SERVL.
MEM = 16-bit address nominated for storing conversion results.
(Remember that the above 16-bit addresses need to be assembled in the order L0-byte, Hi-byte in the object code).

COMMENTS

Remember that the $\overline{WR}$ falling edge sets the MSB high and all the other bits low. Hence the µP must latch the conversion result before any further $\overline{WR}$ falling edges are generated - otherwise incorrect data could be latched! This arrangement is useful when acquiring data relatively infrequently, under the control of some external logic, and/or when the ZN448 is operated with a slow clock.

For evaluation purposes, a single-shot debounced $\overline{WR}$ pulse may be supplied. Data can then be examined for integrity.

INTERFACING ONE OR MORE ZN448/9s TO THE Z80.

When it is required to connect more than a single ZN448 to a port, some control must be exerted over the three-state outputs. This is easily achieved by connecting the $\overline{RD}$ inputs to the bit outputs from another port. The relevant port bits and thus the $\overline{RD}$ inputs, can then be taken low individually, to enable only the desired device.

Further, this controlling port can do other useful things for us, such as generating $\overline{WR}$ pulses (by taking the relevant port bit(s) low and back high) and checking for the end of a conversion by monitoring the $\overline{BUSY}$ output(s).

Setting some of the port bits as inputs and some as outputs takes advantage of the control mode (mode 3) of the port.

The enable/disable times of the converter outputs need not be considered, since they are much less than the Z80 instruction execution times .

DATA ACQUISITION UNDER PROGRAM CONTROL

Here one port is assigned to reading the data from the ZN448s and another port used to control the $\overline{RD}$ and $\overline{WR}$ inputs and to monitor the $\overline{BUSY}$ outputs.

As an example consider interfacing 2 x ZN448s as follows:

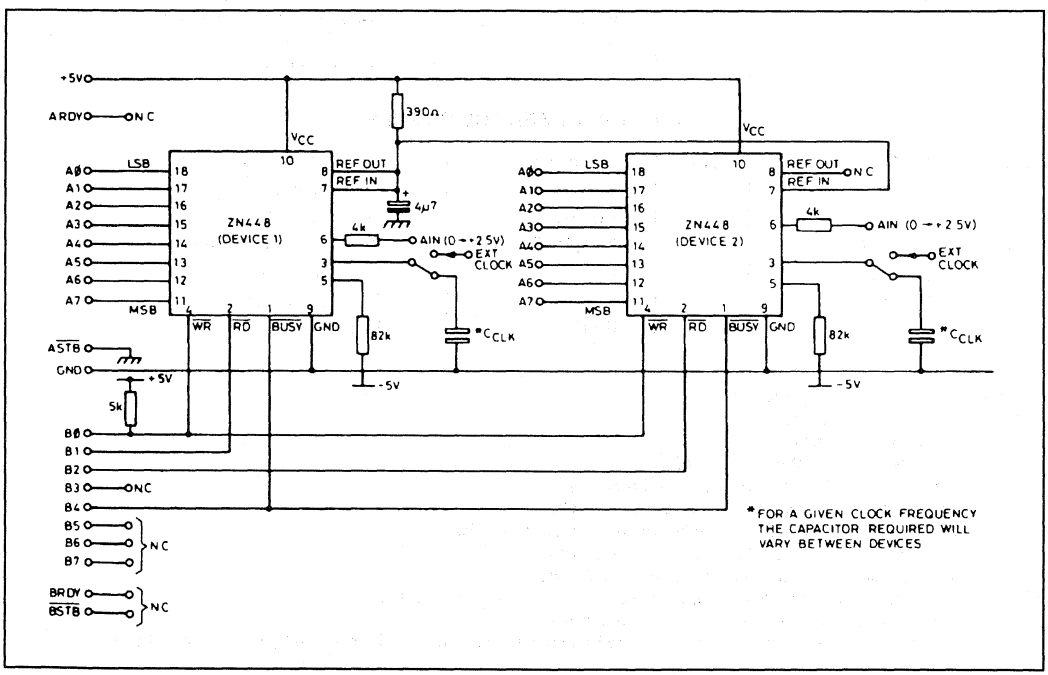


Fig.7 Interfacing 2 x ZN448s to the Z80 using both ports of a Z80 PIO - $\overline{BUSY}$'s polled

Note that in the circuit of Fig.7, the reference input ($V_{REF\ IN}$) of the second ZN448 is driven from the reference output ($V_{REF\ OUT}$) of the first ZN448. This provides excellent gain tracking between converters. Up to five ZN448s may be driven from a single internal reference without changing the reference resistor.

PROGRAM EXAMPLE

Here is a program to start the two ZN448s converting, then read and store the data when they have finished the conversion.

Conversion is initiated by taking B0 (= both $\overline{WR}$ inputs) low and then high. B4 (= both $\overline{BUSY}$s) is then polled until it is found to be high, thus indicating that both ZN448s have finished converting. Each device is then brought out of the three-state condition in turn - by taking B1 and B2 (= both $\overline{RD}$ inputs) low individually - to allow the data to be read.

PROGRAM STATEMENTS

```
:  Nominate memory locations for storing the conversion
   results.
:  It is assumed that both ports need initialising.
:  FEH=Take WR low word.
:  FDH = Select first ZN448 word.
:  FBH = Select second ZN448 word.
```

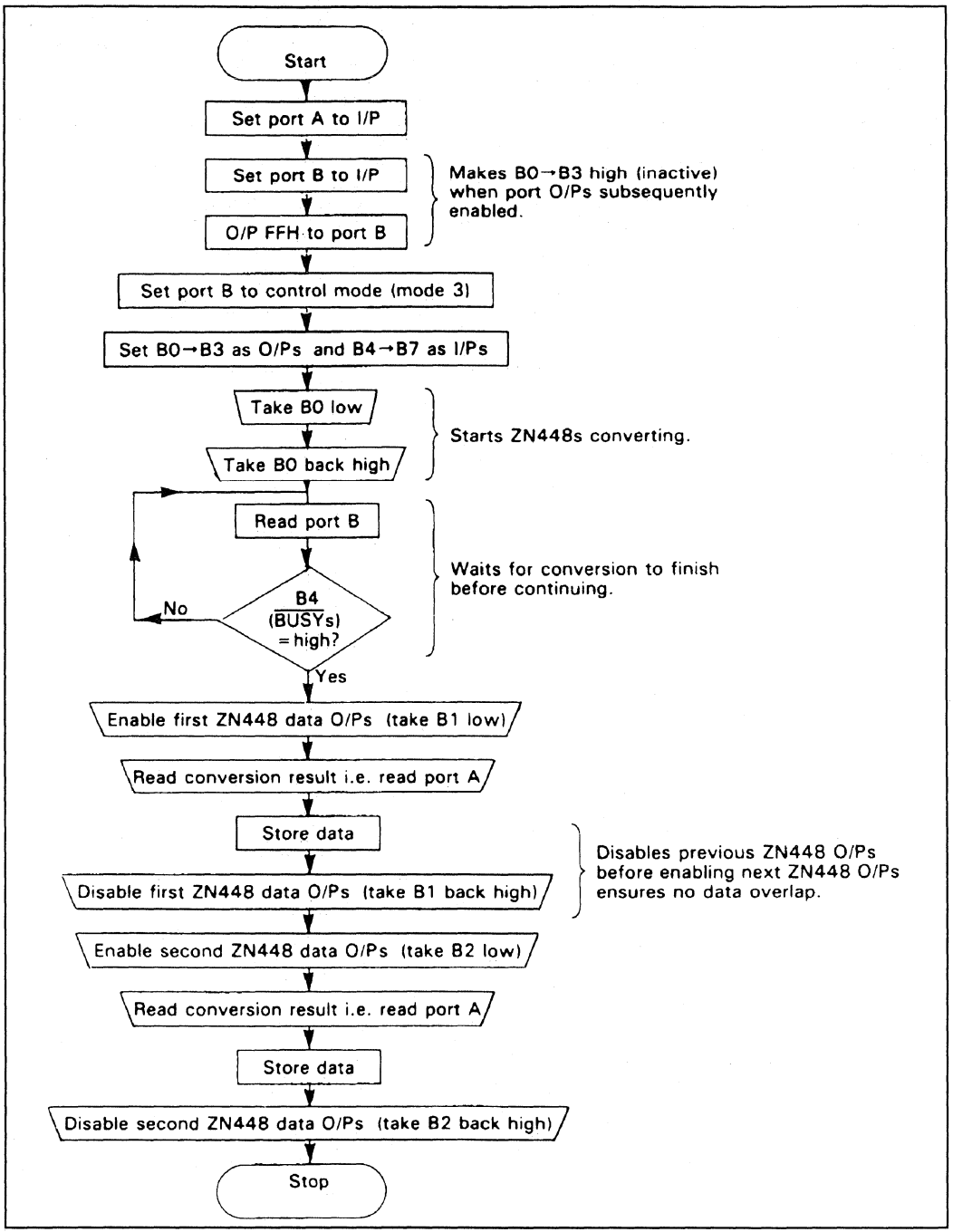


Fig.8 Flow chart 3

PROGRAM LISTING

PROGRAM 3

Address	Object code	Label	Source code	Comments
NN00	3E 4F		LD A, 4FH	Sets port to input (Mode 1)
NN02	D3 PORTCO1		OUT PORTCO1, A	
NN04	D3 PORTCO2		OUT PORTCO, A	Sets port B to input (mode 1)
NN06	3E FF		LD A, FFH	O/Ps FFH to port B (to make O/Ps inactive when first enabled)
NN08	D3 PORTDA2		OUT PORTDA2, A	
NN0A	3E CF		LD A, CFH	Sets port B to control mode (mode 3)
NN0C	D3 PORTCO2		OUT PORTDA2, A	
NN0E	3E F0		LD A, F0H	Sets B0→B3 as O/Ps and B4→ B7 as I/Ps
NN10	D3 PORTCO2		OUT PORTDA2, A	
NN12	3E FE		LO A, FEH	Takes B0 low and then back high to start devices converting
NN14	D3 PORTDA2		OUT PORTDA2, A	
NN16	3E FF		LD A, FFH	
NN18	D3 PORTDA2		OUT PORTDA2, A	
NN1A	DB PORTDA2	POLL	IN A, PORTDA2	Waits for $\overline{BUSY}$s to go high before contimuing
NN1C	CB 67		BIT 4, A	
NN1E	28 FA		JR Z, POLL	
NN20	3E FD		LD A, FDH	Takes $\overline{RD}$ low on first ZN448
NN22	D3 PORTDA2		OUT PORTDA2, A	
NN24	DBPORTDA1		IN A, PORTDA1	Reads and stores first ZN448 conversion result
NN26	32 MEM1		LD (MEM1), A	
NN29	3E FF		LD A, FFH	Takes $\overline{RD}$ back high
NN2B	D3 PORTDA2		OUT PORTDA2, A	
NN2D	3E FB		LD A, FBH	Takes $\overline{RD}$ low on second ZN448
NN2F	D3 PORTDA2		OUT PORTDA2, A	
NN31	DBPORTDA1		IN A, PORTDA1	Reads and stores second ZN448 conversion result
NN33	32 MEM2		LD (MEM2), A	
NN36	3E FF		LD A, FFH	Takes RD back high
NN38	D3 PORTDA2		OUT PORTDA2,A	
NN3A	?		?	Returns to monitor (command(s) system dependant)

KEY:
NN00 = Any Suitable starting address.
PORTCO1 = Port A control address.
PORTCO2 = Port B control address.
PORTDA1 = Port A data address.
PORTDA1 = Port A data address.
MEM1 = 16-bit address nominated for storing first ZN448 data.
MEM2 = 16-bit address nominated for storing second ZN448 data.
(Remember that MEM1 and MEM2 need to be assembled in the order Lo-byte, Hi-byte in the object code).

COMMENTS

The principles illustrated in program 3 can be extended to allow the interfacing of more ZN448s. In fact it can immediately be seen that there are four port B lines spare that can be used for this purpose.

Further, up to three $\overline{BUSY}$ outputs can be connected to a single port bit and likewise up to three $\overline{WR}$ inputs can be driven from a single port bit - but here the pull-up resistor may need reducing to 2.4K. (If a CMOS PIO is used, the pull-up resistor can be dispensed with).

We can readily interface four ZN448s by using two port lines to drive the WR inputs and two port lines to monitor the $\overline{BUSY}$ outputs. The remaining four port lines connecting to the $\overline{RD}$ inputs and being used to select the required ZN448.

If the $\overline{BUSY}$ outputs are not polled and a software delay is used instead (covered in the section on interfacing a single ZN448/9), we can interface up to 6 devices. Two of the port lines will be needed to drive the 6 $\overline{WR}$ inputs and the remaining 6 lines will again be used to enable the required ZN448.

The leakage current of the ZN448 three-state outputs need not concern us ($\pm$ 2μA max. at 2V).

If the software needs changing to suit a particular hardware setup, the above principles are still applicable i.e.:

- Initiate conversions bv taking the relevant port bit(s) assigned to the WR inputs low and back high .
- Ensure that conversion is over before reading the result - by polling the $\overline{BUSY}$ outputs (or using a software delay).
- Enable the ZN448s individually (to prevent contention) - by taking the appropriate port bit(s) and hence $\overline{RD}$ inputs low individually - and read the conversion result.

In practice it may be that we are interested in only one of the ZN448s at a particular time. Here, though we may start several devices converting at the same time, we can just ignore the others and read only the desired device.

DATA ACQUISITION UNDER INTERRUPT CONTROL

As discussed in the previous section on interrupts, the ZN448 is not a slow peripheral and hence does not need to be interrupt driven. However if it is wished to utilise the ZN448 relatively infrequently - under the control of some timing logic - then interrupts become more useful. This is considered in this section.

Here one port is assigned to reading the data from the ZN448s and another port is used to control the $\overline{RD}$ inputs and to monitor the $\overline{BUSY}$ outputs. In fact we can set the port to generate an interrupt when only one of a number of port bits go high. Thus we can generate an interrupt when a $\overline{BUSY}$ goes high. In order to get these facilities the port needs setting to its control mode (mode 3).

Care must be taken when using a port to generate interrupts in this manner. This is because the bits set to give the interrupt, must first all be low, before an interrupt can be generated on any of them going high. Also if any of these bits remain high, further interrupts will be prevented. Therefore, the relevant port bits must be set low initially and must also be set back low after the interrupting device has been serviced. This means that for our purposes, we must ensure that the $\overline{WR}$ inputs and hence the $\overline{BUSY}$ outputs, are low initially and are set back low again after servicing. This can be achieved using positive edge triggered D-type flip-flops with preset and clear inputs - see below. (Remember that $\overline{BUSY}$ is held low by a low on the $\overline{WR}$ input and goes high at the end of a conversion) .

An example, consider interfacing two ZN448s as follows:

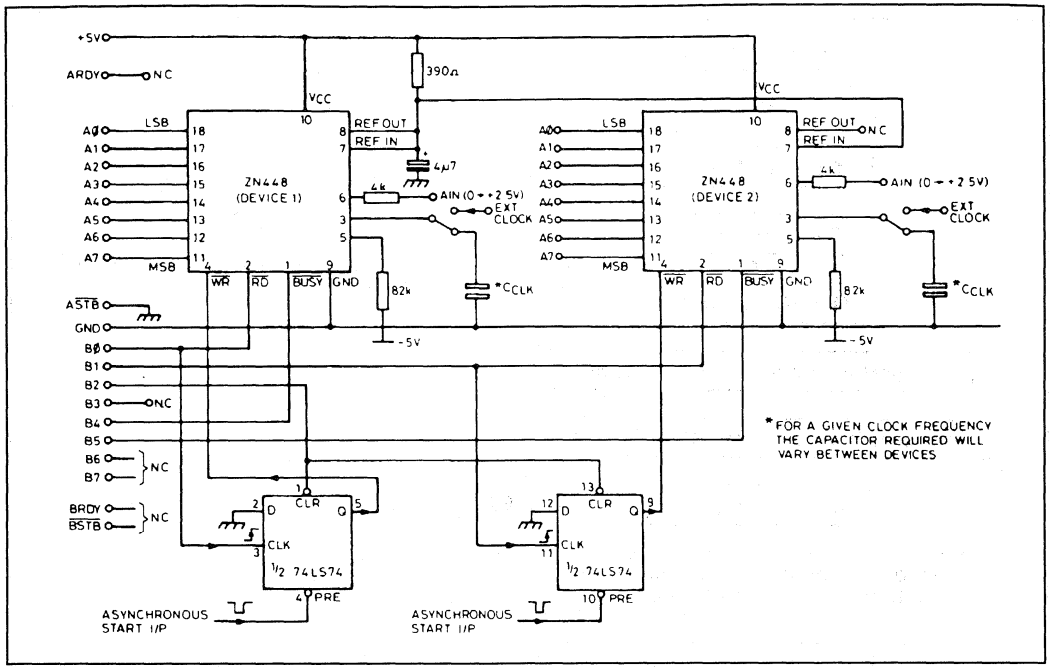


Fig.9 Interfacing 2 x ZN448s to the Z80 using both ports of a Z80 PIO - interrupt driven

(Note that again one reference is used to drive both devices, as in the previous section).

In the circuit of Fig.9, B2 is used to clear the $\overline{\text{BUSY}}$s initially and the rising edge of the relevant $\overline{\text{RD}}$ signal is used to clear the $\overline{\text{BUSY}}$s after servicing (as described below). Thus complying with the above requirements.

The falling edge of the asynchronous start input signal from the timing logic, forces the Q output high on the associated D-type flip-flop. Hence the $\overline{\text{WR}}$ input, which was previously low, is now taken high and this starts a conversion. At the end of the conversion the $\overline{\text{BUSY}}$ output goes high and this is used to generate our interrupt.

During the service routine, the $\overline{\text{RD}}$ input on a given device is taken low to enable the outputs, and then back high after the data has been latched into port A. Thus an $\overline{\text{RD}}$ positive edge is generated every time a device is read. This edge clocks a low through to the Q output on the appropriate D-type, and hence takes the relevant $\overline{\text{WR}}$ input and $\overline{\text{BUSY}}$ output low.

For correct clearing of the $\overline{\text{BUSY}}$s and hence correct operation, the asynchronous start input signals must:

(i) be inactive (high) when the CLR inputs on the D-types (B2) are low initially.

(ii) have returned back high after initiating a conversion, before the associated $\overline{\text{RD}}$ positive edge occurs.

PROGRAM EXAMPLE

This program vectors to an interrupt service routine on the occurrence of an interrupt. The service routine then reads and stores the data from the interrupting ZN448(s).

Conversion is initiated by the users timing logic and an interrupt is generated when one or more of the $\overline{\text{BUSY}}$ outputs goes high.

The µP is set to interrupt mode 2 as the ports are designed to be used with this mode. The contents of the I register and the port interrupt vector are combined by the µP to form a 16-bit vector. This vector is then used to look up the starting address of the interrupt service routine. The µP then loads the program counter with this address and continues program execution from this location.

PROGRAM STATEMENTS

```
:  It is assumed that the user initiates conversion correctly
   when required.
:  It is assumed that both ports need initialising.
:  Nominate memory locations for the vectored address, the
   interrupt service routine and for storing the conversion
   results.
:  FEH = Select first ZN448 word.
:  FDH = Select second ZN448 word.
:  FBH = Clear BUSY outputs word.
```

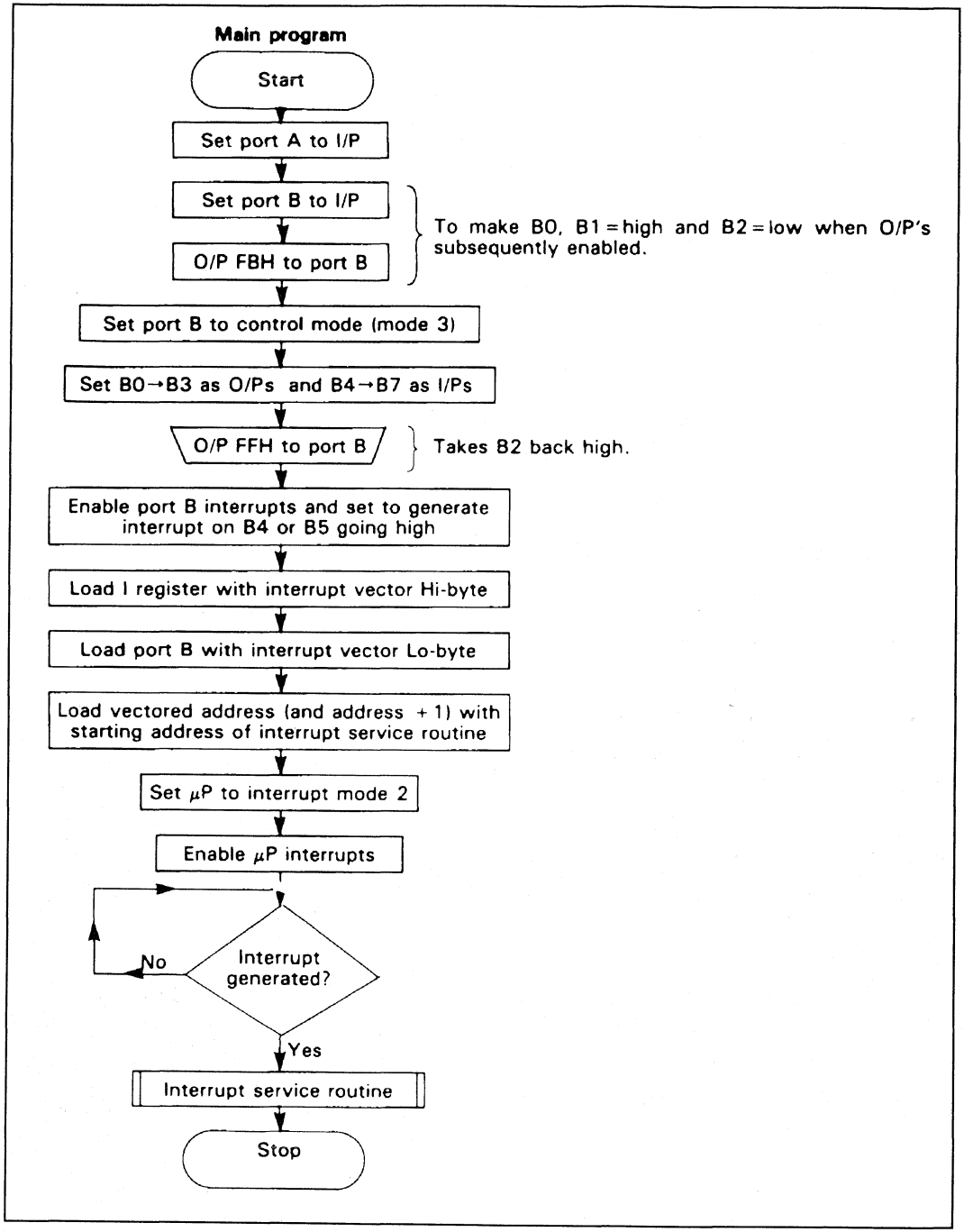


Fig. 10a Flow chart 4

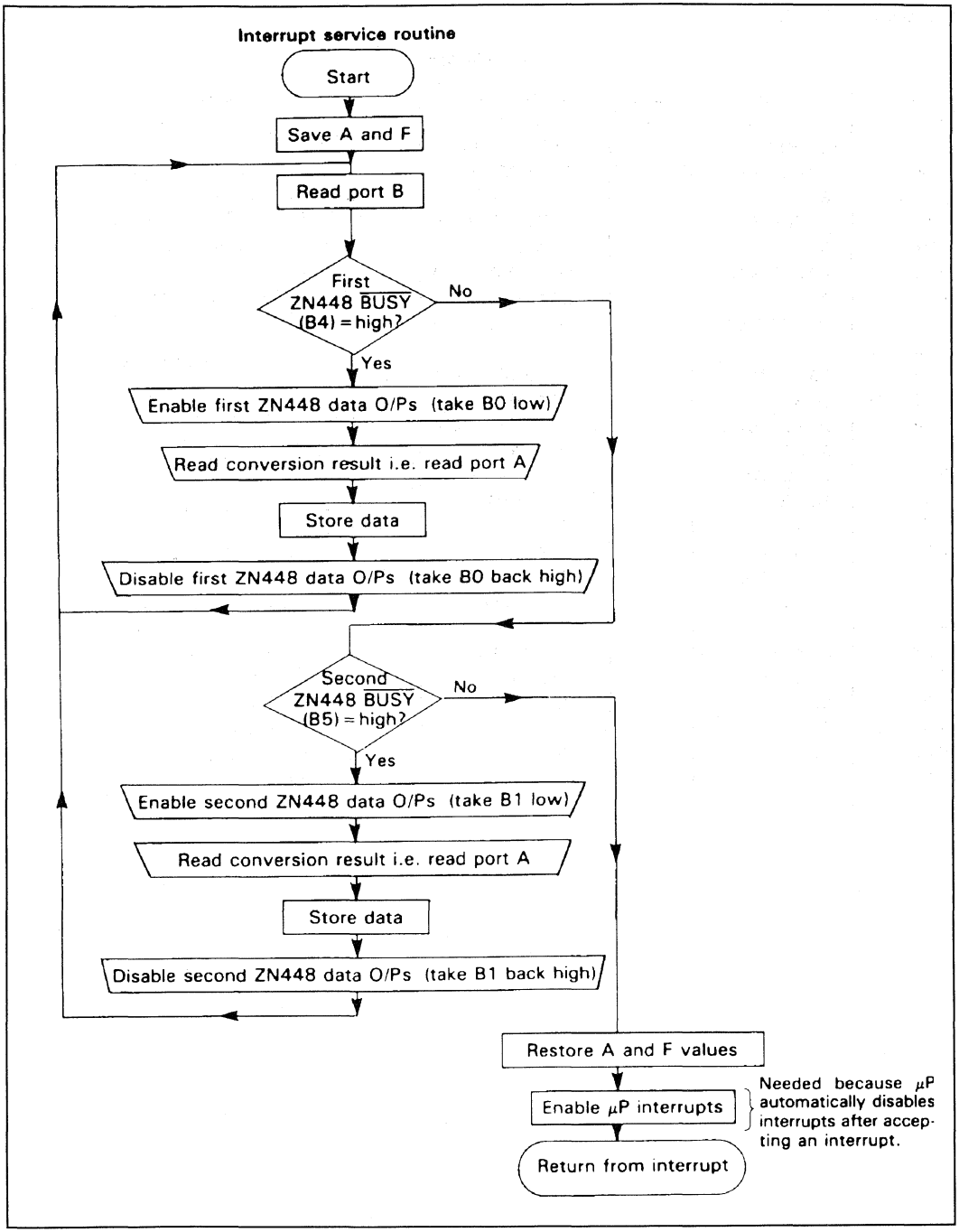


Fig.10b Flow chart 4 (cont.)

PROGRAM LISTING

PROGRAM 4

Address	Object code	Label	Source code	Comments
NN00	3E 4F		LD A, 4FH	Sets port A to input (Mode 1)
NN02	D3 PORTCO1		OUT PORTCO1, A	
NN04	D3 PORTCO2		OUT PORTCO2, A	Sets port B to I/P (mode 1) and sets CLR on D-types to go low when port O/Ps enabled
NN06	3E FB		LD A, FBH	
NN08	D3 PORTDA2		OUT PORTDA2, A	
NN0A	3E CF		LD A, CFH	Sets port B to control mode (mode 3)
NN0C	D3 PORTCO2		OUT PORTCO2, A	
NN0E	3E F0		LD A, F0H	Sets B0→B3 as O/Ps and B4→ B7 as I/Ps
NN10	D3 PORTCO2		OUT PORTCO2, A	
NN12	3E FF		LO A, FFH	Takes CLR on D-types back high
NN14	D3 PORTDA2		OUT PORTDA2, A	
NN16	3E B7		LD A, B7H	Sets port B to generate Int. on B4 or B5 going high, also enables port interrupts
NN18	D3 PORTCO2		OUT PORTCO2, A	
NN1A	3E CF		LD A, CFH	
NN1C	D3 PORTCO2		OUT PORTCO2, A	
NN1E	3E IVECH		LD A, IVECH	Loads I reg. with interrupt vector Hi-byte
NN20	ED 47		LD I, A	
NN22	3E IVECL		LD A, IVECL	Loads port B with interrupt vector Lo-byte
NN24	D3 PORTCO2		OUT PORTCO2, A	
NN26	3E SERVL		LD A, SERVL	Loads vectored address (and next consecutive address) with starting address of interrupt service routine
NN28	32 IVEC		LD (IVEC), A	
NN2B	3E SERVH		LD A, SERVH	
NN2D	32 IVEC + 1		LD (IVEC + 1), A	
NN30	ED 5E		IM 2	Sets µP to interrupt mode 2
NN32	FB		EI	Enables µP's interrupts
NN33	76		HALT	Waits for Interrupt (or reset!)
NN34	?		?	Returns to monitor (command(s) system dependant)

PROGRAM LISTING

PROGRAM 4 (cont.)
Interrupt service routine

Address	Object code	Label	Source code	Comments
MM00	F5		PUSH AF	Saves current values of A and F
MM01	DN PORTDA2	POLL1	IN A, PORTDA2	Reads port B
MM03	CB 67		BIT 4, A	Tests B4 and jumps if B4 = 0
MM05	28 0F		JR Z, POLL2	
MM07	3E FE		LD A, FEH	Selects first ZN448
MM09	D3 PORTDA2		OUT PORTDA2, A	
MM0B	DB PORTDA1		IN A, PORTDA1	Reads and stores first ZN448 data
MM0D	32 MEM1		LD (MEM1), A	
MM10	3E FF		LD A, FFH	Puts first ZN448 O/Ps back into high impedance state
MM12	D3 PORTDA2		OUT PORTDA2, A	
MM14	18 EB		JR, POLL1	Jumps back to read port B
MM16	CB 6F	POLL2	BIT 5, A	Tests B5 and jumps if B5 = 0
MM18	28 0F		JR Z, RETURN	
MM1A	3E FD		LD A, FDH	Selects second ZN448
MM1C	D3 PORTDA2		OUT PORTDA2, A	
MM1E	DB PORTDA1		IN A, PORTDA1	Reads and stores second ZN448 data.
MM20	32 MEM2		LD (MEM2), A	
MM23	3E FF		LD A, FFH	Puts second ZN448 O/Ps back into high impedance state
MM25	D3 PORTDA2		OUT PORTDA2, A	
MM27	18 D8		JR, POLL1	Jumps back to read port B
MM29	F1	RETURN	POP AF	Restores A and F values
MM2A	FB		EI	Re-enables µP Int's.
MM2B	ED 4D		RETI	Return from Int.

KEY:
NN00 = Any Suitable starting address.
PORTCO1 = Port A control address.
PORTCO2 = Port B control address.
PORTDA1 = Port A data address.
PORTDA2 = Port B data address.
IVECL = Low-byte of 16-bit interrupt vector (in port).
IVECH = High-byte of 16-bit interrupt vector (in I register).
IVEC = 16-bit interrupt vector formed by IVECH and IVECL.
IVEC + 1 = 16-bit address one location higher up in memory than IVEC.
SERVL = Interrupt service routine starting address-low byte.
SERVH = Interrupt service routine starting address-high byte.
MM00 = 16-bit starting address for interrupt service routine formed by SERVH and SERVL.
MEM1 = 16-bit address nominated for storing first ZN448 data.
MEM2 = 16-bit address nominated for storing second ZN448 data.
(Remember that the above 16-bit addresses need assembling in the order Lo-byte, Hi-byte in the object code).

COMMENTS

The principles illustrated above can be extended to allow more ZN448s to be interrupt driven in this manner. Readily we can interface three ZN448s with each $\overline{RD}$ and $\overline{BUSY}$ allocated to their own port bit. Further if we clear the $\overline{BUSY}$ outputs by some method which does not use one of the port bits, we can interface four ZN448s. (For example we could pulse the CLR inputs low on the D-types, by writing to an address dedicated to this purpose).

It is important to realise that in the above example, the μP was not allowed to return from the service routing until both $\overline{BUSY}$s were low simultaneously. This is to ensure that none of them remain high and inhibit further interrupts! Regardless of how many ZN448s are being interfaced, the same applies i.e. ensure that all $\overline{BUSY}$s are low before returning from the service routine.

The software may need modifying to suit a particular hardware setup. If so, then in addition to the above, it should be ensured that the $\overline{BUSY}$ outputs are cleared initially and after device servlcing .

The leakage current of the ZN448 three-state outputs need not concern us (± 2μA max. at 2V) .

FURTHER CONSIDERATIONS

Some sections of the above programs can be separated out and placed in the users initialisation routines i.e. they do not need repeating once proper initialisation has been achieved. Also the above programs were ended in some "return to monitor' commands. However in a real environment, sections of the programs will probably form part of a subroutine or loop, or part of a service routine.

The data acquired in the above examples was put straight into memory. It could instead have been processed and then either stored or outputted to another port.

In the examples given, where the $\overline{RD}$ inputs are controlled by port bits, these bits could be further decoded, thus extending their addressing range. This would also have the benefit of preventing the outputs from more than one device being enabled together (should an erroneous word be accidentally written to that port).

Again when the ZN448 three-state outputs are controlled, various other devices can be connected to the port that reads the data. This port could also be swapped between input and output modes - provided proper control is exerted .

In the foregoing description, port A has been used for reading the data and port B for controlling/monitoring the ZN448s. These ports could be interchanged or could even be from different PIOs.

SUMMARY

This report describes the versatility with which the ZN448/9 A-D converters can be interfaced with the Z80μP. Clearly, there are many other ways of storing and processing the acquired data. The user can tailor these to suit her/his own particular requirements.

Most of the above principles can also be applied when interfacing the ZN448/9 to other popular μPs. Full Engineering and Applications support is available to assist with technical queries relating to the applications of any of our data converter products.

Section 10
Package Outlines

NOTES

1. Dimensions are shown thus: mm (in).
2. Unless otherwise indicated, controlling dimensions are in inches.
3. All package outline diagrams are for guidance only. Please contact your nearest GPS Customer Service Centre for further information.

GEC PLESSEY
SEMICONDUCTORS

Packaging and coding

Lead finish

Devices will be supplied with the following lead finishes as standard:

Package Type	Lead Finish (MIL-M-38510 3.5.6.3.2)
Metal Can (CM)	Gold plate over Nickel plate
Sidebrazed Ceramic DIL (DC)	
Ceramic DIL (DG)	Hot solder dip over Tin plate

ESD protection

GEC Plessey Semiconductors considers all devices to be sensitive to electrostatic discharge to varying degrees (but at least to category A). All units are therefore marked with the equilateral triangle ESD sensitivity indicator.

In addition, all devices are packaged and shipped in conductive material or packaged in anti-static material with an external field shielding barrier in accordance to MIL-M-38510.

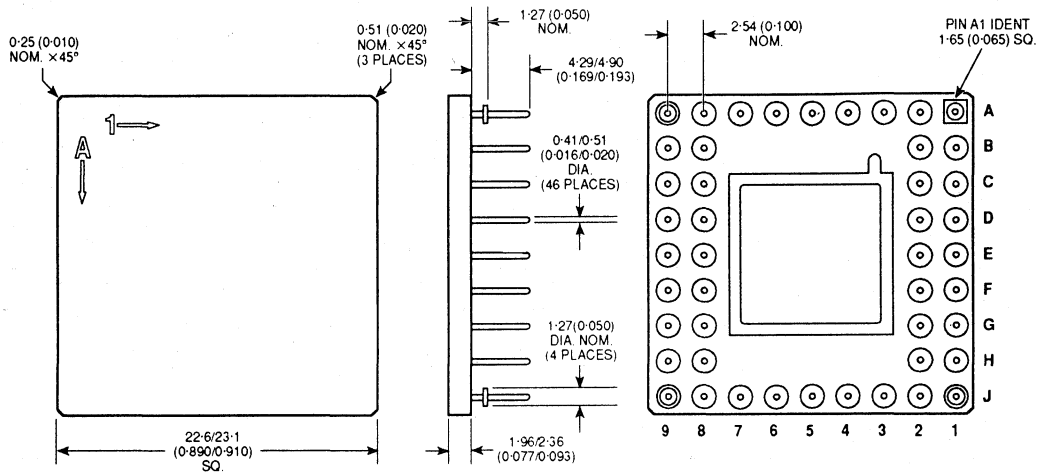
Device marking

All devices are marked with the following coding:

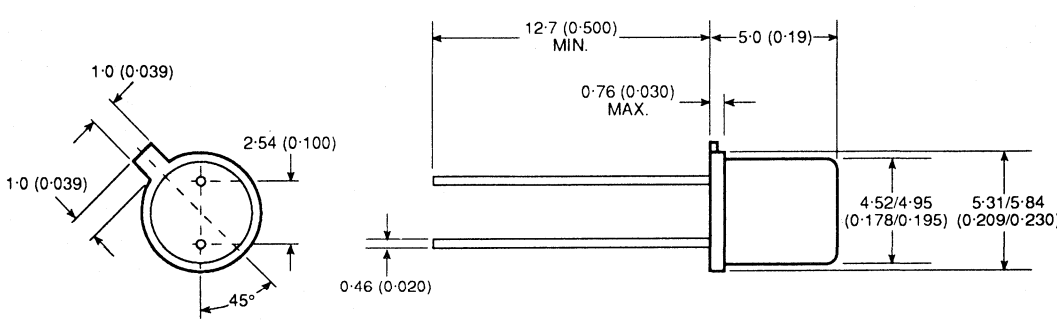
1. GPS logo or 'GPS' (manufacturer's identity).
2. ESD sensitivity indicator (equilateral triangle).
3. Date code (per MIL-M-38510).
4. Assembley lot identifier. Suffix letter added to date code indicating lot identity within production week.
5. Device type number - 'AC' indicating a MIL-STD-883 Class B compliant device.
6. Process/Assembly site identifier (two-letter code). Initial letter 'S' indicates GPS Swindon UK Wafer Process site. Second letter 'J' indicates GPS Swindon assembly site.
7. Pin 1 identifier. This may be either a package notch or dot for dual-in-line packages, gold corner for leadless chip carriers or tab for metal can packages.

Package Codes

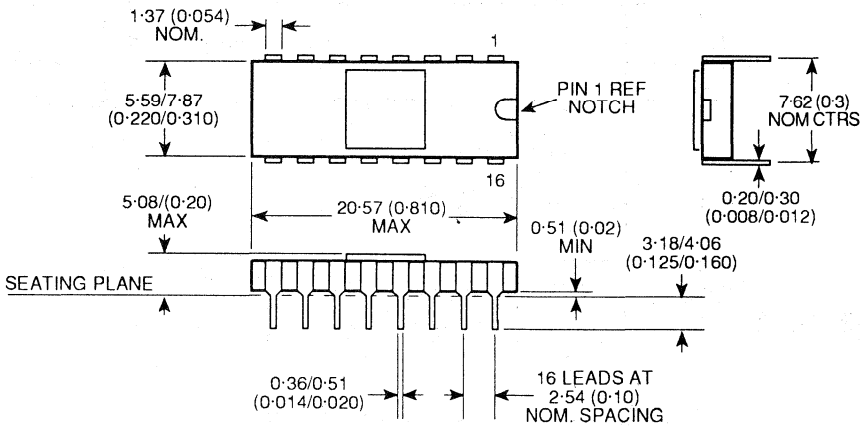
Code	Type	Description
AC	PGA	Pin Grid Array, multi-layer ceramic, metal sealed lid, through board.
CM	TO-n	Cylindrical multi-lead metal can.
DC	DILMON	Dual-in-line, multi-layer ceramic, sidebrazed leads, metal sealed lid, through board.
DG	CERDIP	Dual-in-line, ceramic body, Alloy 42 leadframe, glass sealed, through board.
DP	PLASDIP	Dual-in-line, Copper or Alloy 42 leadframe, plastic moulded, through board.
GP	PQFP	Four sided, Plastic Quad Flat Pack. 'Gullwing' formed leads, surface mount.
HG	Quad Cerpack	Glass sealed ceramic chip carrier, J-formed leads on four sides, surface mount.
HP	PLCC	Plastic moulded chip carrier, J-formed leads on four sides, surface mount.
MP	Small Outline	Dual-in-line, plastic moulded, 'Gullwing' formed leads, metal sealed lid, surface mount.
SOT-23	Small Outline	3-lead miniature plastic, 'Gullwing' formed leads, surface mount.
TO-92		3-lead plastic through-board.



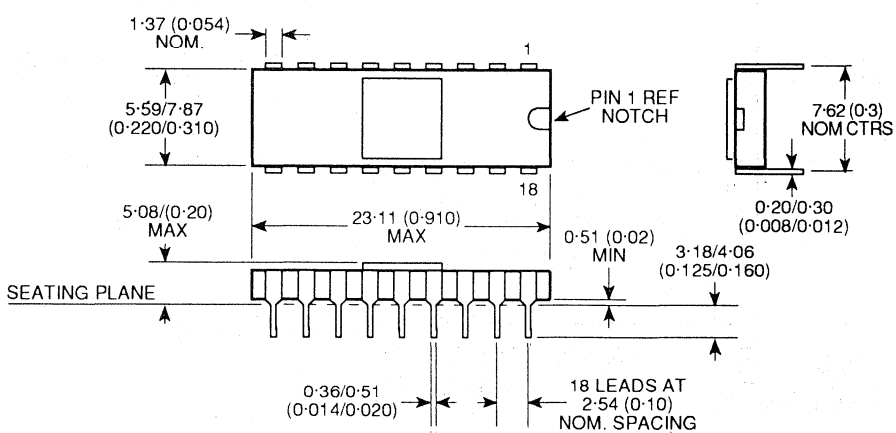
46-PIN GRID ARRAY PACKAGE - AC46



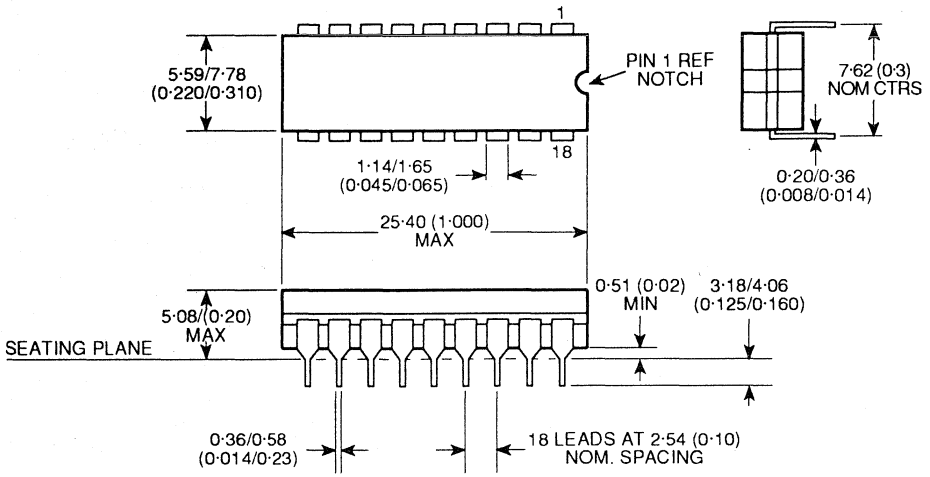
2-LEAD METAL CAN - CM2



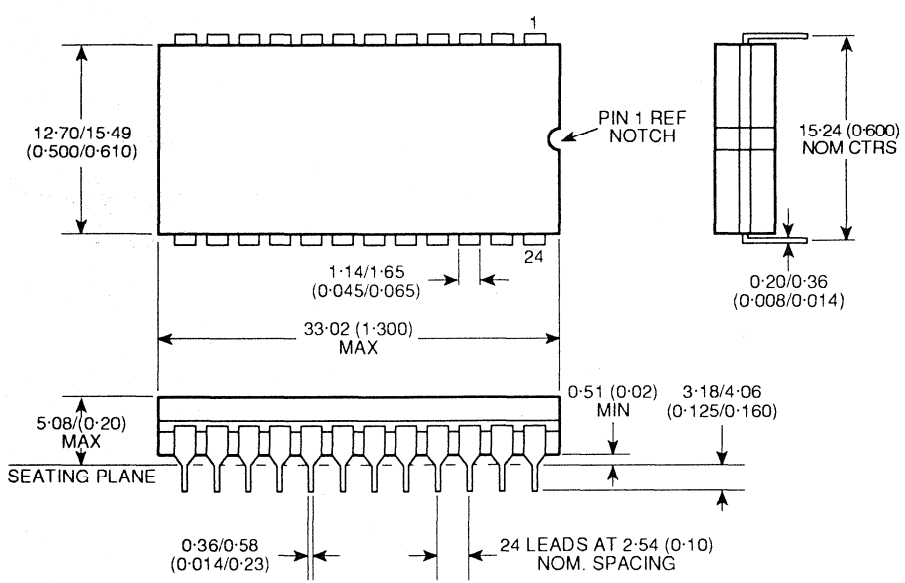
16-LEAD SIDEBRAZED CERAMIC DIL - DC16



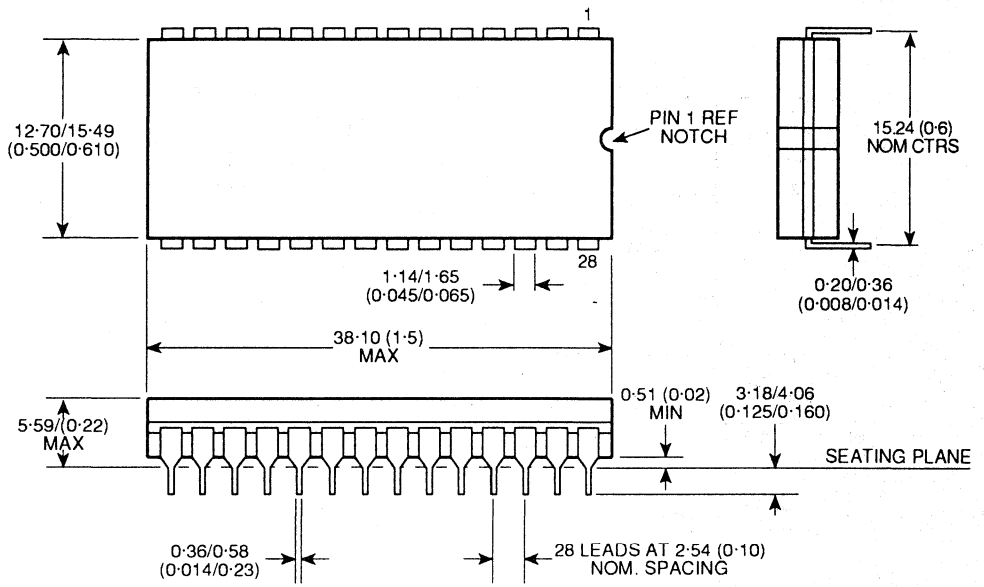
18-LEAD SIDEBRAZED CERAMIC DIL - DC18



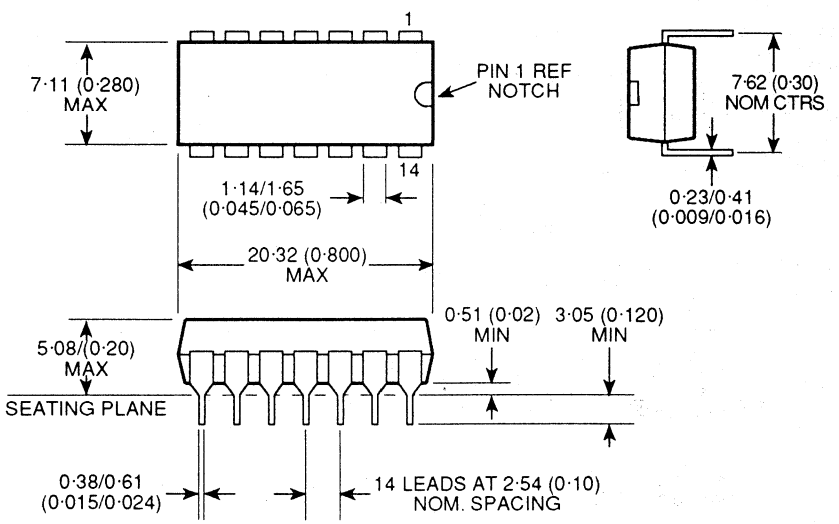
18-LEAD CERAMIC DIL - DG18



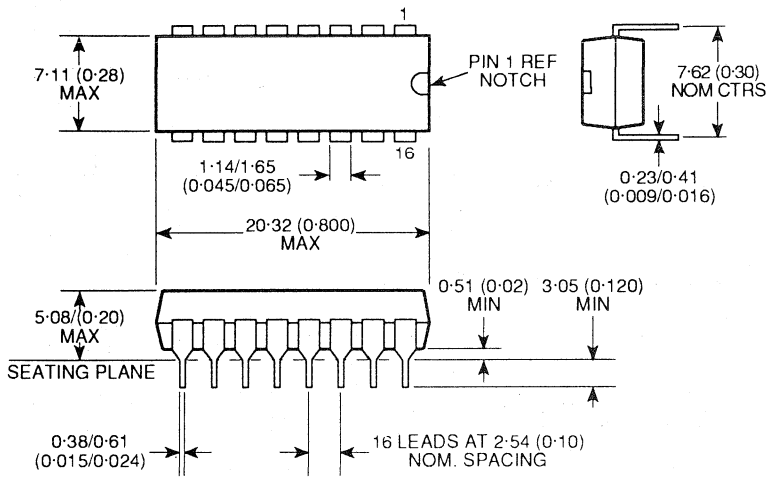
24-LEAD CERAMIC DIL - DG24



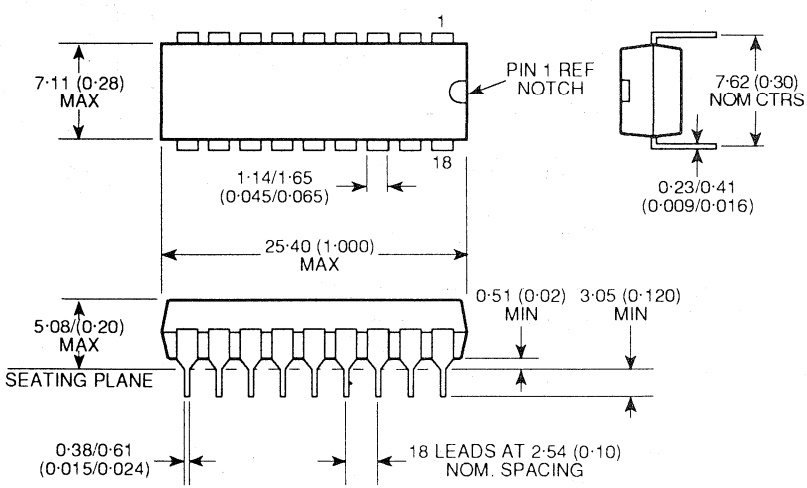
28-LEAD CERAMIC DIL - DG28



14-LEAD PLASTIC DIL - DP14



16-LEAD PLASTIC DIL - DP16



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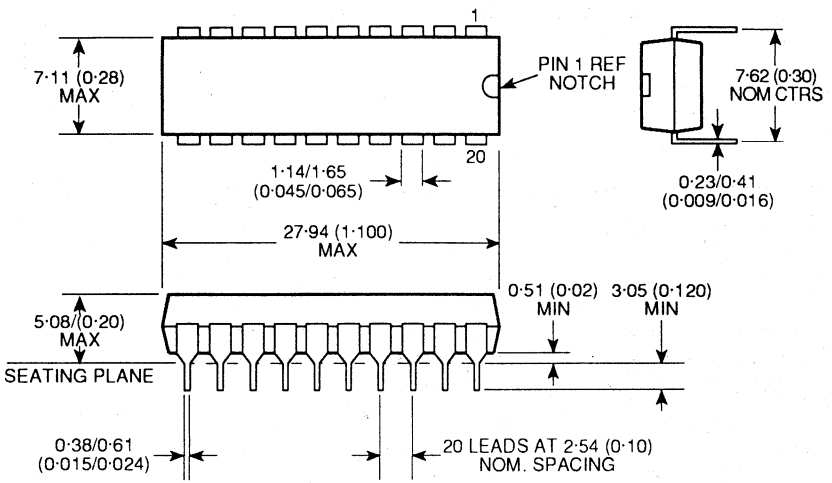

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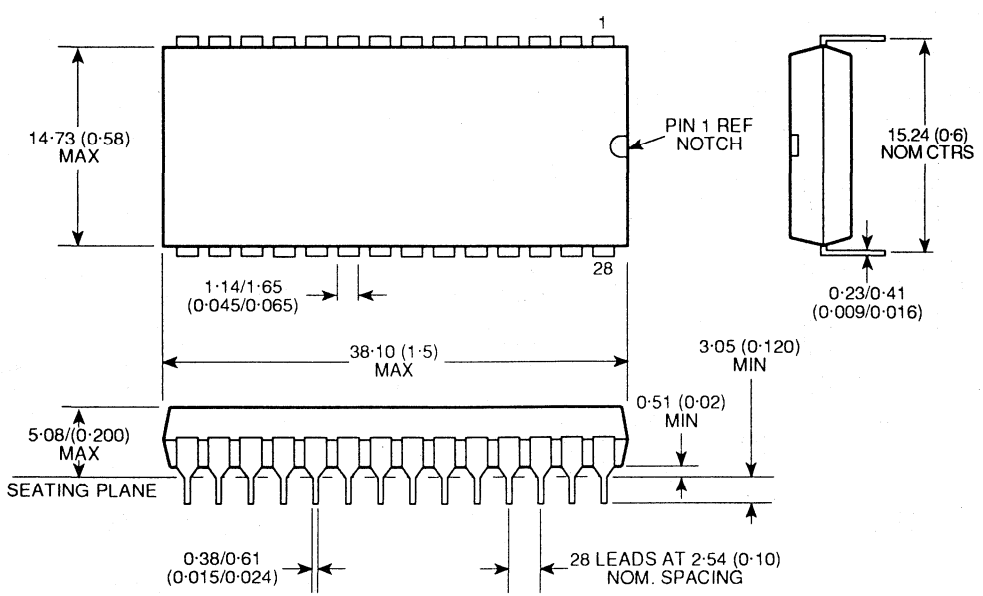

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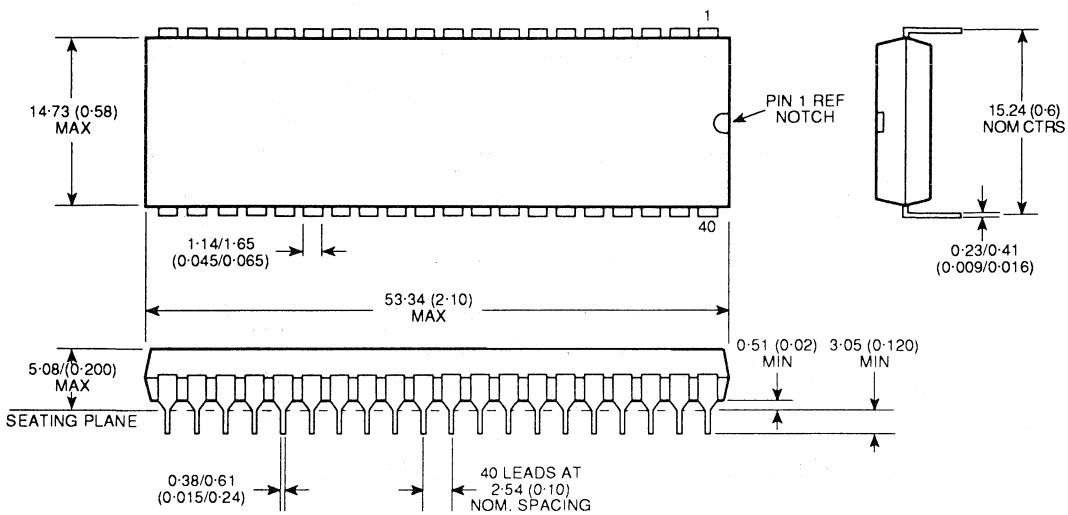

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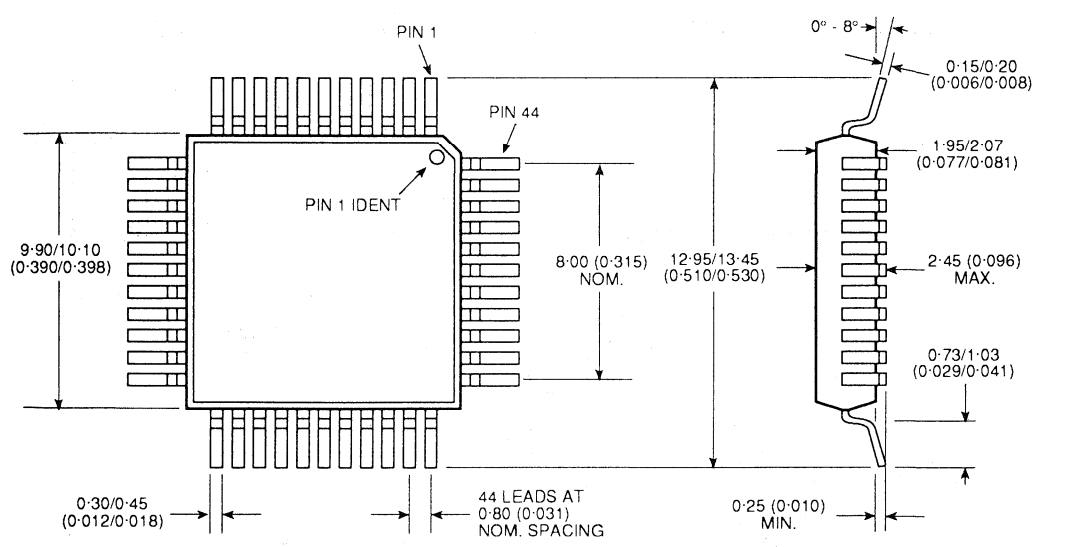
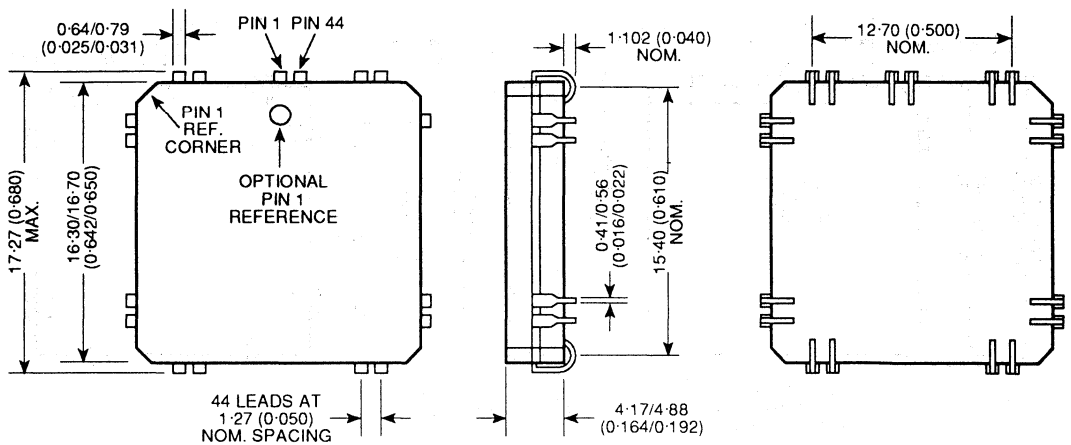


NOTE: Controlling dimensions are millimetres

44-LEAD PLASTIC QUAD FLATPACK - GP44



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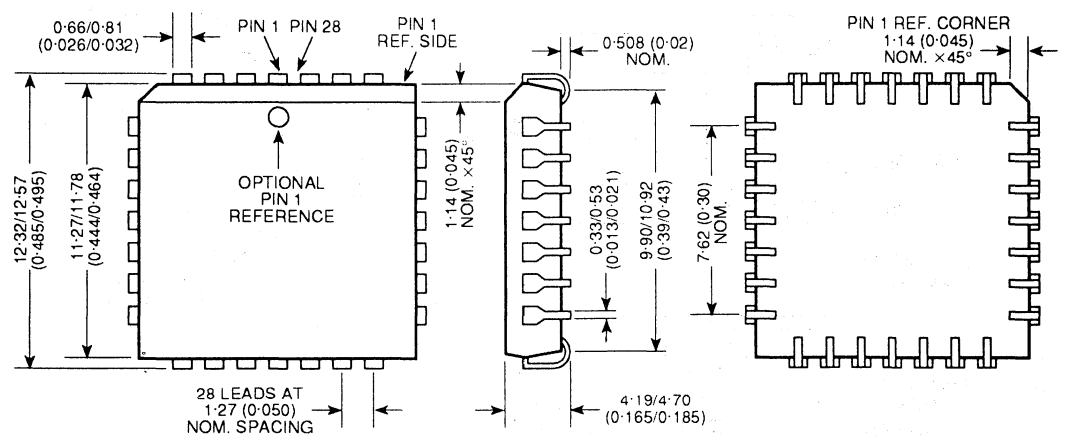

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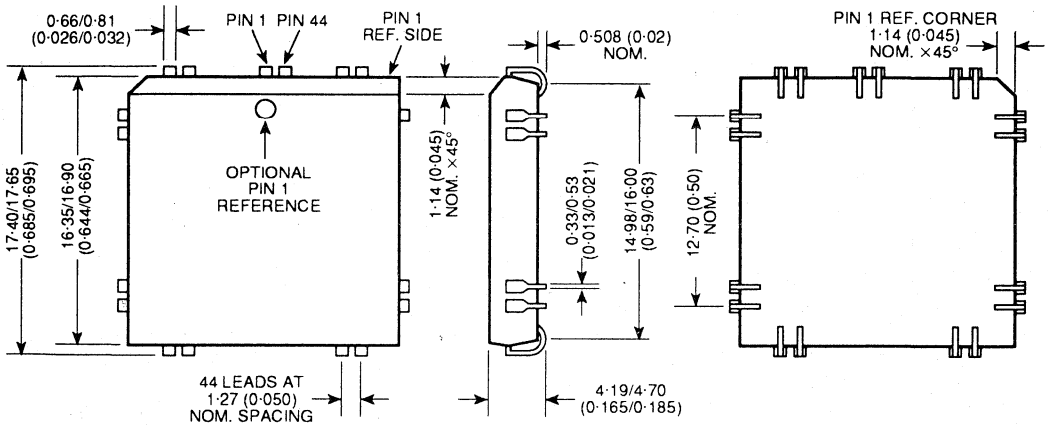

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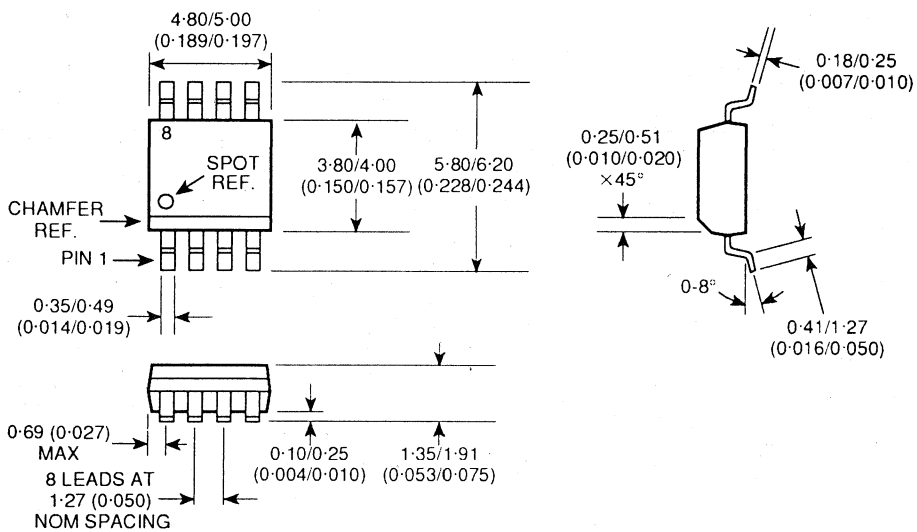
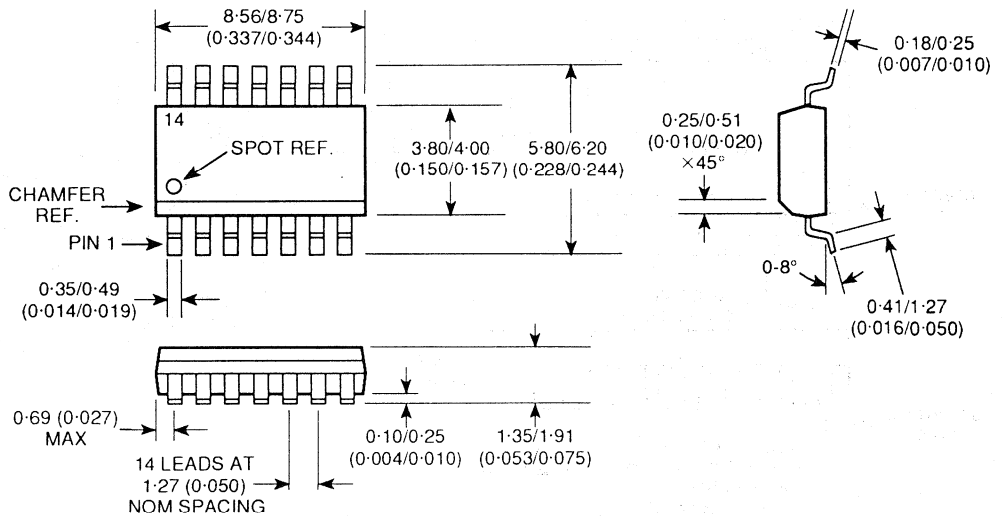


8-LEAD MINIATURE PLASTIC DIL - MP8



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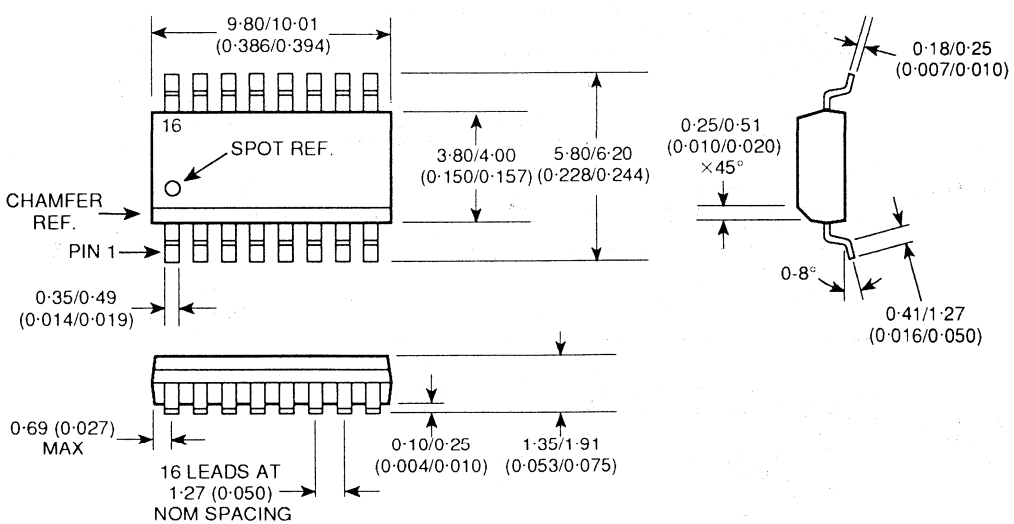

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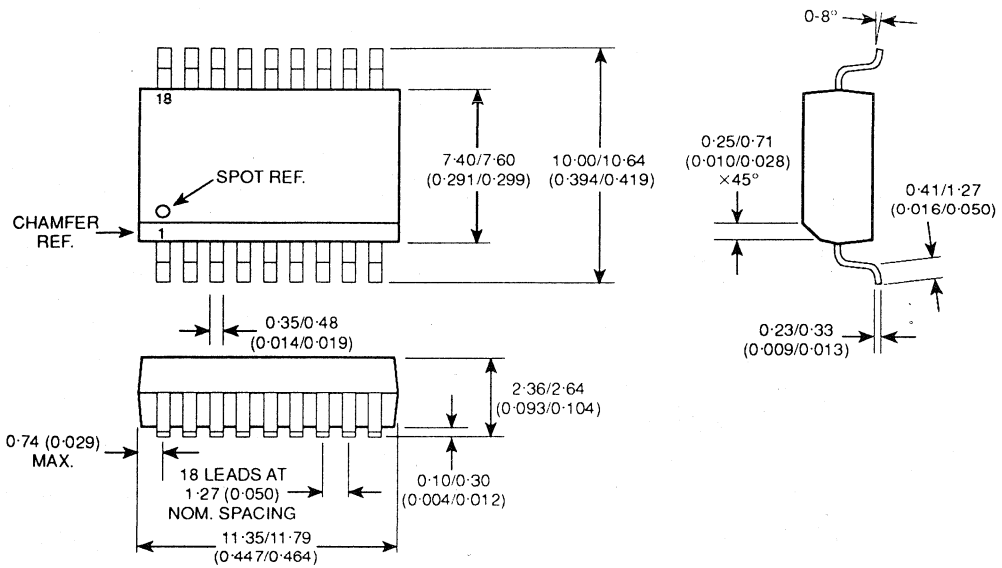

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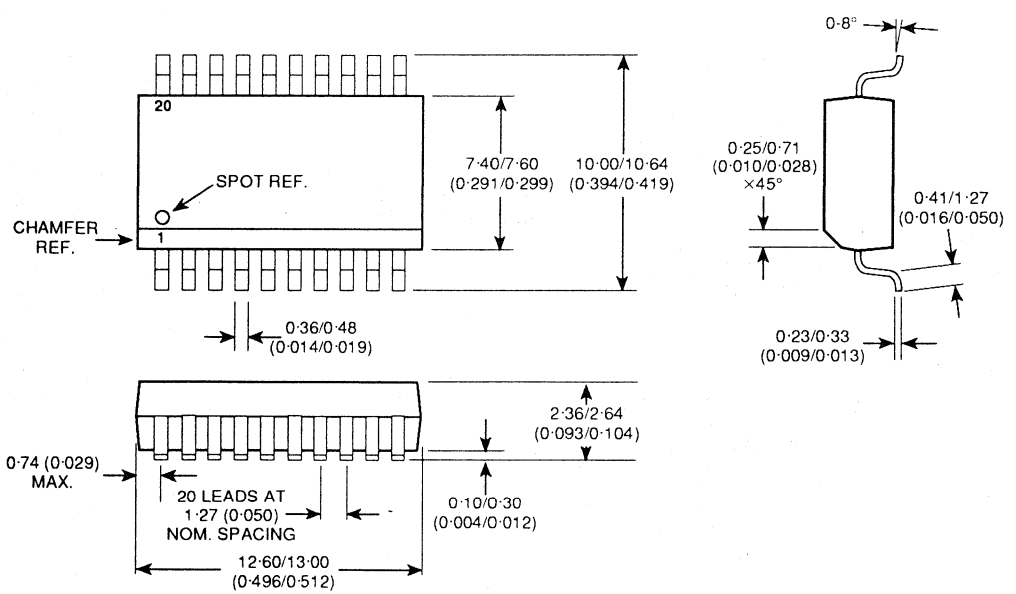

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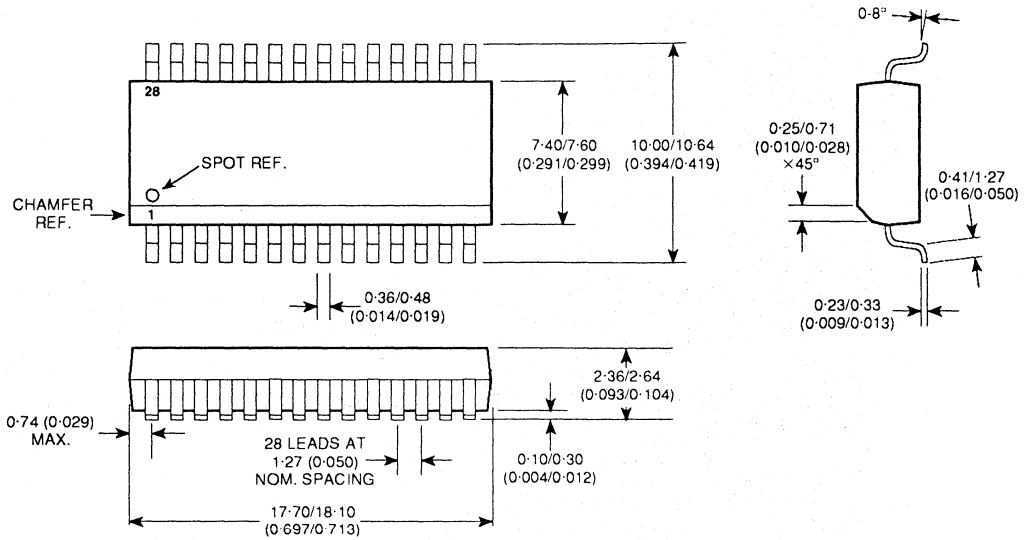

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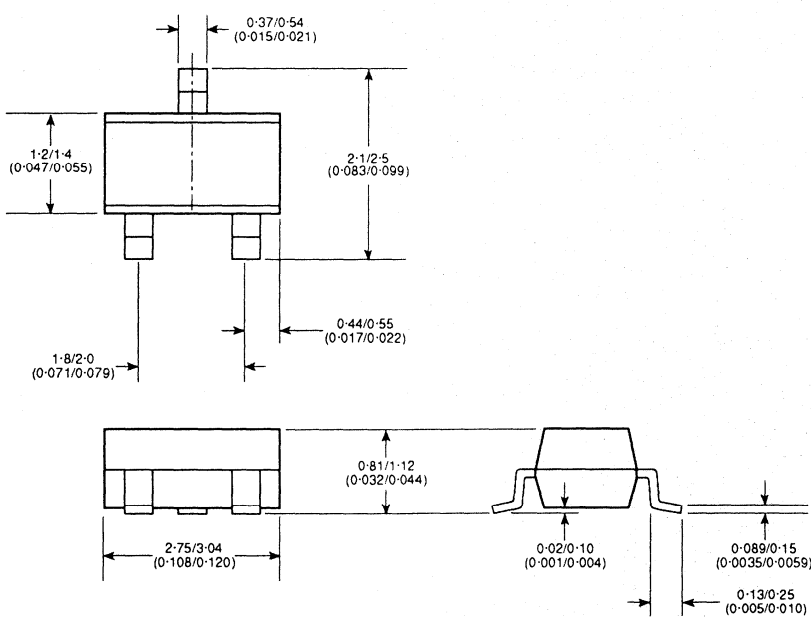
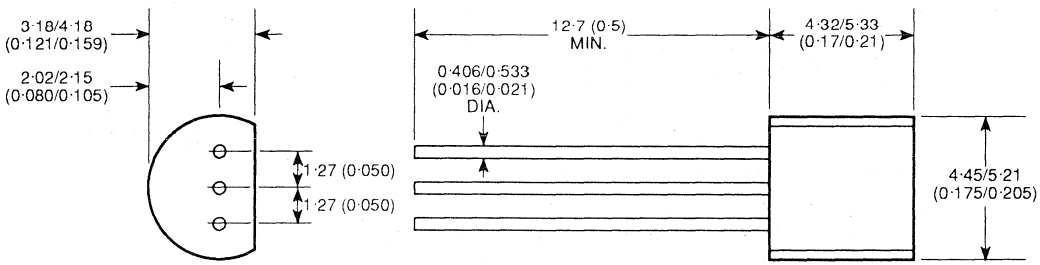


3-PIN MINIATURE PLASTIC DIL - SOT-23



3-LEAD PLASTIC - TO-92

Section 11
GPS Locations

GEC PLESSEY
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GERMANY, AUSTRIA and SWITZERLAND	Ungererstraße 129, 80805 Munchen 40, Germany. Tel: 089/36 0906-0. Fax: 089/36 0906-55
ITALY	Via Raffaello Sanzio, 4, 20092 Cinisello Balsamo (MILAN). Tel: (02) 66040867. Fax: (02) 66040993.
JAPAN	CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.
NORTH AMERICA	P O Box 660017, 1500 Green Hills Road, Scotts Valley, California 95067-0017, USA. Tel: (408) 438 2900. Fax: (408) 438 7023
SOUTH EAST ASIA	No. 3 Tai Seng Drive, GEC Building, Singapore 1953. Tel: (65) 3827708. Fax: (65) 3828872
SWEDEN	Katarina Bangata 79, 116 42 Stockholm. Tel: 46 8 7029770. Fax: 46 8 6404736
TAIWAN, ROC	Room 503, 5F, 131 Min-Sheng E Road, Sec 3, Taipei. Tel: 886 2 5461260. Fax: 886 2 7190260
UK, EIRE, DENMARK, FINLAND and NORWAY	Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts, U.K., SN2 5AF. Tel: (01793) 518510. Fax: (01793) 518582. **Power Division** Carholme Road, Lincoln, U.K., LN1 1SG. Tel: (01522) 510500. Fax: (01522) 510550

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NATIONAL SALES	P O Box 660017, Scotts Valley, CA 95067-0017. Tel: (408) 438-2900. ITT Telex: 4940840. Fax: (408) 438-5576.
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WESTERN	1735 Technology Drive, Suite 100, San Jose, California 95110. Tel: (408) 451-4700. Fax: (408) 451-4710.
ARIZONA/NEW MEXICO	4635 South Lakeshore Drive, Tempe, AZ 85282. Tel: (602) 491-0910. Fax: (602) 491-1219.
SOUTH CENTRAL	9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930. Fax: (214) 680-9753.
NORTHWEST	7935 Datura Circle West, Littleton, CO 80120. Tel: (303) 798-0250. Fax: (303) 730-2460.
DIXIE and FLORIDA	668 N. Orlando Ave., Suite 1015 B, Maitland, FL 32751. Tel: (407) 539-1700. Fax: (407) 539-0055. 385 Commerce Way, Longwood, FL 32750. Tel: (407) 339-6660. Fax: (407) 339-9355.
SOUTHWEST	2600 Michelson Drive, Suite 830, Irvine, CA 92715. Tel: (714) 852-3900. Fax: (714) 852-3910.
DISTRIBUTION SALES	1500 Green Hills Road, Scotts Valley, CA 95066. Tel: (408) 438-2900. ITT Telex: 4940840. Fax: (408) 438-7023.
CANADA	3608 Boul. St. Charles, Suite 9, Kirkland, Quebec, H9H 3C3. Tel: (514) 697-0095. Fax: (514) 694-7006.

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AUSTRALIA	Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia. Tel: 612 638 1888. Fax: 612 638 1798.
FRANCE & BENELUX	Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat.2-B.P. No.142 91944 Les Ulis Cedex A, France.Tel: (1) 64 46 23 45. Fax: (1) 64 46 06 07.
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GERMANY	Ungererstraße 129, D 80805 Munchen 40. Tel: (089) 3609 06 0. Fax: (089) 3609 06 55.
JAPAN	CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.
N AMERICA: Canada	**Alberta Microelectronics Center,** 3553 31st St., N.W., Calgary, Alberta T2L2K7. Tel: (403) 289-2043. **Microstar Technologies,** 7050 Bramelea Rd., #27A Mississaugo, Ontario L5SITI Canada. Tel: (416) 671-8111
USA	P O Box 660017, 1500 Green Hills Road, Scotts Valley, California 95067-0017. Tel: (408) 438-2900. Fax: (408) 438-5576. Two Dedham Place, Suite 1, Allied Drive, Boston, Massachusetts 02026. Tel: (617) 251-0100. Fax: (617) 251-0104. 2600 Michelson Drive, Suite 830, Irvine, CA 92715. Tel: (714) 852-3900. Fax: (714) 852-3910.
Colorado, USA	**Analog Solutions,** 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.
Illinois, USA	**Frederikssen & Shu Laboratories, Inc.,** 531 West Golf Rd., Arlington Heights, IL 60005. Tel: (312) 956-0710.
UNITED KINGDOM	Cheney Manor, Swindon, Wiltshire SN2 2QW. Tel: (01793) 518000. Fax: (01793) 518411. Tweedale Way, Hollinwood, Oldham, Lancashire OL9 7LA. Tel: (0161) 682 6844. Fax: (0161) 688 7898. Doddington Road, Lincoln LN6 3LF. Tel: (01522) 500500. Fax : (01522) 500550.

North American Representatives

ALABAMA	**Electramark, Inc.,** 500 Wynn Drive, Suite 521, Huntsville, AL 35816. Tel: (205) 830-4400 Fax: (205) 830-4406.
ARIZONA	**Fred Board Associates,** 7353 E, 6th Avenue, Scottsdale, AZ 85251. Tel: (602) 994-9388. Fax: (602) 994-9477.
CALIFORNIA	**Gary Chilcote & Associates,** P.O. Box 1795, 1902 Quite Ranch Road, Fallbrook, CA 92028. Tel: (619) 728 7678.Fax: (619) 728 3738. **Jones & McGeoy,** 5100 Campus Drive, Suite 300, Newport Beach, CA 92660. Tel: (714) 724 8080. Fax: (714) 724 8090.
CONNECTICUT	**Stone Components,** 123 Commerce St., Clinton, CT 06413. Tel: (203) 669-4344. Fax: (203)669-9958.
FLORIDA	**American Micro Sales,** 1325 N. Congress Ave., Ste 204, West Palm Beach, FL 33401. Tel: (407) 689 3860.Fax: (407) 689 3168. **American Micro Sales,** 274 Wilshire Blvd., Ste 241, Casselberry, FL 32707. Tel: (407) 831 2505. Fax: (407) 831 1842. **American Micro Sales,** P.O. Box 399, 1033 Rosetree Lane, Tarpon Springs, FL 34688/9. Tel: (813) 938 3073. Fax: (407) 831 1842.
GEORGIA	**Electramark, Inc.,** 6030-H Unity Drive, Norcross, GA 30071. Tel: (404) 446-7915. Fax: (404) 263 6389
ILLINOIS	**Micro Sales, Inc.,** 901 West Hawthorn Drive, Itasca, IL 60043. Tel: (708) 285-1000. Fax: (708) 285-1008.

INDIANA	**Leslie M. DeVoe,** 4371 E. 82nd St., Suite D, Indianapolis, IN 46250. Tel: (317) 842-3245. Fax: (317) 845-8440.
IOWA	**Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666. Fax: (319) 377-2273.
KANSAS	**Lorenz Sales, Inc.,** 8645 College Blvd., Suite 220, Overland Park, KS 66210. Tel: (913) 469-1312. Fax: (913) 469-1238. **Lorenz Sales, Inc.,** 1530 Maybelle, Wichita, KS 67212. Tel: (316) 721-0500. Fax: (316) 721-0566.
MARYLAND	**Walker Associates,** 1757 Gablehammer Road, Westminster, MD 21157. Tel: (410) 876-9399. Fax: (410) 876-9285. **Walker Associates,** 169 Queen Anne Bridge Road, Mitchellville, MD 20716. Tel: (410) 249-7145.
MASSACHUSETTS	**Stone Components,** 2 Pierce Street. Framingham, MA 01701. Tel: (508) 875-3266. Fax: (508) 875-0537. **Stone Components,** 10 Atwood Road, Newburyport, MA 01950. Tel: (508) 462-1079.
MICHIGAN	**Greiner Associates Inc.,** 15224 E. Jefferson Avenue, Grosse Point Park, MI 48230. Tel: (313) 499-0188. Fax: (313) 499-0665.
MINNESOTA	**High Technology Sales,** 4801 West 81st Street, Suite 115, Bloomington, MN 55437. Tel: (612) 844-9933. Fax: (612) 844-9930.
MISSOURI	**Lorenz Sales, Inc.,** 10176 Corporate Square Dr., Suite120, St. Louis, MS 63121. Tel: (314) 997-4558. Fax: (314) 997-5829.
NEBRASKA	**Lorenz Sales,** 2801 Garfield Street, Lincoln, NE 68502. Tel: (402) 475-4660. Fax: (402) 474-7094. **HLM Assoc.,** 333 Littleton Raod, Parsippany, NJ 07054. Tel: (201) 263-1535. Fax: (201) 263-0914.
NEW HAMPSHIRE	**Stone Components,** 436 S. Baboosic Lake Rd., Merrimack, NH 03054. Tel: (603) 429-3462. Fax: (603) 429-3462.
NEW YORK	**HLM Assoc.,** 64 Mariners Lane, Box 328, Northport, NY 11768. Tel: (516) 757-1606. Fax: (516) 757-1636. **Regan Compar,** 3301 Country Club Road, Endwell, NY 13760. Tel: (607) 754-2171 Fax: (607) 754-4270. **Regan Compar,** 214 Dorchester Avenue, Syracuse, NY 13202. Tel: (315) 432-8232. Fax: (315) 432-8238. **Regan Compar,** 37A Brookhill Lane, Rochester, NY 14625. Tel: (716) 271-2230. Fax: (716) 381-2840.
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PENNSYLVANIA/ NEW JERSEY	**Metz-Jade Associates, Inc.,** 7 Wynnewood Rd, Suite 203, P.O.Box 276, Wynnewood, PA 19096. Tel: (215) 896-7300. Fax: (215) 642-6293.
TEXAS	**Oeler & Menelaides, Inc.,** 8430 Meadow Rd., Suite 224, Dallas, TX 75231. Tel: (214) 361-8876. Fax: (214) 692-0235. **Oeler & Menelaides, Inc.,** 8705 Shoal Creek Rd., #103, Austin, TX 78758. Tel: (512) 453-0275. Fax: (512) 453-0088.
WISCONSIN	**Micro Sales, Inc.,** 210 Regency Ct., Suite L101, Waukesha, WI 53186-0545. Tel: (414) 786-1403. Fax: (414) 786-1813.
CANADA	**GM Assoc. Inc.,** 7050 Bramalea Road, Mississauga, Ontario L5S 1T1 (Toronto). Tel: (416) 671-8111. Fax: (416) 671-2422. **GM Assoc. Inc.,** 3860 Cote-Vertu, St. Laurent, Quebec H4R 1N4. Tel: (514) 335-9572. Fax: (514) 335-9573.

GM Assoc. Inc., 301 Moodie Dr., Nepean, Ontario K2H 9CR (Ottawa).
Tel: (613) 820-3822. Fax: (613) 820-7633.
GM Assoc. Inc., 300-3665 Kingsway, Vancouvr, BC V5R 5W2.
Tel: (604) 439-3383. Fax: (604) 439-8479.

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AUSTRALIA and NEW ZEALAND — **GEC Electronics Division,** Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia.
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AUSTRIA — **Eurodis Electronics GmbH,** Lamezanstrasse 10, A-1232 Wien.
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BELGIUM — **ACAL NV,** Lozenberg 4, B-1932 Zaventem. Tel: 02 720 5983. Fax: 02 725 4815.

BULGARIA — **Macro Sofia,** 116 Geo Miller Str, Bl 57 AP70, 1574 Sofia. Tel/Fax: 359 2 708140.

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Semad (Corp.), 85 Spy Court, Markham, Ontario L3R 4Z4.
Tel: (416) 475-8500. Fax: (416) 475-4158.
Semad, 243 Place Frontenac, Pointe Claire, Que H9R 4Z7.
Tel: (514) 694-0860. Fax: (514) 694-0965.
Semad, 6815 8th St. N.E., Ste. 175, Calgary, Alberta T2E 7H7.
Tel: (403) 252-5664 Fax: (604) 420-0124.
Semad, 8563 Government St, Burnaby, BC V3N 4S9.
Tel: (604) 420-9889. Fax: (604) 420-0124.

CHINA — **Gain Tune Ltd,** Room 709, Oriental Building, 39 Jianshe Road,
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Shenzen, China.Tel: 755-2284970. Fax: 755-2284972.

CZECH REPUBLIC — **Macro Weil SRO,** Bechynova 3, 160 00 Prague 6.
Tel: 42 2 3112182. Fax: 42 2 24310335.

DENMARK — **Scansupply A/S,** Gladsaxevej 356, DK-2860 Soeborg.
Tel: 45 39 66 50 90. Fax: 45 39 66 50 40.
Scansupply A/S, Marselisborg Havnevej 36, 8000 Arhus C.
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EASTERN EUROPE — **FA Bernhart GmbH,** Melkstattweg 27, PO Box 1628, D 8170 Bad Toelz., Germany.
Tel: 80 41 41 676 Fax: 80 41 71 504 Tx: 526246 FABD.

FRANCE — **3D:**
6-8 rue Ambroise Croisat, Z.I. des Glaises, 91120 Palaiseau. Tel: 1 64 47 29 29.
Fax: 1 64 47 00 84.
3 rue Berthelot, 69627 Villeurbanne CEDEX. Tel: 72 35 22 00. Fax: 72 34 67 72.
Z.I. du terroir, rue de l'industrie, 31140 Saint Alban.
Tel: 61 37 44 00. Fax: 61 37 44 29.
Parc Club du golf, Batiment 1, 13856 Aix-en-Provence CEDEX 3. Tel: 42 16 77 88
Fax: 42 39 4728.
1 rue de la Faisandereie, Bat B1 P.C. de Tanneries, F-67883 Tanneries CEDEX.
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165 boulevard de Valmy, Evolic Batiment 1, 92706 Colombes.
Tel: 1 46 13 07 80. Fax: 1 46 13 07 90.
ZAC des Petites Landes, 44470 Thouare-sur-Loire. Tel: 40 49 90 90.
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Parc Cadera Sud, Batiment F, 33700 Bordeaux Merignac. Tel: 56 34 46 00.
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Publication No. HB3037-2.0 October 1994

Supersedes 3037-1.0 July 1991 Edition

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